National Aeronautics and Space Administration

Advanced Packaging Class Y – Non-hermetics for Space

Infusion of New Technology into Military Standards

Shri G. Agarwal
NASA – Jet Propulsion Laboratory,
California Institute of Technology
Shri.g.agarwal@nasa.gov
818-354-5598

June 18, 2019

This is NASA InSight's first selfie on Mars. It displays the lander's solar panels and deck. On top of the deck are its science instruments, weather sensor booms and UHF antenna.

Image Credit: NASA/JPL-Caltech

Presented at NASA NEPP ETW, June 17 – 20, 2019

Background

Back in 2009, there was a big push to bring the Xilinx Viirtex-4 (a non-hermetic part) into the QML system as Class V device*. NASA and others were not in favor as it would have created a massive confusion. Mike Sampson conceived the idea of a new Class Y for non-hermetic space parts to provide QML coverage for Xilinx Virtex-4 and similar devices.

*Around the same time, it was uncovered that a supplier was selling non-hermetic versions of TSPC603 32-bit RISC processor as QMLQ (to 5962-97608). So, the non-hermetics had already penetrated the QML system. Upon this finding, DLA removed them from the QML listing.

Creation of Class Y Task Group

A new G-12 Task Group, TG 2010-01, was formed in early 2010 to address non-hermetic devices for space. The team included NASA (Agarwal), the Aerospace Corp. (Harzstark), Boeing (Sunderland) and DLA (Akbar).

This task was challenging because it:

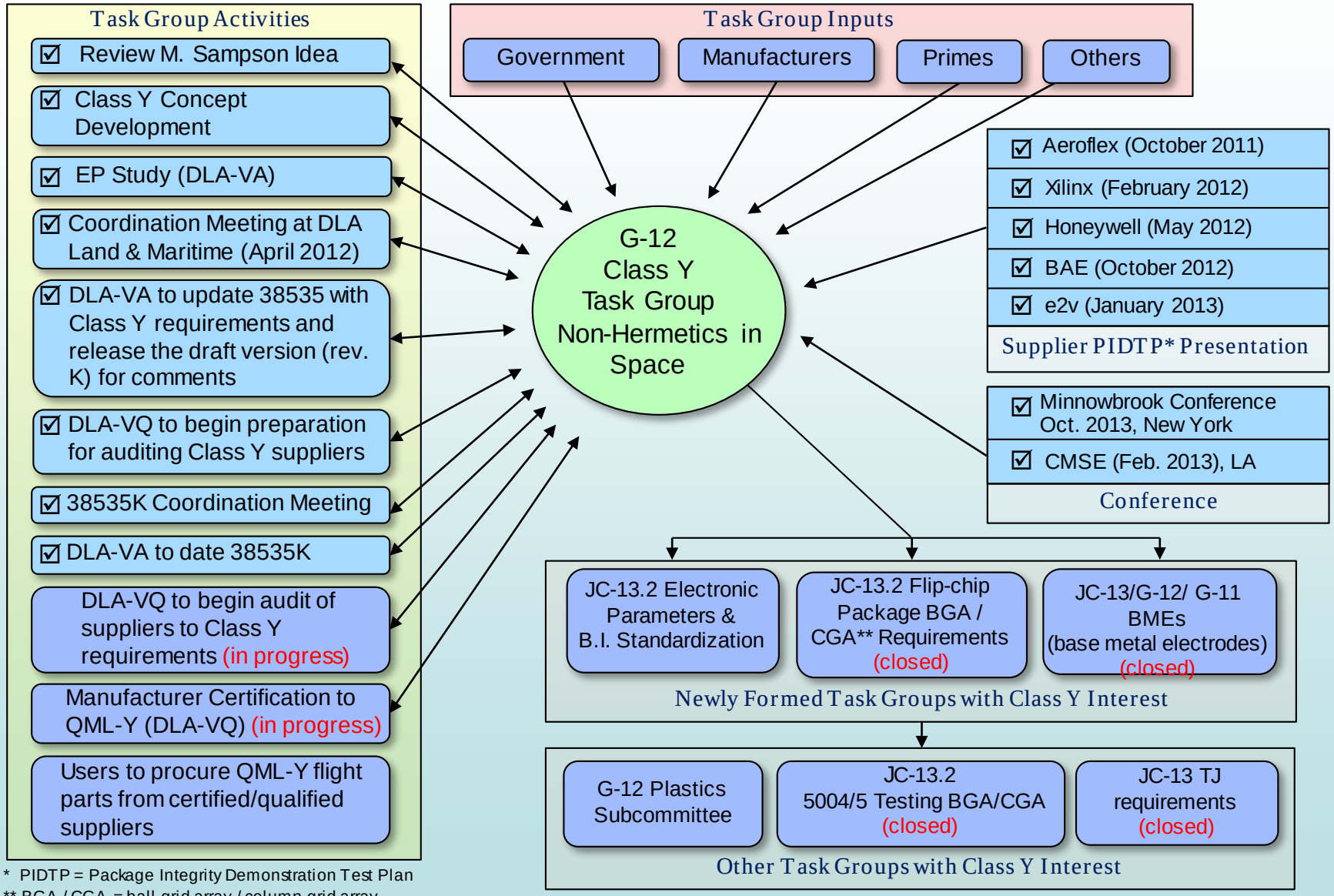
- Was far more involved than typical G12 tasks,
- Required development of a brand new concept,
- Used system-on-a-chip (SoC) — one of the most complicated devices,
- Needed to be simple and easily understood,
- Possessed sketchy testing and board assembly boundaries, and
- Was needed to procure a standard QML product as quickly as possible.

Why "Class Y"?

- The goal of this effort was to bring advancements in packaging technology into the QML system.
- Advancements in packaging technology, increasing functional density, and increasing operating frequency have resulted in single-die SoCs with non-hermetic flip-chip construction, in high-pin-count ceramic column grid array packages
  - "Poster Child" example: Virtex-4 (V-4) FPGAs from Xilinx
  - Such products were evaluated for radiation and reliability and have drawn the attention of the space user community
- Question: How would we bring V-4 and similar microcircuits into the QML system as space products?
  - It couldn't be Class V because those are hermetic devices
  - Our intent was to put V-4 like products for space users in a new category: "Class Y".

- What if we dropped the Class Y effort?
  - It would have been a major loss for the space community and the QML program at large because the industry would be limited to ordering via Source Control Drawings (SCDs), which is counterproductive to Mission Assurance, prevents standardization, and is expensive.

Infusion of the New Class (Y) Technology into the QML System for Space



* PIDTP = Package Integrity Demonstration Test Plan

** BGA / CGA = ball-grid array / column-grid array

NEPAG

Class Y (Contd.)

- Signal Integrity Capacitors
  - Base Metal Electrode construction
  - Developed MIL-PRF-32535 (NASA GSFC, Aerospace, DLA)
  - Several slash sheets, including those for IDCs (Inter digitized capacitors) used on V-4 FPGAs

- Burn-in
  - A new document was written
  - JEP 163
  - Still need to address
    - Alternate burn-in approaches
    - High speed devices (GHz)
    - Hot spots

- Concerns with Handling of Devices
  - Per unit costs are approaching $200k
  - Handling/ESD concerns
  - Electrical testing added after column attach operation

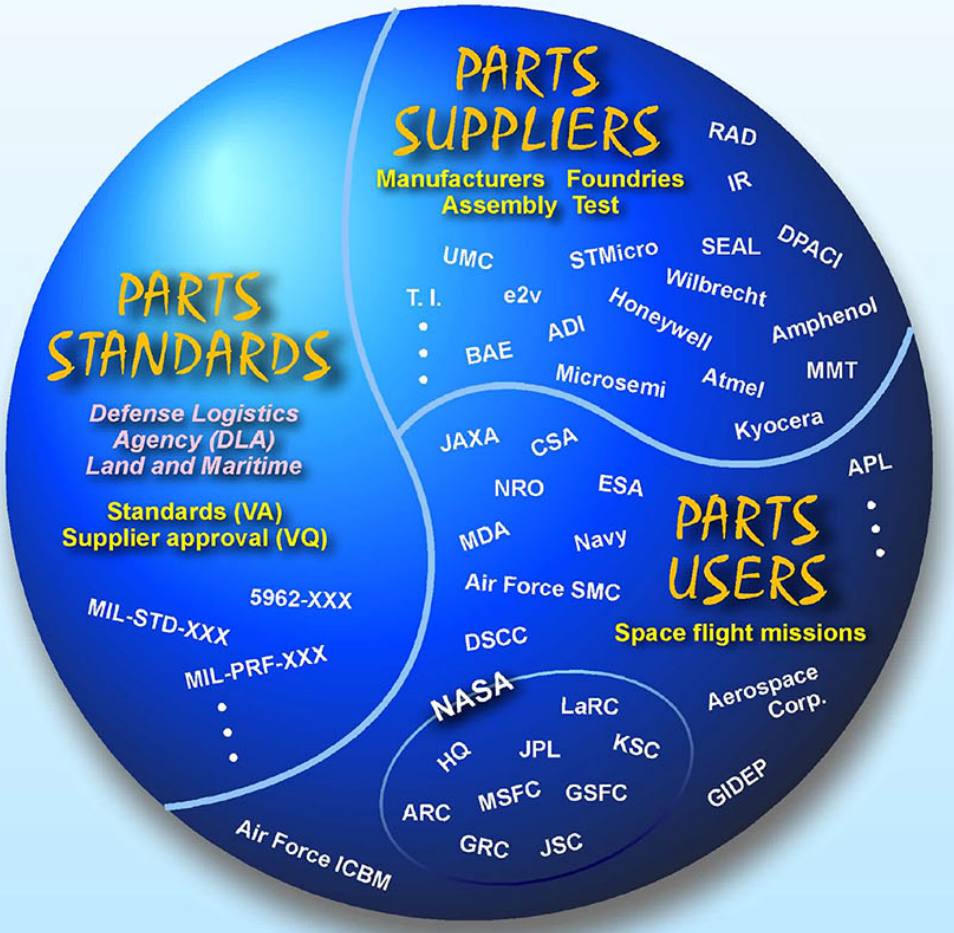
Infusion of New Technologies into MIL/Space Standards: PIDTP and its Applicability

- Issue
  - How to address the manufacturability, test, quality, and reliability issues unique to new non-traditional assembly/package technologies intended for space applications?
- Change in Paradigm
  - Move away from rigid requirements; provide flexibility to manufacturers
- Solution Proposed
  - Introduced a new concept called Package Integrity Demonstration Test Plan (PIDTP)
  - Each manufacturer shall develop a PIDTP that shall be approved by the qualifying activity (QA) for space microcircuits. Ref: MIL-PRF-38535K, Para B.3.11.
- The PIDTP requirement would apply to:
  - Non-hermetic packages (e.g., Class Y). Ref: 38535K, H.3.4.4.1.1.
  - Flip-chip assembly. Ref: 38535K, H.3.4.4.1.2.
  - Solder terminations. Ref: 38535K, H.3.4.4.1.3.
- Microcircuits employing more than one of the above technologies shall include elements for each in the PIDTP. Ref: 38535K, H.3.4.4.1

NEPAG

Space Parts World

NEPAG helps to Develop/Maintain Standards for Electronic Parts



The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD, and others. **For Space microcircuits, DLA, NASA/JPL (S. Agarwal*) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).**

*Also Systems, Standards and Technology Council (SSTC) G-12 Vice-Chair; Chair, Space Subcommittee.

A Changing Landscape (Shipping/Handling/ESD Challenge)

A New Trend – Supply Chain Management
Ensuring gap-free alignment for each qualified product
(All entities in the supply chain must be certified/approved)

Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

More Stops — More Places with ESD Risk

NEPAG

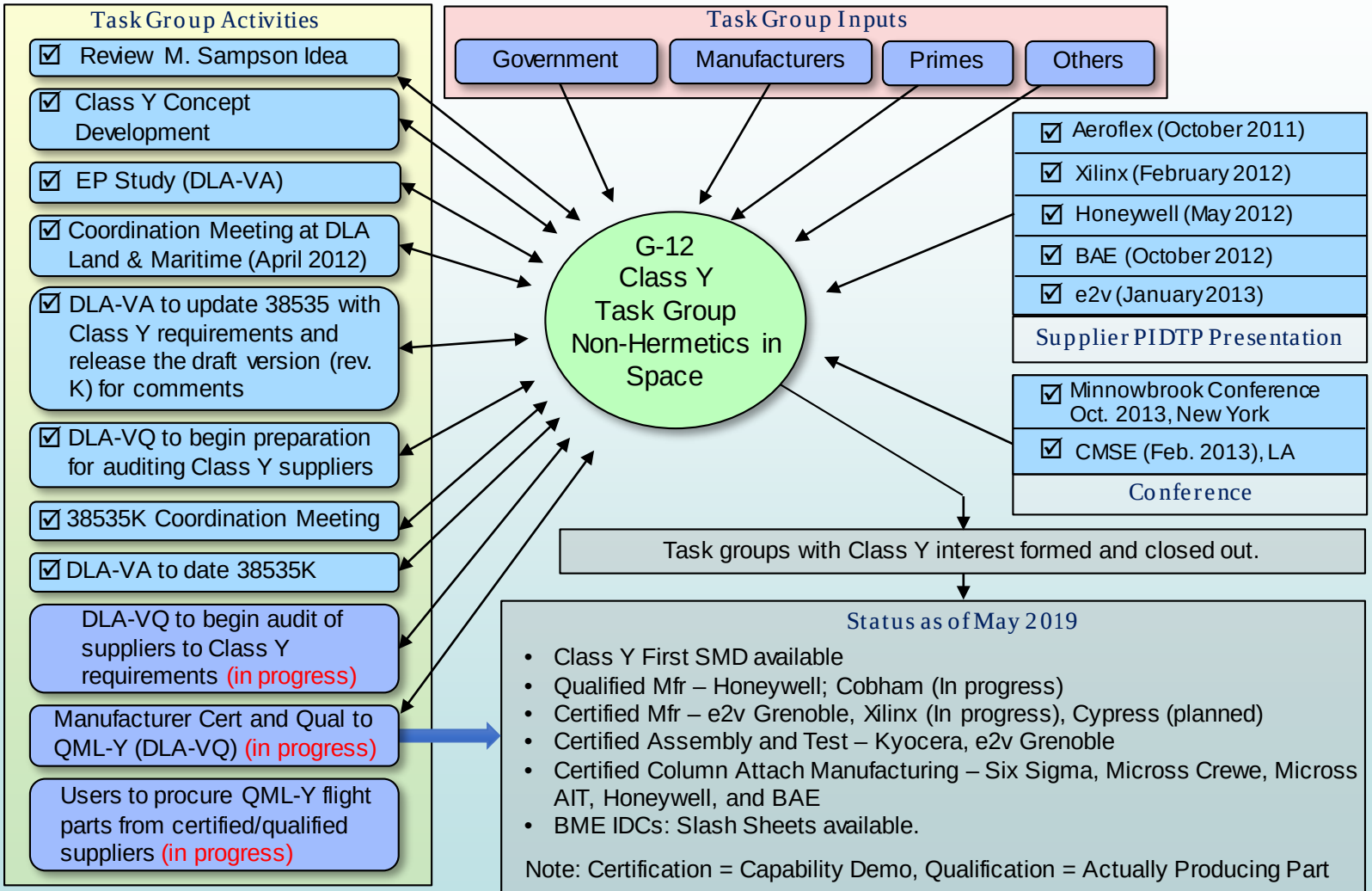
An Example of SMD Boiler Plate Update

TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,2,3,7,8A, 8B,9,10,11 1/	1,2,3,7,8A, 8B,9,10,11 1/
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1, 7 Δ 1/ 2/
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1, 7 Δ 1/ 2/	1, 7 Δ 1/ 2/
6	Final electrical parameters	1,2,3,7,8A,8B,9, 10,11 1/	1,2,3,7,8A,8B,9, 10,11 1/
7	Group A test requirements 3/	1,2,3,4,7,8A,8B,9,10 ,11 4/	1,2,3,4,7,8A,8B,9, 10,11 4/
8	Group C end-point electrical parameters 3/	1,2,3,7,8A,8B, 9,10,11 Δ 2/	1,2,3,7,8A,8B, 9,10,11 Δ 2/
9	Group D end-point electrical parameters 5/	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters 3/	1,7,9	1,7,9
11	Column attach 6/	1,7,9	1,7,9

- For Flip-chip column attach
  - Add room temperature electricals (subgroups 1, 7, 9) after column attach – step 11 above

Infusion of the New Class (Y) Technology into the QML System for Space (Status given at JEDEC in May2019)



BGA / CGA = Ball-Grid Array / Column-Grid Array
BME = Base Metal Electrode
IDC = Inter Digitized Capacitor

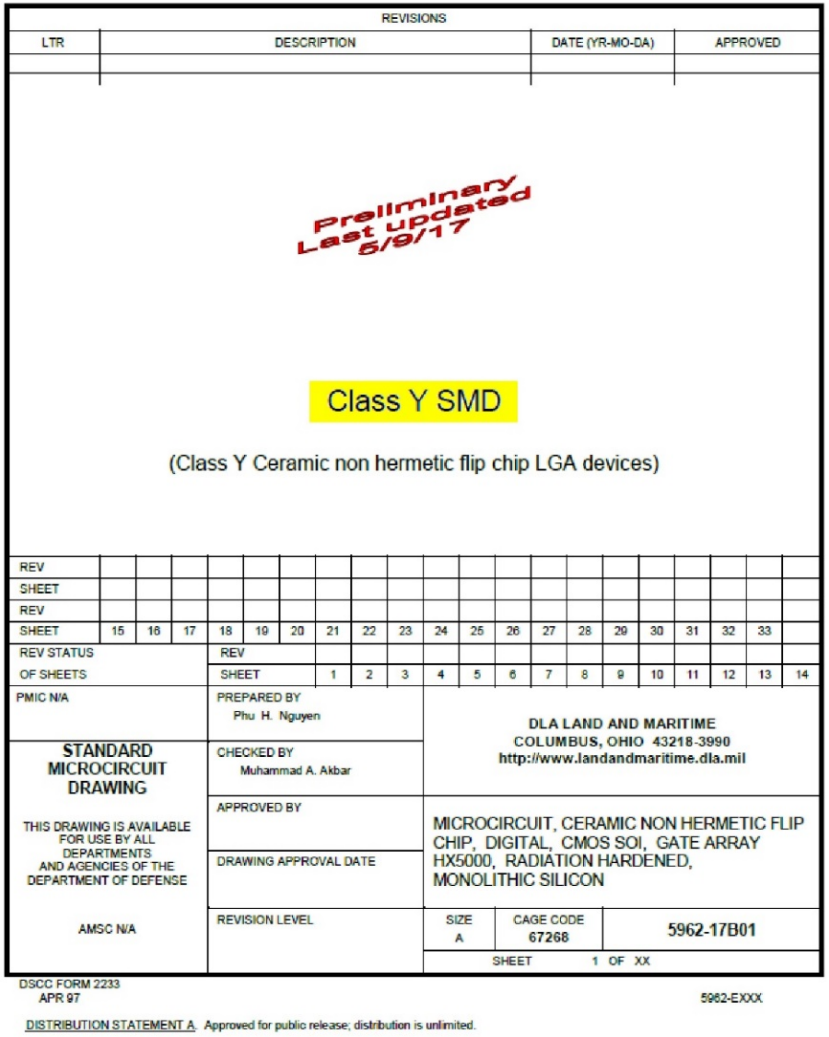
PIDTP = Package Integrity Demonstration Test Plan
SMD = Standard Microcircuit Drawing

NEPAG

Class Y Qualification Status

- Honeywell Aerospace - Plymouth
  - Complete
  - SMD 5962-17B01
  - Title: Microcircuit, Ceramic Non-Hermetic, Flip Chip, Digital, CMOS SOI, Gate Array, HX5000, Radiation Hardened, Monolithic Silicon
- Cobham Colorado Springs
  - In progress
  - SMD 5962-17B02
  - Tentative Title: Microcircuit, Digital, Radiation Hardened, 90nm Standard Cell, Monolithic Silicon, Class Y, Radiation Hardened, Monolithic Silicon
- Teledyne e2V Grenoble France
  - In progress
  - SMD 5962-19205 (just got assigned)
  - High performance processor, PC8548

First SMD for Class Y Part



REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Preliminary
Last updated
5/9/17

Class Y SMD

(Class Y Ceramic non hermetic flip chip LGA devices)

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
REV STATUS				REV															
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Muhammad A. Akbar	
	APPROVED BY	MICROCIRCUIT, CERAMIC NON HERMETIC FLIP CHIP, DIGITAL, CMOS SOI, GATE ARRAY HX5000, RADIATION HARDENED, MONOLITHIC SILICON
	DRAWING APPROVAL DATE	
AMSC N/A	REVISION LEVEL	SIZE A / CAGE CODE 67268 / 5962-17B01
		SHEET 1 OF XX

DSCC FORM 2233
APR 97

5962-EXXX

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: XX-XX-XX

Approved sources of supply for SMD 5962-17B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN
5962H17B0106YXC	34168	HX518X
5962H17B0106YYC	34168	HX518Y

1/ Microcircuits devices supplied to this drawing are land grid array (LGA) packages with lead finish mark letter C (gold). However,for future AID drawing column grid array (CGA) or ball grid array (BGA) packages terminal lead finish mark shall be provided with "F".

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Aerospace - Plymouth 12001 Highway 55 Plymouth, MN 55441-4744

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

NEPAG

Moving Forward

- TG10-01 effort resulted in a major overhaul of the specification MIL-PRF-38535 was done with respect to requirements for flip-chip, underfill, CSAM, column grid arrays, etc. Revision K reflecting these changes was released in December 2013.
- A Follow-on to Ceramic Substrate Class Y
  - Interest in organic Class Y, and molded plastic parts is growing.
  - The JC-13.7 created a new task group on organic substrate Class Y (September 2018).
  - Related task groups started as well
- Defense Logistics Agency (DLA) conducted an EP (Engineering Practice) study

JC-13.7/CE-12 Task Group 2018-02
Class Y Expansion to Organic Substrates

- Notional Milestones/Schedule for 2019 and 2020
  - What do we want to accomplish by the end of 2019?
    - ❖ Organic Class Y definitions and technology classes (Done)
    - ❖ DLA Engineering Practice, EP, Study (Done)
    - ❖ NASA NEPP Special Bulletin article (In Progress)
    - ❖ Define PIDTP risk areas
    - ❖ Preliminary PIDTP demonstrations
    - ❖ Organic Class Y poster child identification
    - ❖ Determine if new QML designation is needed, or use Class Y or Class N? (Tied to EP. Doesn't appear that a new QML designation will be needed.)
  - What do we want to accomplish by the end of 2020?
    - ❖ Poster child characterization and qualification demonstration
    - ❖ Recommendations for technology insertion into MIL-PRF-38535 and MIL-STD-883
- Bi-Weekly Conference Calls Starting on January 30

Credit: Scott Popelar, Cobham, 2019 MRQW, February 7, 2019

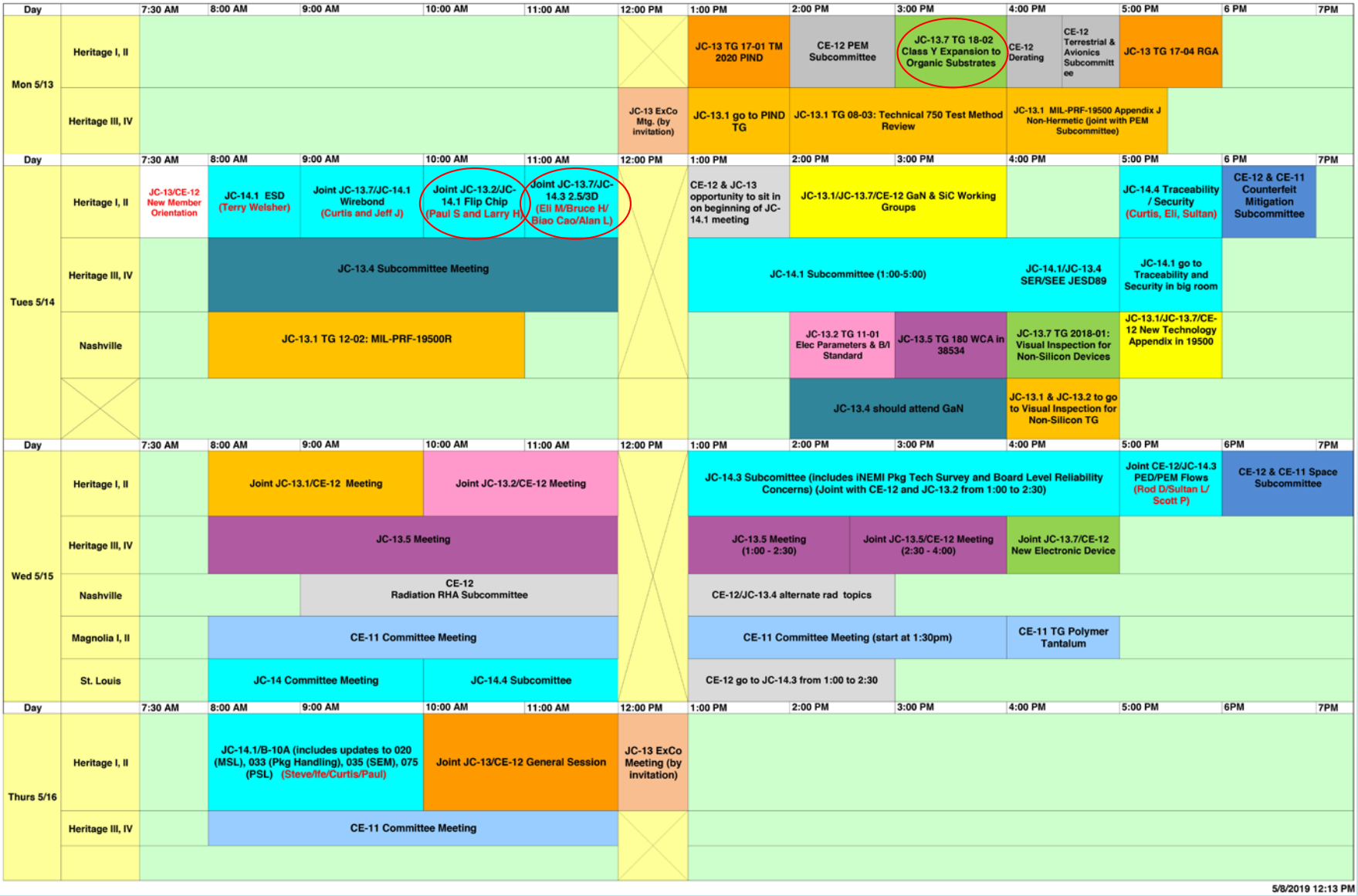
Current Efforts

- Four Related Efforts Underway
  - JC-13.7 TG 2018-02
    - Class Y Expansion to Organic Substrates. POC: S. Popelar
  - JC-13.2 TG 2018-01
    - Review/update flip chip evaluation criteria. POC: P. Syndergaard
  - JC-13.7 TG 2015-01
    - Use and test of 2.5D/3D packaging. POC: B. Hughes/E. Minson
  - JC-13.7 TG 2017-01
    - Use of Pb-free solder in 38534/38535 devices. POC: A. Touw/P. Nixon
      - Commercial industry is moving away from leaded products.

- Alignment is in progress
  - Avoid overlaps

- NEPP 2.5/3D Task
  - Develop a book of knowledge (BoK). POC: D. Sheldon
  - Feed into JC-13 effort

JEDEC/CE May 2019 Meetings Grid



JC-13.7/CE-12 Task Group 2018-02
DLA Engineering Practice (EP) Study

EP study on
Update of non-hermetic microcircuits class N (military, terrestrial and avionics application and class Y (Space application) to MIL-PRF-38535.

I. OBJECTIVE: The purpose of this Engineering Practice (EP) Study is to obtain input and justification from the military services, microcircuit manufacturers, and space application user's communities, concerning the update/addition of non-hermetic class N (military, terrestrial and avionics application) and class Y (non-hermetic Space application) microcircuits to MIL-PRF-38535.

II. BACKGROUND: MIL-PRF-38535 offered non-hermetic class N (plastic package) and class Y (ceramic substrate non-hermetic device for space application). In table IB, class N has an inclusive table that comprises screening and QCI tests requirement, which called tests/monitors for plastic package. However, this inclusive table fails to distinguish between screening and QCI test flows that creates confusion with periodic QCI test monitoring issue as well as product reliability.

On the other hand, design requirement of modern electronics satellite/warfare systems are growing faster and moving forward with an advance and complex package technologies. Considering complexity of new technologies and device packaging techniques, JEDEC CE-12 formed a task groups (TG) for exploring the state of the art class Y concept to develop a new organic substrate flip chip devices, and 2D, 2.5D and 3D package technology requirements for qualification and screening of non-hermetic microcircuits packages for space applications.

Accordingly, to bring advancement and adopting new package technologies into QML system to MIL-PRF-38535, DLA Land and Maritime-VAC is conducting an EP study (phase 1) which includes:

(1) Update class N with separating screening and QCI tables to make robust high reliability plastic encapsulated microcircuits(PEM) devices for military, terrestrial and avionics application;

(2) Update/create a new appendix K (Next Gen) with other appendix/sections update for non-hermetic microcircuits devices that includes organic/ceramic substrate flip chip devices, 2D, 2.5D and 3D package technology requirements for space applications.

DLA Land and Maritime-VAC is requesting to review all attachment and send comments and feedback to DLA within the stipulated time for discussion and further development. Survey questionnaire (**see attachment # 1**) to evaluate the industries overall opinion for adding/updating class N and class Y devices package construction technical issues. Proposed non-hermetic class N and class Y devices screening and QCI requirements (**see attachment # 2**). Proposed update Appendix H (new technology qualification including PIDTP update (**see attachment # 3**). Proposed addition of Appendix K (Next Gen) for non-hermetic class Y devices including organic/ceramic substrate flip chip device, 2D, 2.5D and 3D package technology requirements for space applications (**see attachment # 4**).

New Appendix K (Next Gen)

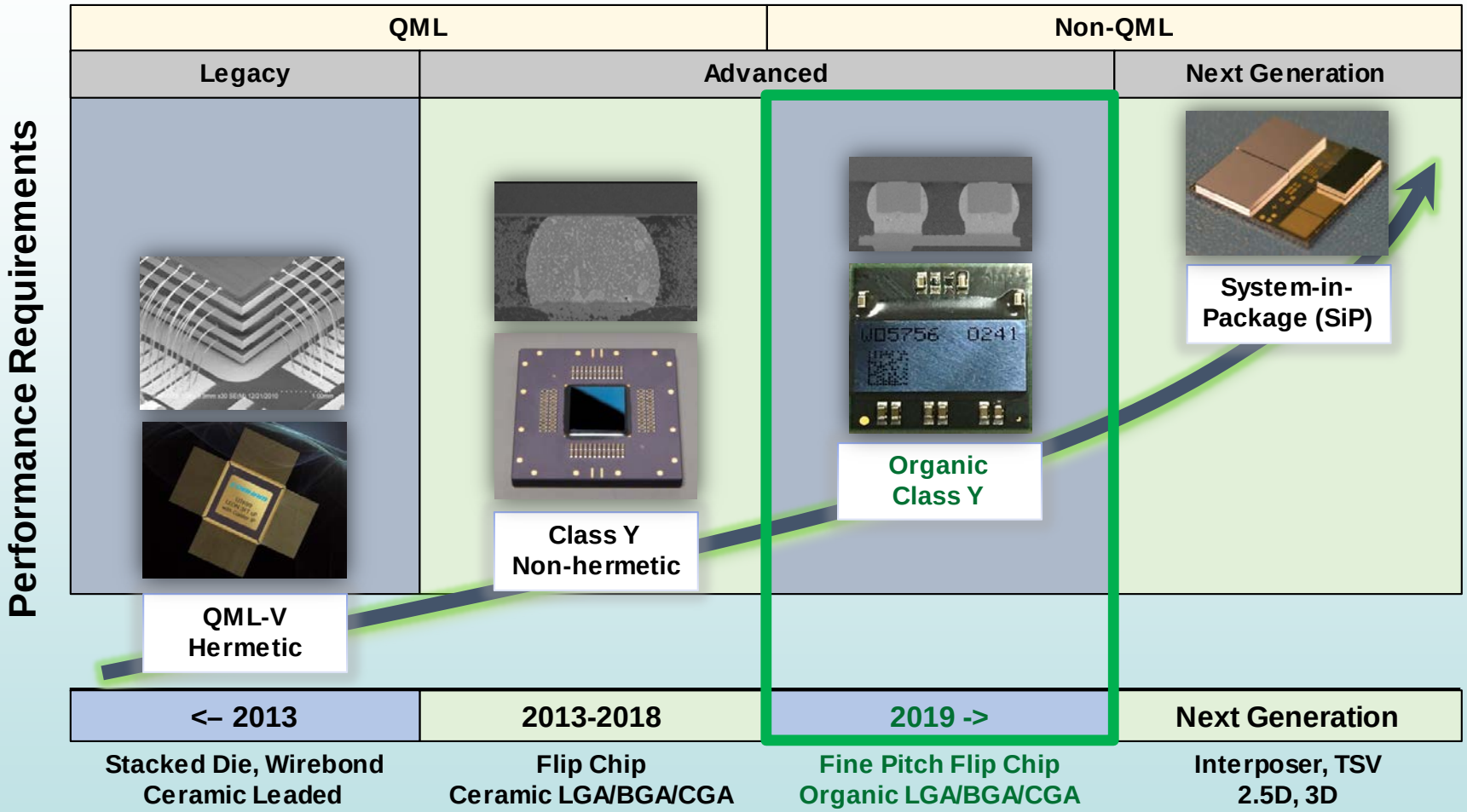
- This appendix is expected to take 2-3 iterations

- Have the 2.5D/3D TG develop it.
  - Manufacturability, test, quality and reliability issues unique to these non-traditional assembly/packaging technologies intended for space applications
  - Identify/use a poster child

- Among other things, the TG to make recommendations on PIDTP candidates
  - Heat sink – could be covered under flip-chip PIDTP category
  - Capacitor attach (for signal integrity) might be a separate PIDTP category, but should be generalized to accommodate other variations (not just capacitors)
  - Treat silicon interposer (2.5D) as another type of substrate
  - TSV, which enables 3D, could be another PIDTP "nonstandard assembly technology."
  - Etc.

Next Generation Package Technology for Space

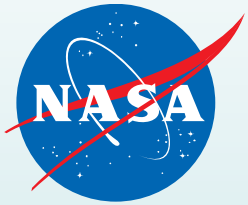
Development Roadmap for Space Applications



Package Technology Availability

Credit: Scott Popelar, Cobham, 2019 MRQW, February 7, 2019

http://nepp.nasa.gov



ACKNOWLEDGMENTS

The research described in this publication was carried out, in part, at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Help is gratefully acknowledged from Melissa Klose, Nazia Ovee, Mohammad Mojjaradi, Joon Park, and Michael Sampson.

Government sponsorship acknowledged.

NEPAG