Advanced Non-Volatile Memories (NVM)

Jean Yang-Scharlotta
jean.yang-scharlotta@jpl.nasa.gov
818-354-0412
Jet Propulsion Laboratory –California Institute of Technology

Acknowledgment:
This work was sponsored by:
NASA Office of Safety & Mission Assurance
Copyright 2019 California institution of Technology
Government funding acknowledged

Open Access

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Outline

• Introduction- Tracking and Evaluating Memory Technologies
• Roadmap Recent Tests
• Emerging Memory Update 2019
  – STT-MRAM
  – Future Plans
• NAND Flash Update 2019
  – Newly developed universal NAND reliability tool
  – Future Plans
NEPP – Memories Ongoing Activities

Emerging Memories
- Resistive
  - Fujitsu/Panasonic
  - GF/Intel
- Spin torque transfer magnetoresistive
  - Everspin, Avalanche
- 3D Xpoint
  - Intel Optane
- Enabling “universal” memories

DRAMs
- DDR4 test capability (in progress)
- Commercial DDR (various)
- Tezzaron DiRAM
- Enabling high performance computing

Commercial Flash
- 3D
  - Samsung, Hynix, Micron
  - Planar SLC
  - Enabling data storage density

Best Practices and Guidelines

Partnering
- Navy Crane
- NASA STMD
- Everspin
- University of Padova

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Commercial NVM Technology Roadmap
- collaborative with NSWC Crane, others

Other
- STT-MRAM (Avalanche, Everspin (STMD))
- FeRAM

Resistive
- CBRAM (Adesto)
- ReRAM (Panasonic/Fujitsu)
- 3D XPoint (Intel Optane™)
- TBD (HP Labs, Intel, GF?)

NAND FLASH
- Samsung VNAND
- Micron planar (16nm)
- Micron 3D
- SK Hynix 3D, other

TBD – (track status)

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Emerging Memory in 2019

• STT-MRAM gaining wide adoption as embedded flash replacement around 22-28nm nodes
  – Intel announced p-STTMRAM production on 22nm FINFET technology in Feb (ISSCC)
  – Samsung announced e-STMRAM production on 28nm FDSOI technology in May
  – Global Foundries had previously reported that it plans to have STTMRAM as embedded memory in its 22nm technology
    • Also fabricating Everspin’s 1Gb STTMRAM on its 28nm CMOS technology
    – UMC licenced 28nm STTMRAM from Avalanche

• Memory has internal EDAC- should be considered in application


To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Spin Torque Transfer Magnetic Memory (STT-MRAM)

- STT-MRAM is a near term storage & working memory technology
  - MRAM already used in RH applications
- STT-MRAM enables further scaling of density well above current RH availability in toggle MRAM at 16Mb/chip
Spin Torque Transfer Magnetic Memory (STT-MRAM)

• **Everspin Technologies**
  - 1st Gen Toggle MRAM in 16Mb RH chips offered by Honeywell and Cobham
  - New STT-MRAM **256Mb DDR3** chip targeting high speed and high density, 1Gb part coming soon
  - 256Mb chip had some test done for STMD in FY18
  - Of interest for RH processor system memory

**Test Results (Guertin et al., RADECS 2018)**
- Tests were done unbiased due to interest as candidate for Rad Hard memory part and shows memory core quite robust in radiation
- TID test show no data loss up to 1.5Mrad (Si) for the part
- TID testing on the memory cell show no bit flips up to 7Mrad(Si)
- SBU cross section <1×10^{-7}cm^2 at LET 33.7 MeV-cm^2/mg.

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Emerging Memory Looking Forward

• The value of tracking commercial development through partnership is demonstrated, and continuing

• Dual track study example- STTMRAM
  – include fundamental memory device testing and production part testing at the same time
  – allowed for separation part level reliability and radiation performance (influenced by manufacturer dependent support circuitry design) from fundamental reliability of the memory core itself which should remain constant from manufacturer to manufacturer for the same device architecture.
  – Currently MRAM fundamental device study is on-going with Everspin and University of Minnesota

• Technology Tracking and Testing in 2019 will continue to
  – Track the more mature STT-MRAM and test new products for potential use for agency-wide information gathering
  – Continue to track RRAM which continues with substantial industry development, and other emerging memories as new products and architectures become available for testing
Diatribe: Gartner Hype Cycle Concept

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
NAND Flash in 2019

• NAND Flash continues to scale in 3D
  – Very mature, bulk of NAND production
  – Scaling is by inc. # of stacks, now 96 or 128 layers
  – For leading manufacturer Samsung, 6th generation VNAND announced

• Planar scaling has slowed down but availability is steady
  – Automotive market sustaining high reliability SLC products

From ISSCC 2019, Samsung
From this GSFC test result (2017) we see that SLC mode operation is less susceptible to SEU than MLC from both manufacturers.
NAND Flash in 2019

• Implications of NAND Manufacturers Targeting the Automotive Market
  – More choices for high reliability parts
    • High density SLC parts now available in planar and in 3D NAND with SLC mode
    • Wider selection of densities, technologies and manufacturers available for high reliability needs
    • Versus managed NAND such as SSD, iNAND, eMMC, SD cards which dominate the market and manufacturer support. e.g. Samsung VNAND is only available as SSD
  – Wider operating temperature range available
  – More product longevity ( >10 yr vs 2-4yrs)
    • If we qualify a part, there is greater chance for reuse in future missions
    • Greater incentive to do more in-depth evaluation of NAND parts

➢ New NAND reliability eval tool
Pulsed/Partial Programming Bit Evaluation Tool

- Method introduced by Navy Crane demonstrating ability to interrupt NAND programming sequence to create bit level analysis of NAND parts (Roach et al, TNS, 2015)
- We have developed this test as part of an internal R&TD task on a commercial NAND tester and built a GUI interface to be a readily available tool to evaluate bit level performance for any SLC NAND
  - Useful for comparing manufacturers, technology nodes, or even for screening
  - FY19 plan is to compare 2D NAND vs 3D NAND in reliability
- Identifies outlier “weak” bits which are often the first to fail in reliability and possibly radiation
  - Key in on number and range of “weak bits” to compare
How Does Pulsed Programming Work?

1. Program command
2. Reset after time “t” - Pulse width
3. Read
4. REPEAT

Commercial tester runs the test through a GUI.

- The resolution of pulse width is limited by the FPGA, which is 50 ns

CHIPS

BLOCK

PAGE

BIT

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Distribution of bits in programming speed (pulses) within a single page of NAND bits

Allows for the identification of tail or “weak” bits universally in all NAND parts
Higher level data - programming speed for a block of pages

Program pulses decreases with endurance stress and increases with TID exposure

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Programming data for multiple blocks showing the last 5% of the bits require ~ 90% of the programming time.

This method is scaled to examine the entire chip to identify the slow “weak” bits—programming time and address...
Weak tail bits take ~ 90% of the programming time and statistically the first to fail.

We expect this trend to worsen with technology shrink due to lower number of electrons stored = wider statistical variation.

Identifying weak bit trends across part numbers, manufacturer and even parts in a lot allows selection of more reliable parts.
Weak Bits @ t=0 Identifies Reliability and Radiation Vulnerability

Pre/Post Reliability Correlation

Pre/Post TID Radiation Correlation

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
Applicability Across Manufacturer Demonstrated

Vendor 1
Vendor 2
Vendor 3

Interrupt program pulses

# of unprogrammed bits in the page

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.
NAND Flash Future Plans

- For 2019 we will utilize the pulsed programming tool to test Micron and Hynix 3D NAND chips for a comparison of the two fundamental devices used (floating gate versus charge trapping) as well as comparison to 2D NAND reliability performance.

- Moving forward, we plan to continue to track new 3D NAND and new automotive grade 2D NAND development and test for technology upgrade impact on reliability and radiation effects.
APPENDIX

Hynix 3D 1X nm NAND equivalent
FIB Cross-Section- 128Gb

Cross section showing FLASH array transition to periphery. Connections are identified for reference to higher magnification images below. Cross sections were taken along the Y-Axis

Higher magnification images of array connections
Hynix 3D NAND (128Gb, MLC) initial construction SEM analysis reveals a single die with 3D construction comprising of 40 physical device layers and staircase array edge connection.

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 26-29 2017