Radiation Testing of Advanced Non-Volatile Memories

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## Acronyms

<table>
<thead>
<tr>
<th>BER: Bit Error Rate</th>
<th>Program</th>
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<tbody>
<tr>
<td>CMOS: Complementary Metal-Oxide Semiconductor</td>
<td>NVM: Non-Volatile Memory</td>
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<tr>
<td>COTS: Commercial Off The Shelf</td>
<td>nvSRAM: Non-volatile SRAM</td>
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<tr>
<td>DRAM: Dynamic Random Access Memory</td>
<td>QLC: Quad-level Cell</td>
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<td>ECC: Error-Correcting Code</td>
<td>RBER: Raw Bit Error Rate</td>
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<td>EDAC: Error Detection and Correction</td>
<td>SBU: Single Bit Upset</td>
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<tr>
<td>EEPROM: Electrically-Erasable Programmable Read-Only Memory</td>
<td>SEE: Single Event Effects</td>
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<tr>
<td>FRAM: Ferroelectric RAM</td>
<td>SEFI: Single Event Functional Interruption</td>
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<tr>
<td>GEO: Geostationary Earth Orbit</td>
<td>SEU: Single Event Upset</td>
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<td>LET: Linear Energy Transfer</td>
<td>SLC: Single-level Cell</td>
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<td>MBU: Multiple Bit Upset</td>
<td>SRAM: Static Random Access Memory</td>
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<tr>
<td>MCU: Multiple Cell Upset</td>
<td>SSD: Solid State Drive</td>
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<tr>
<td>MLC: Multi-level Cell</td>
<td>SSR: Solid State Recorded</td>
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<td>MRAM: Magnetoresistive RAM</td>
<td>STT-MRAM: Spin-torque Transfer MRAM</td>
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<tr>
<td>NAND: Not AND (Flash Technology)</td>
<td>TID: Total Ionizing Dose</td>
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<tr>
<td>NEPP: NASA Electronics and Packaging</td>
<td>TLC: Triple-level Cell</td>
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<td></td>
<td>UBER: Uncorrected Bit Error Rate</td>
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To be presented by Ted Wilcox at the 2019 NEPP Electronics Technology Workshop (ETW), NASA GSFC, Greenbelt, MD, June 17-20, 2019.
Outline

- Non-Volatile Memory Technologies
- Tests, Testability, and Facilities Of Use
- Typical Memory Test Setups
- Recent Radiation Results
- Ongoing Testing & Future Plans
NVM Technology

• **Advanced Non-Volatile Memories Are:**
  – Technologies or products used for long- and intermediate-term storage of data in a non-volatile storage cell
  – Typically used in
    • EEPROMs & nvSRAMs (serial, small, random access)
    • Solid-State Recorders (complex, large, sequential access)
    • Boot PROMs / MCU code memory (small, random access, hi-reliability)
    • Certain FPGAs and embedded applications

• **Embedded or DRAM-like NVM technologies are a collaborative effort with other NEPP tasks (scaled CMOS evaluation, DDR memories)**

*NEPP’s focus here is technology evaluation*
Common NVM Technologies (today…)

NOR Flash
- Electrical charge
- Random Access
- Low Density
- Simple interface
- Limited endurance
- Varied rad tolerance
- Example Usage: FPGA configuration

NAND Flash
- Electrical charge
- Seq Access
- Highest Density
- Complex interfaces
- Very limited endurance
- Limited rad tolerance
- Example Application: bulk data storage

FRAM
- Ferroelectric orientation
- Random Access
- Low Density
- Simple interfaces
- High endurance
- Rad tolerant

ReRAM, 3DXPoint, PCM, CBRAM
- Resistive memory
- Random Access
- Lowest to Highest Density
- Varied interfaces
- Very high endurance
- Excellent rad tolerance
- Still developing…

STT-MRAM
- Electron spin
- Random Access
- Lowest* Density
- Simple interfaces
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NOW TESTING

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Common NVM Radiation Test Interests

Memory Cell SEU
- Powered off state to isolate from control circuitry
- Powered on and dynamic tests to evaluate differences
- Consider number of bits relative to fluence
- SBU vs. MBU, angular effects, data pattern, etc

Peripheral Circuitry SEFI
- Powered on and operating dynamically
- Depends on underlying tech, but can reveal error signatures typical for a memory type

TID Tolerance
- Evaluate all operational modes
- Irradiate in appropriate conditions (worse case? flight-like?)
- Failure distributions, lot-specific testing issues

Memory-Specific Hard Failures
- Stuck bits
- Broken program/erase circuits

Single-Event Latchup
- Powered on, static and dynamic
- High voltage and temperature
- Focus on power supply and recovery, less on SEFI that will inevitably occur
- Strongly dependent on fab process

Relative importance of each varies tremendously by technology and application

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Heavy Ion Testing

Memory Cell SEU
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Ideal
Helpful
Not Useful
Co-60 Irradiation

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Ideal
Helpful
Not Useful
Pulsed Laser

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Ideal
Helpful
Not Useful
High Energy Protons

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- Broken program/erase circuits

Ideal
Helpful
Not Useful
Testability & Challenges

• **We want to evaluate rad tolerance of memory blocks**
  – Product-level performance data is great too
  – But sometimes the product limits our view → What’s happening inside?

• **Not always easy to decouple memory errors from controller errors or see past EDAC**

• **Can’t always shield or remove controlling circuitry.**

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**TID:**
- Limited biasing configurations
- May be able to place controller a few feet away and heavily shield

**Heavy Ions:**
- Easy to “shield” controller
- Impossible to fully test large memories in real-time
- Vacuum chamber feed-thrus limit speed or prevent testing entirely

**Laser**
- Focus on individual memory cells or raster across control circuitry
- But memories often have a LOT of metal on top and large areas

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Sample Memory Tester Setups

- **COTS ARM Microcontroller Boards**
  - < $30
  - Easy toolset & programming; low-level bare-metal access
  - Up to 240 MHz CPU core
  - 10Mbps USB link to PC
  - Not appropriate for DRAM, high-bandwidth, or timing-sensitive devices
  - Sufficient for heavy ion testing, some TID, but not proton tolerant

- **PC-based m.2 PCIe tests**
  - PCIe to Thunderbolt 3 for high-speed testing (TID)
  - PCIe to USB bridge for low-speed testing at long-distance (e.g. SEL/SEFI)
Recent Results – Avalanche STTMRAM

- Currently evaluating 40nm sample parts
- pMTJ STT-MRAM
- 16Mb serial nvSRAM

- Memory array cells proven at 55nm node:
  - No SEU after $1.1 \times 10^7$/cm$^2$ @ 85.4 MeV·cm$^2$/mg
  - Fully functional, no errors after 500+ krad(Si)

- Overall performance depends on underlying CMOS process:
  - Low SEFI threshold for control circuitry
  - Latchup investigation at 40nm
    - Focused laser testing

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Recent Results – 3D NAND Flash

• Planar NAND flash limited by CMOS scaling
  – Step back a few nodes but grow vertically (96+ layers!)
• Extensive SEE/TID testing of Micron 32-layer 3D NAND for flight use

• Some SSD test data on:
  – Intel, Micron 64-Layer
  – WD/SD/Toshiba 64-Layer
  – Samsung 64-Layer
  – more coming soon…
Recent Results -- 3D NAND Flash

- Three-dimensional ion track structure can be determined experimentally, and results look exactly as you’d expect:

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Recent Results – 3D NAND Flash

- 3D, MLC+ NAND has high ECC requirements based on normal “background” errors intrinsic to NAND flash (left)

Non-irradiated part (MLC)  
After 1x10^6/cm² Neon (MLC)  

Plus Heavy-Ion Irradiation
3D NAND Flash TID Testing

- Memory devices – like everything EEE – are getting complicated.
- Are we testing complex devices in a worst-case configuration?

“It’s CMOS. Biased is probably worst-case, but we’ll do half the parts grounded just to be sure.”
3D NAND Flash - Biased vs Unbiased TID

Erase circuitry is flash’s weakest link

Biased irradiation appears slightly worse than unbiased

Micron 32-layer NAND tested in SLC mode

The big question: Are we good to fly?

Biased irradiation appears slightly worse than unbiased.
What if we dynamically operate device to keep our weak link operational?

Highly application-specific testing...

Don’t forget about endurance limitations – in this case we had 30,000 cycles to play with.
3D NAND Flash TID (Rewrite)

- Well-established that erase circuitry is weakest link for TID (high-voltage CPs)
- Commonly fail 20-75 krad (Si) while program and read circuitry may last longer
- In continuous rewrite application, retention errors are minimal but eventually we can’t program clean data
3D NAND Flash TID (Read Only)

• Consider a read-only test:
• Traditional dose-step testing does not thoroughly exercise anything
• Time between steps limits ability to implement heavy testing at each dose
• Always consider your application!
MLC vs SLC

- So far, applications seem to be using SLC devices or “SLC mode” if at all possible – for performance and endurance... not thinking rad
- MLC doubles our density but at what cost to rad tolerance?

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3D NAND Flash TID

• Still processing data to evaluate:
  – Memory fidelity: Read-only (retention) results, effects on R/W cycle (endurance) limits
  – 3D Factors: Bit error rate vs layer/position seems to vary
  – Mode of operation: Need more MLC TID data
  – Facility Factors: Angle of irradiation, dose rate, time-to-measure

• End Goal: NEPP will have extensive data on SEE and TID test configurations as a solid baseline comparison for future 3D NAND flash
Other Plans Moving Forward

- **3D NAND Flash**
  - Piece-part testing when able, particularly as projects begin to use them!
  - SSD testing as a rough figure; a work in progress…
  - These parts will be (or are!) obsolete long before they fly

- **STT-MRAM**
  - Possible add’l testing on 40nm Avalanche STT-MRAM
  - Avalanche 40nm STT-MRAM TID testing ~Fall
  - Embedded MRAM testing collaborations with other NEPP tasks

- **Intel Optane**
  - Basic proton and heavy-ion SEU data
  - 3D X-Point (Intel Optane) TID testing imminent

- **Identify emerging non-flash technologies & partnership opportunities…………..**