EEE Parts Strategies for SmallSat Missions

Neutron Star Interior Composition ExploreR
as an Example

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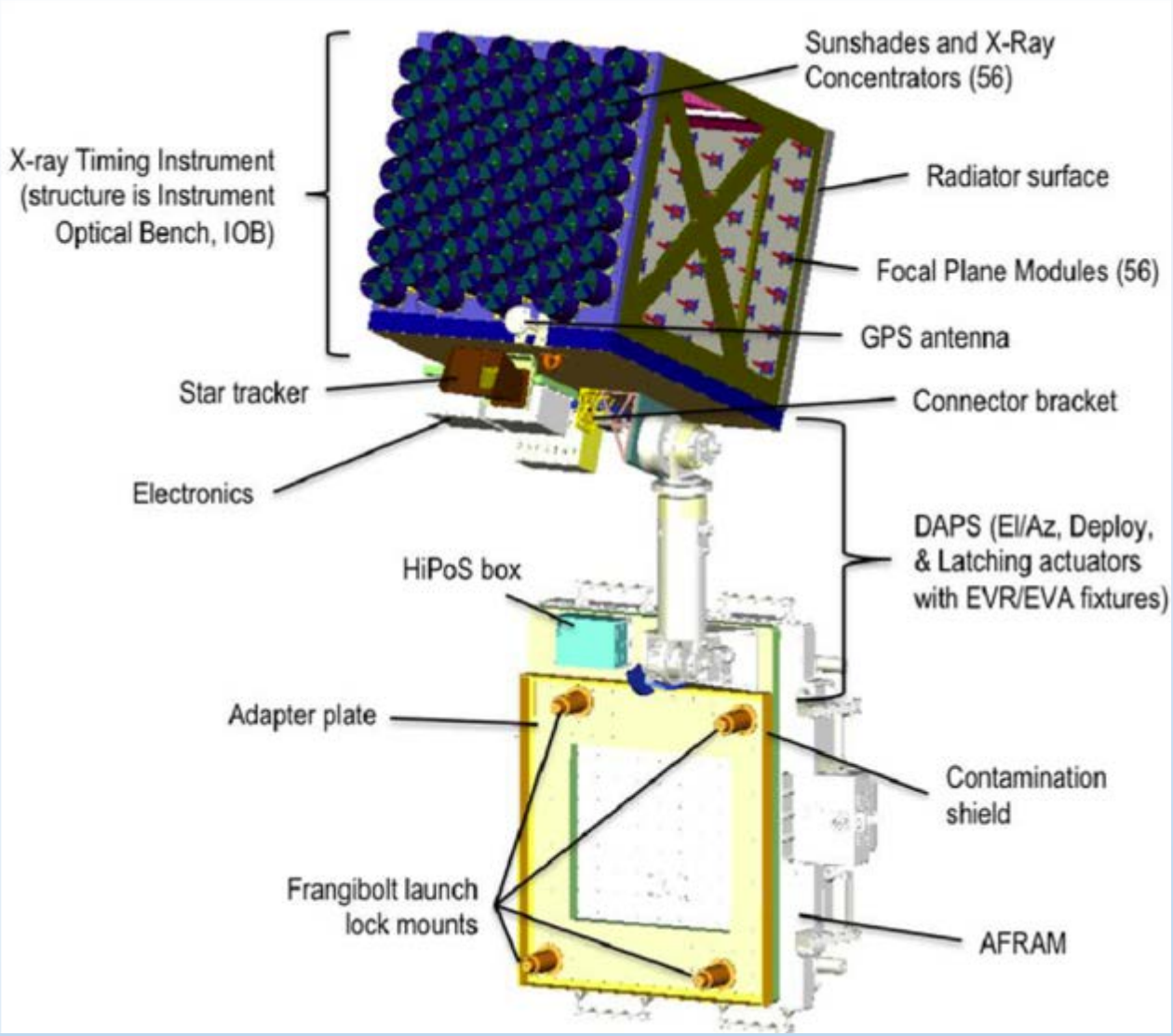
Acronyms

Acronym	Definition
COTS	Commercial Off The Shelf
DPA	Destructive Physical Analysis
ISS	International Space Station
LDC	Lot Date Code
MIL	Military
MIT	Massachusetts Institute of Technology
NICER	Neutron star Interior Composition ExploreR
SCD	Source Control Drawing
TEC	Thermo Electric Cooler

Neutron star Interior Composition ExploreR (NICER)

- Partnership with GSFC and MIT Kavli Institute
- X-ray timing and spectroscopy instrument mounted on International Space Station
- Class D mission – 18 months ISS orbit
  - **Relatively benign environment**
  - **Moderately short duration**
- Systems include Gimbal Control Electronics, Main Electronics Box, ISS Power Conversion, Star Tracker, Measurement Power Units, and Focal Plane Modules.
- Design (and mission proposal) based on successful prototype X-ray detector electronics. Array of X-ray Detection, 56 total detectors, 8x7 configuration
- Consolidated Parts Control Plan into the Mission Assurance Requirements, rather than separate document.
- Selected EEE-INST-002 Grade 3, lowest grade available, as baseline "requirement"

NICER System Architecture



Reliability Requirements: Do No Harm to ISS or Crew

- NICER was willing to take class D risks, except when it came to Safety- treated just as critical as any other ISS or manned mission.
- Systems were ranked in terms of criticality (specifically safety critical)
- **High Criticality** systems based on heritage designs, using Grade 2 parts
  - No cost savings to redesign with lower grade parts
  - Gimbal Control Electronics, Main Electronics Box, Deployment and Pointing System
- **Single String** Systems with **lower Fault Tolerance**, using Grade 2 parts
  - ISS Power Conversion, Star Tracker…
- **Fault Tolerant**, and **Lower Criticality** Systems taking advantage of COTS parts with minimal piece part screening
  - Detector electronics inherently fault tolerant featuring 56 detectors (minimum 35 needed to meet science objectives).
  - COTS parts enabled higher resolution/science objectives.

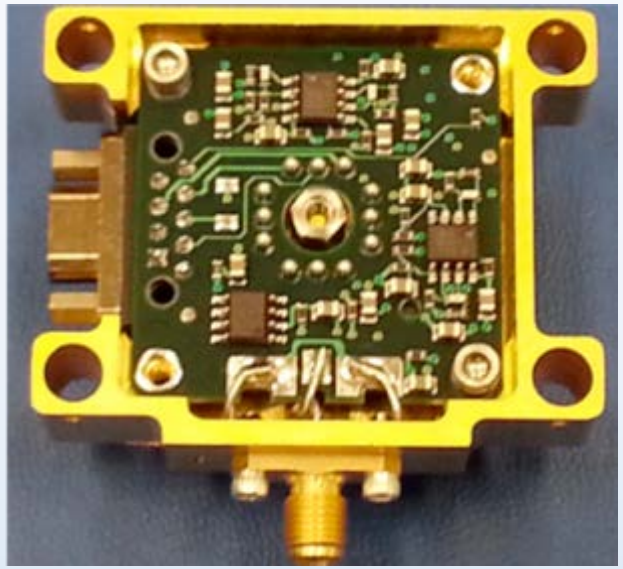
NEPP Guidance for SmallSat Parts

Criticality/Fault Tolerance

High	Level 1 or 2 suggested. COTS upscreening/ testing recommended. Fault tolerant designs for COTS.	Level 1 or 2, rad hard suggested. Full upscreening for COTS. Fault tolerant designs for COTS.	Level 1 or 2, rad hard recommended. Full upscreening for COTS. Fault tolerant designs for COTS.
Medium	COTS upscreening/ testing recommended. Fault-tolerance suggested	COTS upscreening/ testing recommended. Fault-tolerance recommended	Level 1 or 2, rad hard suggested. Full upscreening for COTS. Fault tolerant designs for COTS.
Low	COTS upscreening/ testing optional. Do no harm (to others)	COTS upscreening/ testing recommended. Fault-tolerance suggested. Do no harm (to others)	Rad hard suggested. COTS upscreening/ testing recommended. Fault tolerance recommended
	Low	Medium	High

Environment/Lifetime

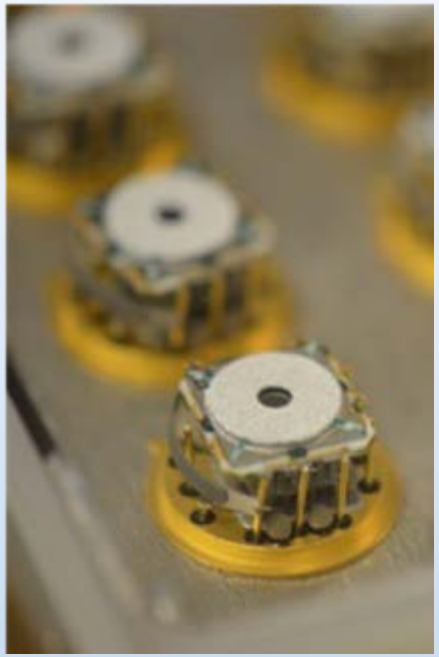
Detector Electronics



- Based on COTS parts
- Each Detector sits on a Preamp Board,
- 8 detectors/preamps controlled by 7 Measurement Power Units, including Analog and Digital Board
- Commercial/Custom X-ray Detector- Vacuum sealed, TEC cooled, Multi-planar construction Hybrid, sealed in micron thick “glass” window.
- Commercial obsolete Atmel Microprocessor- critical to the hardware, could not be designed out.
- Other COTS diodes, transistors, microcircuits, and passives.

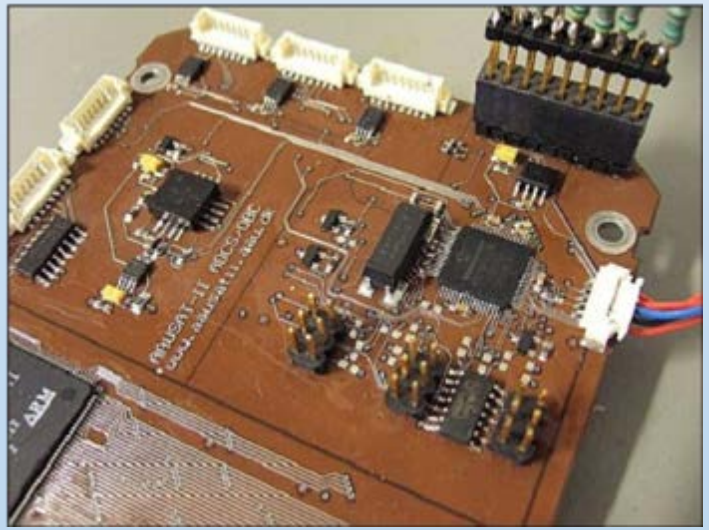
X-Ray Silicon Drift Detector Hybrids

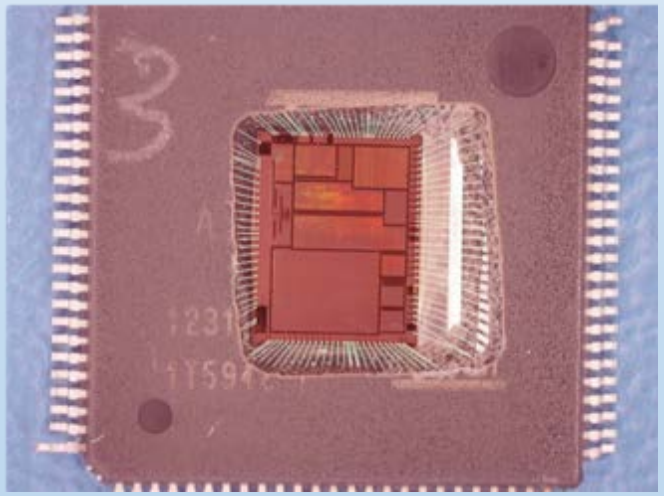
- Parts were customized with window and collimator dimensions specific for NICER mission.
- SCD for procurement, mostly electrical performance specs.
- Internal 2 stage TEC qualified to Telcordia GR-468
- Standard manufacturing processes, workmanship, and testing from manufacturer
- Performed precap inspection on our flight lot, mostly informational.
- Sample DPA on flight lot
- Performed Proton Radiation Characterization at Massachusetts General Hospital
- Fault Tolerant by system design- but common mode failures could impact science

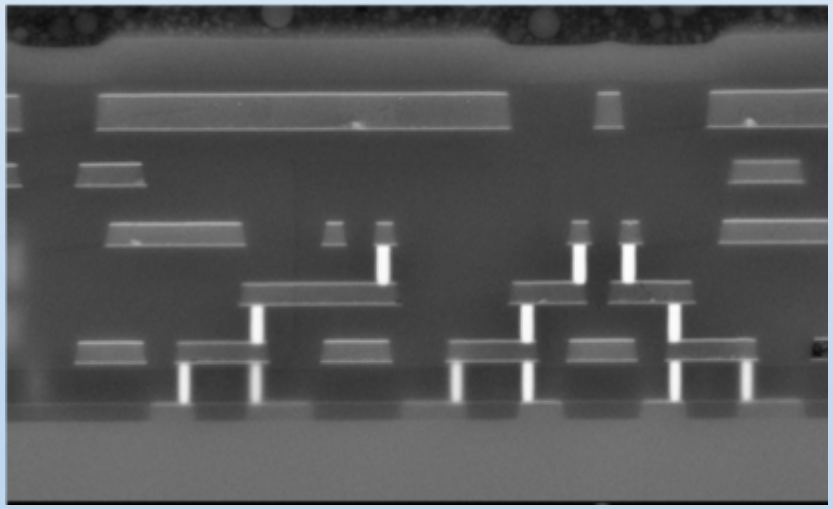


Atmel Microprocessor

- Had been recently obsoleted at the time- bought up large quantity of two LDCs remaining in authorized distributor inventory.
- Built-in unique features, 8 input channels, etc. which made it highly suited for the application (and difficult to design away from).
- Performed DPA- did identify pure tin leads (expected) and a clean looking planar device construction.
- Flight Heritage? Had flown on Danish Aalborg University AAUSAT-2 and AAUSAT-3, worked "successfully" in that radiation environment multiple years.







Remaining Detector Parts

- Tried proposing more traditional “flight” parts- very few were possible due to part package size constraints. Larger parts would necessitate fewer detectors/less fault tolerance.
- Were able to keep selected capacitor values within reasonable range (available flight equivalents).
- Attempted to use MIL “ish” capacitors and resistors when available (lead time). Ended with a mix of COTS and screened/MIL parts due to schedule constraints.
- Swapped out COTS micro-D connectors for more suitable MIL parts and plating finishes.
- Class H, rad “tolerant” DC/DC converters over COTS options.
- Board level testing campaign- accumulate at least 700 hours of operational time, and through environmental test campaign (cycle, vibe, etc) prior to launch
- Anecdote: we did uncover one capacitor short circuit failure during board level screening campaign- ended up being one of the MIL “ish” screened parts.

NICER Results

- Launched June 3, 2017, Completed 24+ month mission, still working today
- 95% of COTS detectors survived board level screening campaign
- NICER has produced 30 peer reviewed papers so far, a dozen in the review process right now… and many more to come…
- Principle Investigators: Keith C. Gendreau, Zaven Arzoumanian
- Project Manager: Sridhar Manthripragada
- Chief Safety and Mission Assurance Officer: Susie Pollard
- Radiation Effects Engineer: Megan Casey
- Links and References:
- https://www.nasa.gov/nicer
- https://heasarc.gsfc.nasa.gov/docs/nicer/index.html
- The Neutron star Interior Composition Explorer (NICER): Design and Development: Gendreau, K.C., Arzoumanian, Z. et al. 2016, Proc. SPIE 9905, Space Telescopes and Instrumentation 2016: Ultraviolet to Gamma Ray, 99051H (22 July 2016).
- http://amptek.com/products/fast-sdd-silicon-drift-detector/
- https://directory.eoportal.org/web/eoportal/satellite-missions/a/aausat-2

In-House SmallSat Architecture Development

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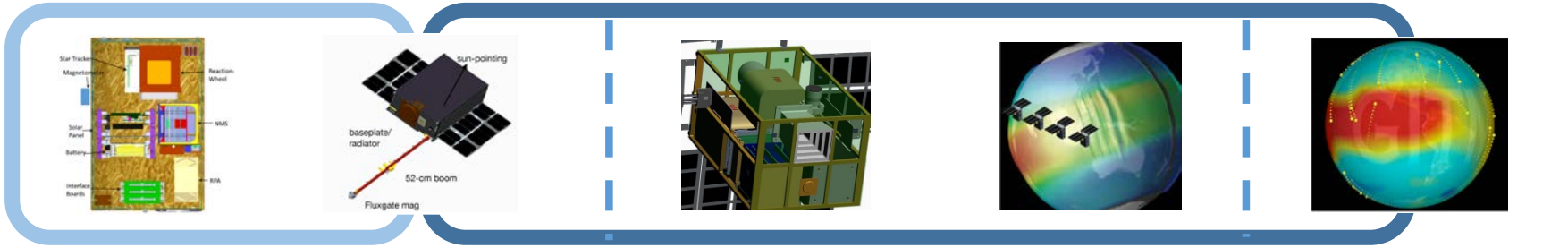
SmallSat Relevance to GSFC

Significantly more missions, even though small, provide unique opportunities

- Additional diversity to the directorate portfolio, inherently reducing risk and reliance on large missions
- Significant opportunities to train personnel across the full life-cycle due to decreased development schedules and increased number of missions
- Increased interaction frequency with and throughout the science community (including the underserved)
  - Establishing relationships early puts us on ground floor of next big science idea/mission



6U LEO | 6U ↑Rel ↑Rad | 12U+ Planetary | Constellations | 25-100 Armada

Increased mission complexity

GSFC poised to innovate SmallSat solutions

SmallSat Mission Challenges	
Radiation	Surviving and performing in high radiation environments
Lifetime	Surviving long duration cruises
Ride opportunities	Achieving higher reliability because the fly-learn-refly philosophy doesn't hold
Power	Generating solar power beyond 1 AU Increasing capability for telecom and propulsion
Thermal	Dissipating increased power from subsystems, inside 1AU, or near high albedo planetary bodies
Telecom	Closing direct to earth links over large distances Crosslinking to relay mothership
GN&C	Tracking and navigating outside GPS desaturating wheels
Propulsion	Increasing delta-V for orbit insertions and exploration

- Enable challenging and harsh environment mission architectures being proposed by our scientists, especially planetary missions
- Tailor balancing/scaling of programmatic and technical risks for Class-D missions
- Reduce SWaP while increasing flexibility and robustness by integrating electronics and software for core subsystems

Alternative Concepts

- Big mission thinking and point designs lead to high cost
- Out of house bus solutions
  - Adequate for simple LEO
  - Gaining momentum but do not currently meet all needs
  - Does not provide additional benefits including employee development and skills, technology infusion, and flexibility

Common spacecraft architecture reduces non-recurring engineering providing a cost efficient solution to meet the demanding SmallSat science mission being proposed now and in the near future.

Goddard Modular SmallSat Architecture (GMSA)

- The Goddard Modular *SmallSat* Architecture (GMSA) was the initial in-house initiative that addressed the need for developing high reliability SmallSat technology within a *minimum* 6U SmallSat volume.

- The purpose of GMSA is to have a spacecraft architecture that can enable high reliable, long duration SmallSat missions that operate in harsh radiation environments.

- GMSA can accommodate spacecraft subsystems developed both within NASA and outside of NASA

- The initial GMSA hardware development involved the design and assembly of multiple board assemblies that implements the Command and Data Handling (C&DH) subsystem the Power System Electronics (PSE) subsystem functionality within the satellite.

C&DH Primary Functions

- C&DH hardware consists of the following two boards:
  - SmallSat Common Electronics Board (SCEB)
  - Adapter Board

- GMSA C&DH supports the following features:
  - TID > 20 krad
  - SEL immune
  - 2 years mission including activation and checkout (does not include storage)
  - Predominant use of flight qualified parts for higher reliability.

C&DH Interfaces

- Multiple I/O options
  - 4 RS-422 drivers and 4 RS-422 receivers
    - Interface for up to 4 additional RS-422 drivers and 4 RS-422 receivers populated on the Adapter Board
  - Interface for 4 LVDS drivers and 4 LVDS receivers populated on the Adapter Board
  - 1 dedicated CAN bus interface
  - 2 dedicated spacecraft SPI interfaces each with 2 slave select signals
  - 2 dedicated spacecraft I2C interfaces
  - 1 dedicated I2C interface to the PSE
  - 1 dedicated I2C interface to the SCEB Adapter Board for controlling multiple multiplexers and 16 general purpose inputs / outputs (GPIO)
  - 4 inputs from the SCEB Adapter Board that are +5V tolerant
  - ADC I/Os
  - Driver signals for 3 H-bridge drivers on the SCEB Adapter Board

C&DH General Information

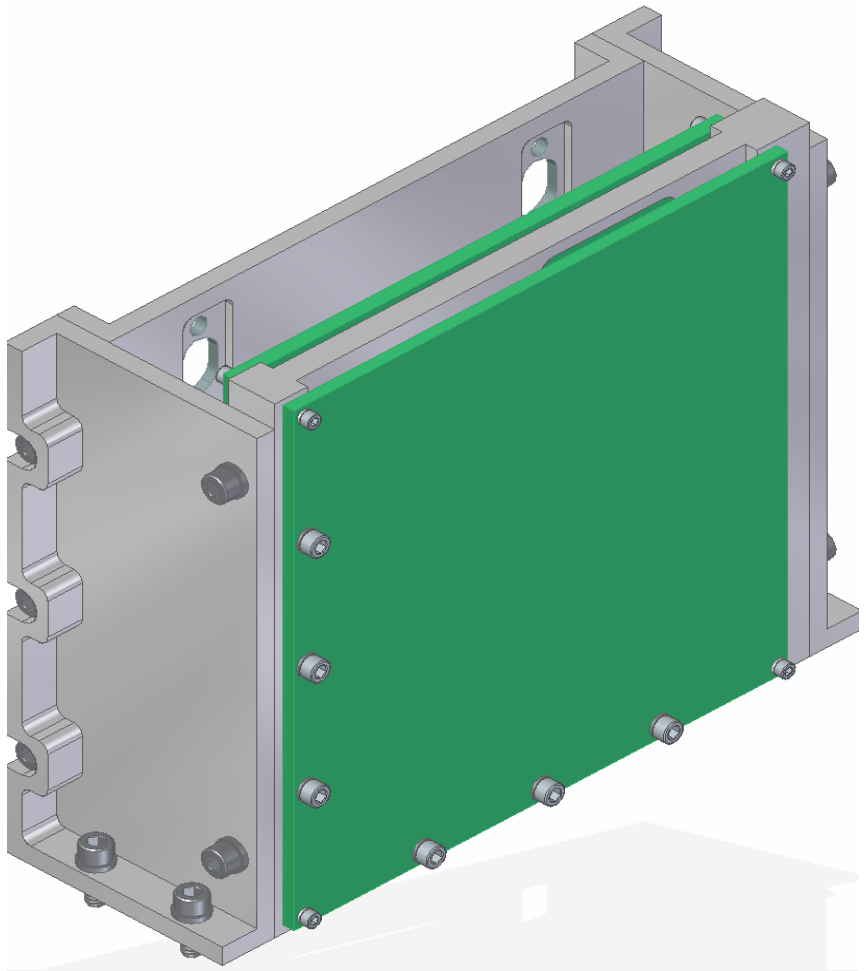
- **Target C&DH Assembly Power Consumption: < 3 Watts**

- **C&DH Total Mass = 419.86 g**
  - SCEB (Processor Board): 135 g
  - Adapter Board: 258.55 g
  - C&DH Assembly Hardware: 26.31 grams

- **Temperature Ranges:**
  - C&DH survival temperature range: -40C to +65C
  - C&DH operating temperature range: -20C to +50C

- **Individual Board Dimensions: 90 mm x 90 mm**

- **C&DH Assembly Dimensions: 116.56 mm x 44.35 mm x 92.51 mm (LxWxH)**



COTS Parts Selection

- Mosfets used to implement 3 H-bridge drivers had to be COTS parts because of limited board area for placement of these parts.

- Completed TID and SEE testing on both mosfets used:
  - N-channel Mosfet: ON Semiconductor BSS123
  - P-channel Mosfet : Vishay Siliconix SI1013

- TID testing was completed at NASA Goddard Space Flight Center by Rebekah Austin

- SEE testing was completed at Lawrence Berkeley National Laboratory by Michael Campola and Jean-Marie Lauenstein

COTS Parts Selection

- TID test results showed the following:
  - Changes in the supply current were not seen till 50 krad(Si) and this was a slight increase in the drain and ground voltages.
  - At 100 krad(Si), the average supply current also started to increase.
  - The output load current did not change noticeably over dose.
  - The circuits also exhibited little part to part variability.

- SEE test results showed the following:
  - All of the BS123 NFET devices failed at 1039 MeV Ag. These failures were observed between 25 and 50 Vds with Vgs at 0V.
  - All Si1013 PFET devices passed at 1039 MeV Ag with a maximum Vds of 20 V and Vgs at 6 V.

- Test results were satisfactory based on the design implementation

Continuing Work

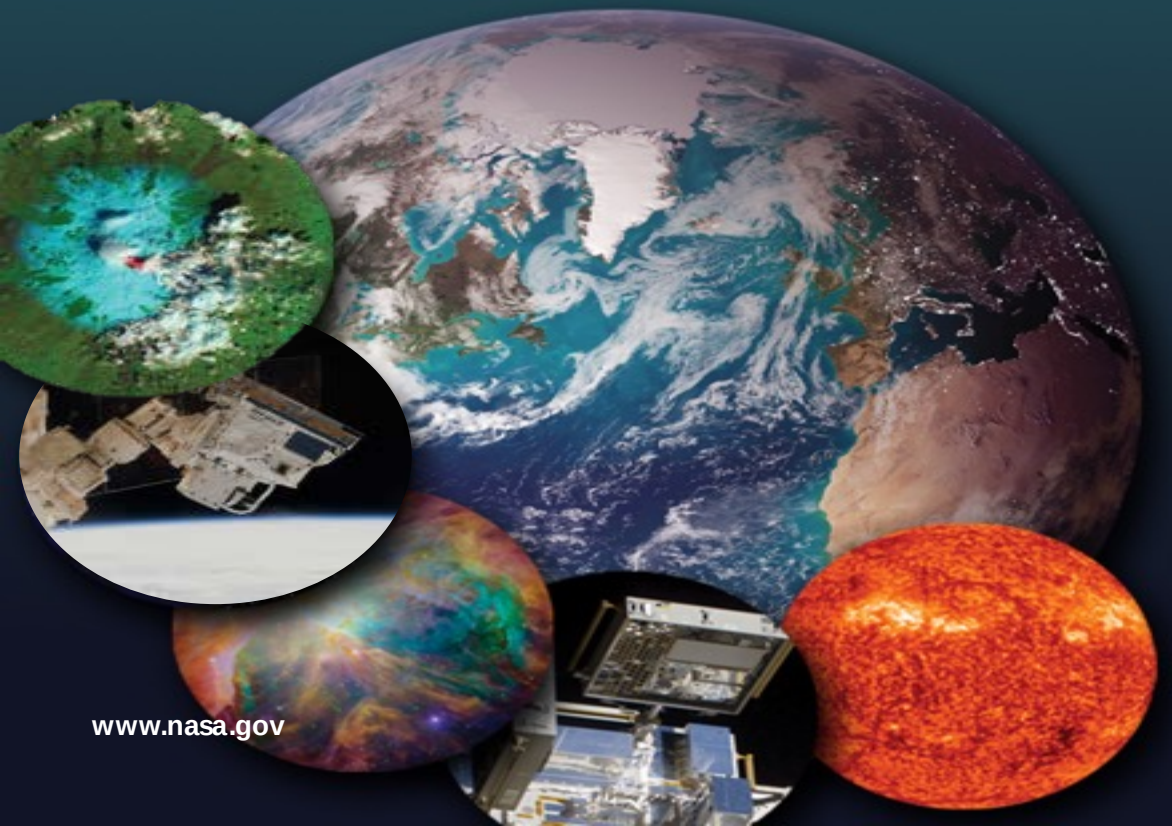
- The GMSA experience laid the foundation for bridging into the DellingrX architecture

- The lessons learned from the GMSA hardware development effort along with in-flight experience on multiple in-house SmallSat missions over the past few years have been very beneficial to the formulation of the DellingrX architecture

National Aeronautics and Space Administration

SpaceCube v3.0 Mini

NASA Next-Generation Data-Processing System for Advanced CubeSat Applications



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NASA Electronic Parts and Packaging (NEPP) Program
2019 Electronics Technology Workshop

June 2019

SpaceCube

www.nasa.gov

Acronyms

Acronym	Definition
BL-TMR	BYU-LANL TMR
cFE	Core Flight Executive
cFS	Core Flight System
CPU	Central Processing Unit
CSP	CHREC/CubeSat Space Processor
DSP	Digital Signal Processor
FF	Flip-Flop
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
ISA	Instruction Set Architecture
LEO	low-Earth Orbit
MGT	Multi-Gigabit Transceiver
PCB	Printed Circuit Board
RE	Recuring Engineering
SBC	Single-Board Computer
SEL	Single-Event Latchup
SEM	Soft Error Mitigation
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy

Outline

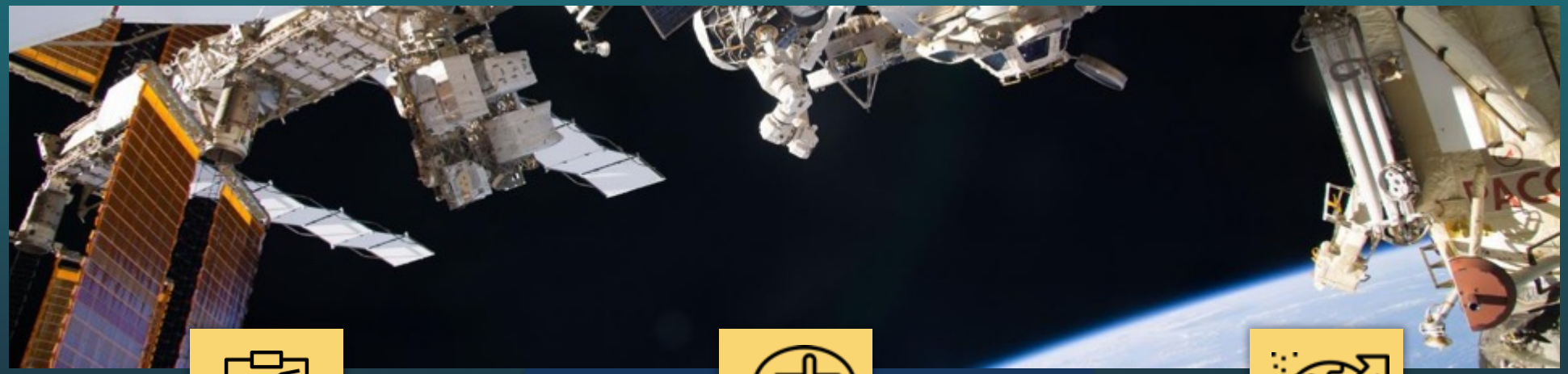
1. Introduction

2. SpaceCube Overview
   - SpaceCube Introduction
   - SpaceCube Approach
   - Mini Design Philosophy
   - Lessons Learned

3. SmallSat / CubeSats for Space
   - SmallSat/CubeSat Challenge
   - Xilinx Space-grade Devices
   - Kintex UltraScale
   - Soft-Core Processors

4. SpaceCube v3.0 Mini
   - Configuration Schemes
   - Fault-Tolerant Operation
   - Specification

Goals, Motivations, Challenges



Goals

Develop reliable, high-speed hybrid processor using **SpaceCube design approach** to enable next-generation instrument and CubeSat capability

Motivations

Many commercial CubeSat processor offerings primarily target benign LEO orbits and **do not strongly address** radiation concerns and parts qualification

Need exceptional capability to support complex applications such as artificial intelligence

Challenges

Managing PCB area restrictions for rad-hard components, balancing cost, educating mission designers for key reliability differences

SpaceCube Introduction

What is SpaceCube?

A family of NASA developed space processors that established a **hybrid-processing approach** combining radiation-hardened and commercial components while emphasizing a novel architecture **harmonizing** the best capabilities of CPUs, DSPs, and FPGAs

High performance reconfigurable science / mission data processor based on Xilinx FPGAs

- Hybrid processing …
  CPU, DSP, and FPGA logic
- Integrated "radiation upset mitigation" techniques
- SpaceCube "core software" infrastructure (cFE/cFS and "SpaceCube Linux" with Xenomai)
- Small "critical function" manager/watchdog
- Standard high-speed (multi-Gbps) interfaces

SpaceCube is Hybrid Processing…

SpaceCube Heritage

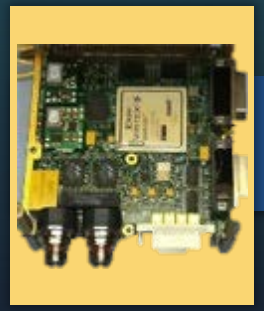
Closing the gap with commercial processors while retaining reliability

- **57+ Xilinx device-years on orbit**
- **26 Xilinx FPGAs in space to date (2019)**
- **11 systems in space to date (2019)**

SpaceCube is Mission Enabling…

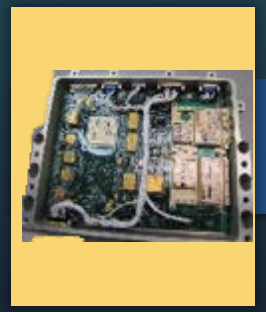
SpaceCube v1.0

STS-125, MISSE-7, STP-H4, STP-H5, STP-H6



SpaceCube v1.5

SMART (ORS)

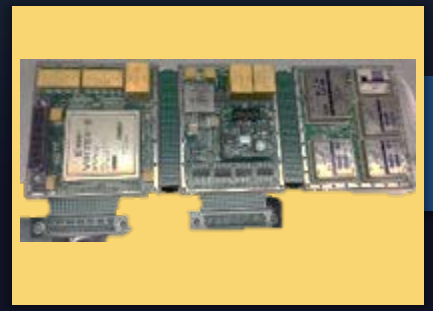


SpaceCube v2.0-EM

STP-H4, STP-H5

SpaceCube v2.0-FLT

RRM3, STP-H6 (NavCube)



SpaceCube v2.0 Mini

STP-H5, UVSC-GEO

SpaceCube Approach

01

The traditional path of developing radiation-hardened flight processor **will not work** … they are always one or two generations behind

02

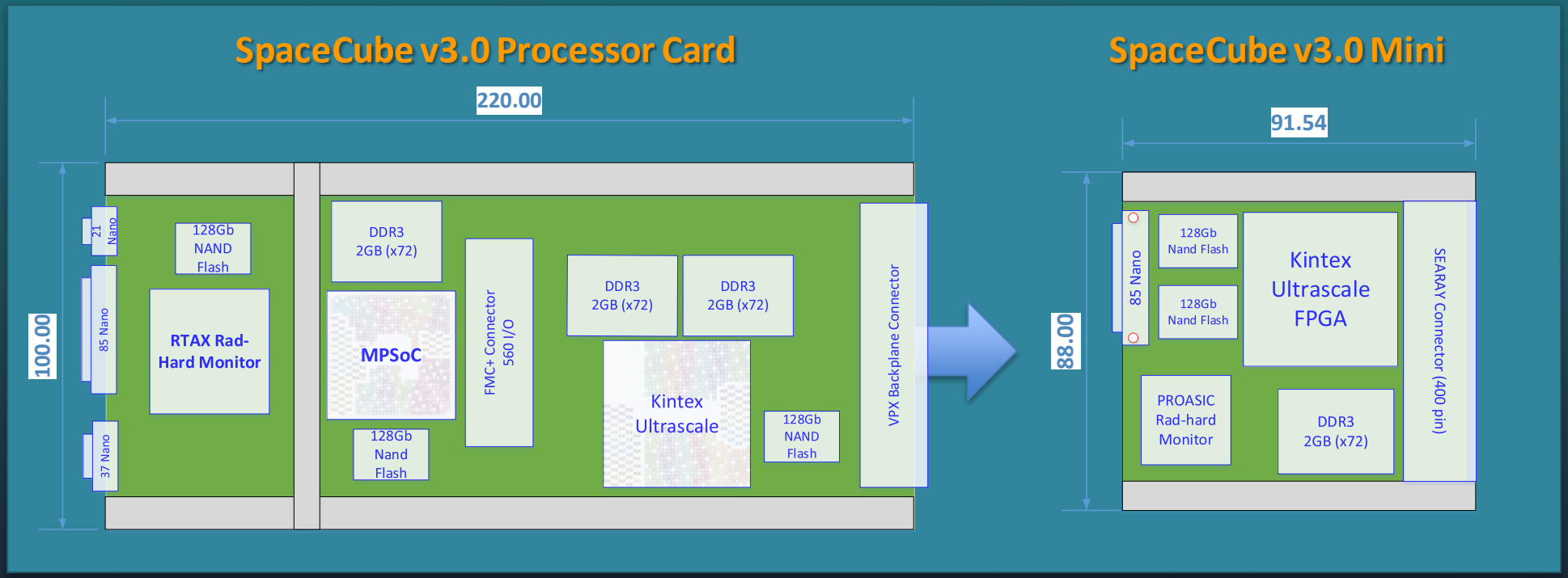
Use latest radiation-tolerant* processing elements to achieve massive **improvement** in "MIPS/watt" (for same size/weight/power)

03

Accept that radiation induced upsets may happen occasionally and just deal with them appropriately … any level of reliability can be achieved via **smart system design!**

***Radiation tolerant – susceptible to radiation induced upsets (bit flips) but not radiation-induced destructive failures (latch-up)**

Mini Design Philosophy



Same Approach, Smaller Size

SpaceCube design approach applied to smaller form-factor

Key Design Reused

Much of UltraScale design and interface remain same between cards including DDR Pinout

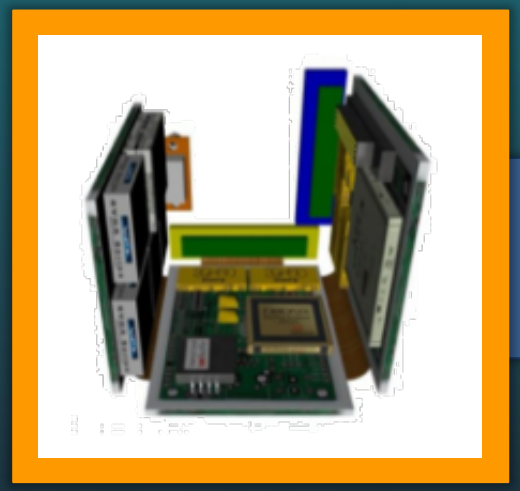
Supervision Requested

Radiation-hardened monitor architecture and code reusable

Trade in, Trade Out

EEE parts trades, analysis, and circuits extensively leveraged from main card design

Mini Form Factor Lessons Learned



SpaceCube Mini v2.0
Lessons Learned

CSPv1
Lessons Learned

Manufacturability

Difficult to manufacture due to rigid-flex and laser-drilled microvias. Tied to single vendor design.

Monitor Design

Aeroflex rad-hard monitor was effective, however, limited by FPGA resources preventing more robust design

CubeSat Connector

Samtec SEARAY connector provided flexibility and performance, same connector used with SpaceVNX (VITA 74.4)

Backplane Advantage

Backplane allows swapping of individual card as advances/ improvements are made and can easily incorporate new components

SmallSat/CubeSat Processor Challenge

Massively Expanding Commercial Market for SBCs

- Tons of commercial vendors in CubeSat Market (e.g. Pumpkin, Tyvak, GomSpace, ISIS, Clyde Space, etc…)

Mission Developers Seeking Commercial Hardware

- Under pressure from cost-cap missions, and reducing costs in general
- Reduced RE for constellation mission concepts
- Attractive all-commercial solutions provided integrating several CubeSat "Kit" types of cards

"2019 Nano/Microsatellite Forecast, 9th Edition," SpaceWorks Enterprises, Inc., Jan 2019.

Not Designed With Harsh Orbit Considerations Beyond LEO

- Many vendors have performed limited radiation testing and largely support missions in more benign LEO orbits
- Mission is radiation test approach
- Little-to-no additional radiation testing or parts qualification
- No recommendations for fault-tolerant configurations of offered SBCs

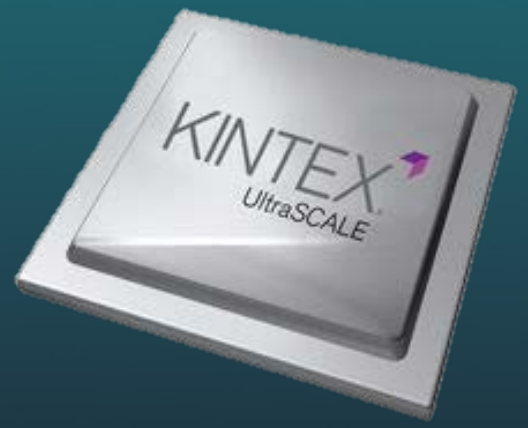
Xilinx Space Devices Compared

	SpaceCube v1.0		SpaceCube v2.0	SpaceCube v3.0	
	XQR4V (RT, 1.2V)		XQR5V (RHBD, 1.0V)	XQRKU060 (RT, 1.01V)	KU060 vs. V5
Resource	FX60	FX140	FX130	KU060	
Logic Cells	56,880	142,128	131,072	726,000	5.54x
CLB FF	50,560	126,336	81,920	663,360	8.10x
Max Distributed RAM (Kb)	395	987	1,580	9,180	5.81x
Total Block RAM (Kb)	4,176	9,936	10,728	38 Mb	3.54x
BRAM/FIFO ECC (36 Kb)	--------	--------	--------	1,080	N/A
DSP Slices	128	192	320	2,760	8.63x
MGT			18 @ 4.25 Gbps	32 @ 12.5 Gbps	5.23x
TID (krad)	300	300	1,000	120	(0.12)
SEL	>125	>125	>125	~80	(0.64)
Flow	V-Flow (QML-V)		B-Flow (QML-Q) V-Flow (QML-V)	B-Flow (QML-Q) Y-Flow (QML-Y Compilant)	N/A
Package	35 x 35 mm	40 x 40 mm	45 x 45 mm	40 x 40 mm	(0.78)

"Xilinx's Adaptive FPGAs for Space Applications" White Paper

Xilinx Kintex UltraScale XQRKU060

- First 20 nm FPGA for Space
  - Designed for SEU mitigation (>40 patents)
  - Deploys same commercial silicon mask set
  - Uses Vivado UltraFast Development



- Ruggedized 1509 CCGA
  - 40 mm x 40mm package
  - Footprint compatible A1517

- Product Space Test Flows
  - B-Flow (QML-Q Equiv.) and Y-Flow (QML-Y Compliant)

Lee, D., Allen, G., Swift, G., Cannon, M., Wirthlin, M., George, J. S., Koga, R., and K. Huey, "Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation," IEEE Radiation Effects Data Workshop, July 13-17, 2015.

- Commercial Radiation Testing Results
  - Improved Xsect compared to 7 series
  - No observed classical SEL signatures

Berg, M., Kim, H., Phan, A., Seidleck, C., Label, K., and M. Campola, "Xilinx Kintex-UltraScale Field Programmable Gate Array Single Event Effects (SEE) Heavy-ion Test Report," NASA Electronic Parts and Packaging, 2017.

Fault-Tolerant Soft-Core Processing

Xilinx TMR MicroBlaze[1]

- Built-in Xilinx TMR solution for newer FPGAs
- Includes TMR SEM IP Core
- Vivado IP integrator for easy project creation

BL-TMR MicroBlaze[2]

- BYU-LANL TMR Tool (BL-TMR) provides automated TMR application
- Fault Injection on MicroBlaze performed for SpaceCube v2.0

BL-TMR RISC-V[3]

- RISC-V is a promising new ISA processor gaining popularity for Intel and Xilinx FPGAs
- Neutron radiation test of Taiga RISC-V
- 27% decrease in operational frequency, for 33x improvement in cross section

Resource Utilization of TMR Designs on KU040

Resource	MicroBlaze Stand Alone	Xilinx TMR MicroBlaze	BL-TMR MicroBlaze	BL-TMR RISC-V[3]
LUTs	3.29%	9.81%	15.58%	0.80 %
CLB FF	1.63%	4.77%	4.89%	0.20 %
BRAM/FIFO ECC (36 Kb)	12.50%	37.50%	37.50%	1.00 %
DSP Slices	0.31%	0.94%	0.94%	0.20 %
FMax	-----	0.95x	0.88x	0.73x

BL-TMR v6.3, MicroBlaze v11, 32-bit 5-stage, FPU, 32 Kb I/D, Vivado 2019.1,

[1]Microblaze Triple Modular Redundancy (TMR) Subsystem v1.0, https://www:xilinx:com/support/documentation/ip documentation/tmr/v1 0/pg268-tmr:pdf, Xilinx, 10 2018.

[2]http://reliability.ee.byu.edu/edif/

[3]A. Wilson and M. Wirthlin, "Neutron Radiation Testing of Fault Tolerant RISC-V Soft Processors on Xilinx SRAM-based FPGAs," 12th Space Computing Conference, July 30 – August 1, 2019.

SCv3.0 Mini Booting Configuration

Selectable Configuration

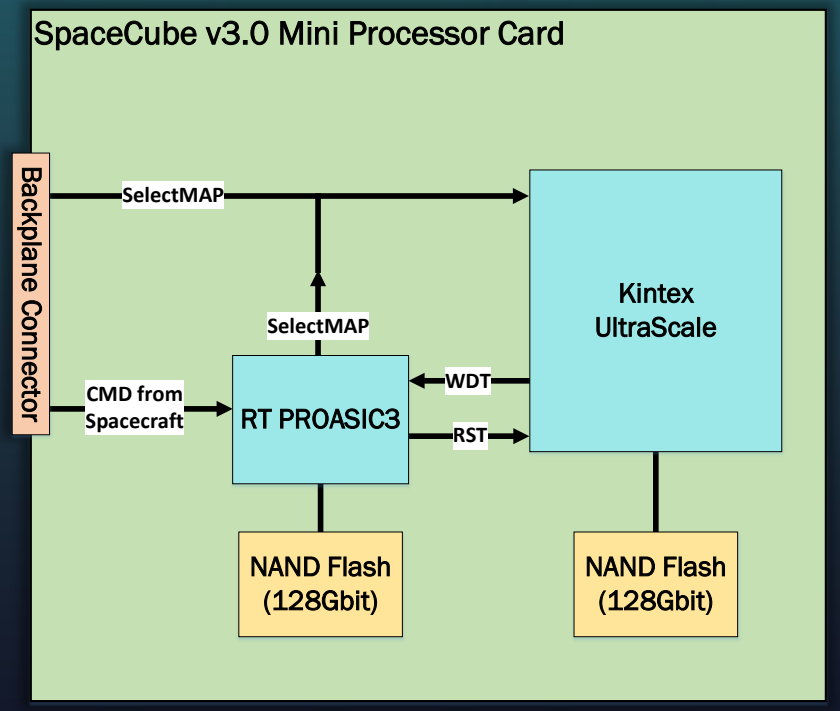
- Kintex configured via SelectMAP from backplane or on-board RTProASIC3 supervisor
- Dozens of configuration files stored with redundant copies across multiple internal dies

Robust RTProASIC Monitor

- Verifies configuration files are valid via page-level CRC checks
- Can reconstruct valid configuration file from several corrupted ones
- Internal FSM ensures Kintex programming and boot sequence is completed correctly
- Automatic program retry

Flexible Configuration

- Can be reconfigured via command from spacecraft to ProASIC
- Can change configurations in-flight to support dynamic mission requirements



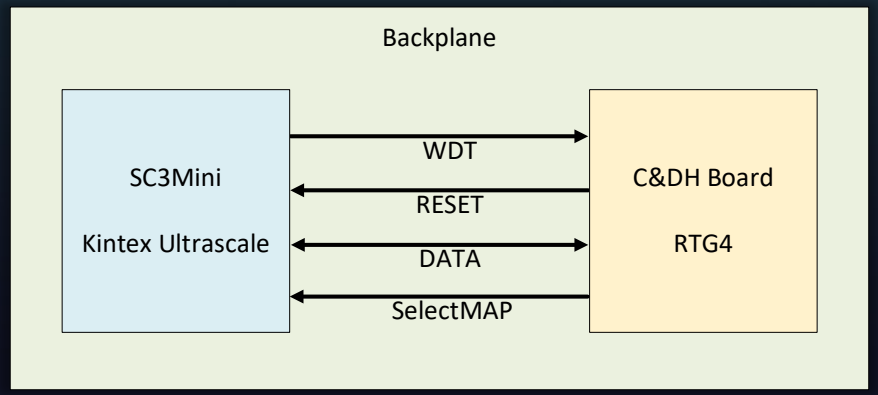
SCv3.0 Mini Fault-Tolerant Architecture

Stand-Alone Operation (RT-ProASIC)

- Scrubs Kintex configuration during operation via either:
  - Blind scrubbing (consistent time interval)
  - Smart scrubbing (readback scrubbing to check configuration and correct errors as they are detected)
- Scrubs configuration files in NAND flash memory

Companion-Card Operation (GSFC CubeSat Bus)

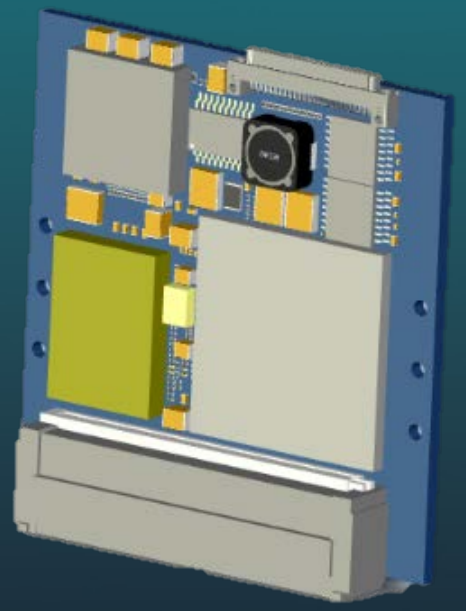
- Combines reliability of RTG4 with high performance of SCv3Mini to form flexible, reusable SmallSat/CubeSat bus
- RTG4 configures and monitors Mini over the backplane



SCv3.0 Mini High-Level Specifications

Overview

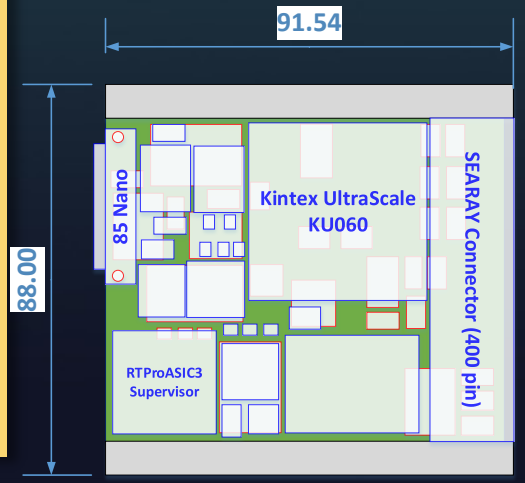
- Apply **SpaceCube design approach** to provide next-generation processor in **CubeSat form-factor**
- Maintain compatibility with SpaceCube v3.0
- High-performance processor of Goddard's modular CubeSat spacecraft bus Dellingr-X

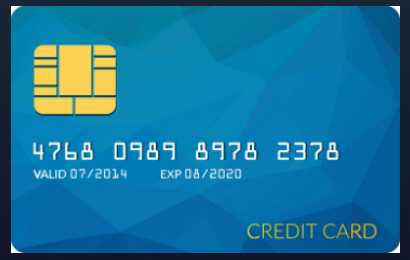


High-Level Specifications

1x Xilinx Kintex UltraScale

- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 30x 3.3V GPIO
  - 2 RS-422/LVDS
  - SelectMAP Interface
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG





Conclusions

SpaceCube is a MISSION ENABLING technology

- Delivers exceptional on-board computing power
- Cross-cutting (Earth/Space/Planetary/Exploration)
- Being reconfigurable equals BIG SAVINGS
- SpaceCube can be used in all mission applications
  … up to and including Class A
- Past research / missions have proven viability
- Ready for infusion into operational missions
- Next-Generation CubeSat design for artificial intelligence and machine learning applications

Thank you! Questions?

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Special thanks to our sponsors: NASA/GSFC IR&D, NASA Satellite Servicing Programs Division (SSPD), NASA Earth Science Technology Office (ESTO), DoD Space Test Program (STP), DoD Operationally Responsive Space (ORS)

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