National Aeronautics and Space Administration



Electronic Parts and Electrostatic Discharge Gaps and Mitigation Strategies Updates (FY 2020)

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NASA's Mars Helicopter, a small, autonomous rotorcraft, will travel with the agency's Mars 2020 rover, currently scheduled to launch in July 2020, to demonstrate the viability and potential of heavier-than-air vehicles on the Red Planet.

Credits: NASA/JPL-Caltech

Why Electronic Parts and ESD Need a Fresher Look – Gaps

- NASA has been supporting Defense Logistics Agency (DLA) audits of the supply chain.
- During the audits, it was observed that the MIL-PRF-38535 requirements were practically nonexistent regarding ESD aspects of electronic parts.
- Microcircuit pin count has increased significantly (e.g., Vertex FPGAs have 1752 columns). Manufacturers are striving for still higher counts.
- Current qualification standards were developed years ago with pin counts in the twenties.
- Applying these old device testing standards to modern high-pin count products can cause severe problems (e.g., testing times increase dramatically).
- Furthermore, microcircuit part production is no longer under one roof, but landscape of supply chain is multiple specialty houses (see next slide).

A Changing Landscape (Shipping/Handling/ESD Challenge)

A New Trend – Supply Chain Management Ensuring gap-free alignment for each qualified product (All entities in the supply chain must be certified/approved)

Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

More Stops — More Places with ESD Risk

Electronic Parts and Electrostatic Discharge (ESD) – Gaps and Mitigation Strategies

- Gaps have evolved because of new technology and inconsistencies of standards development (e.g., three zaps vs. one zap per pin for testing). Parts have continued shrinking to smaller sizes & growing in complexity. Consequently, they are more susceptible to ESD and require more testing effort.
- Costs cannot be ignored—per unit price for advanced devices is approaching \$200K. ESD mitigation costs are minute compared to the device unit costs.
- Mitigation strategies include ESD surveys, observations during audits, standards updates (including harmonization of standards), & outreach to the military & space communities.
- There is always a latency risk from ESD.

The cost information contained in this document is of a budgetary and planning nature and is intended for informational purposes only. It does not constitute a commitment on the part of JPL and/or Caltech.

NASA Electronic Parts and ESD FY20

Activities

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- Continue NASA ESD Surveys of Supply Chain (Deliverables: SAS Reports) Doe, Nelson, others
 - Align with DLA audits
 - DLA Product Test Center (DLA's request)
 - JPLASIC and PWM supply chains
 - GaN supplier(s) of interest to NASA (new technology)
 - ✤ TopLine
 - Recent findings
 - Ionizer generated +2000V spikes when tested.
- ESD Test Data (Deliverable: Test Report) Kim, Han
 - Limited resources
 - ✤ HBM per 883/3015 vs JEDEC 001
 - CDM per JEDEC 002
 - ✤ MM
- o ESD Program Implementation Doe
 - Review ESD test data and issue internal guidelines
- o Mil Standards Update (Deliverables: Inputs to DLA. Complete) Agarwal
 - Shri and Paul Nixon to clarify the language in MIL-PRF-38535 (Done, sent to DLA)
 - Shri to provide paragraph on wafer foundries (Done, see previous slide)
- o Continue to support JC-13 Task Group (Deliverable: Technical Talk by ON Semi) Ovee, Agarwal
 - Present at meetings
 - Facilitate Technical Talk on ESD by ON Semi (Done)
- Guidelines document (Deliverable: Document) Han
 - Combine the bulletins and any new work
- \circ $\;$ Questions from Designers Taylor $\;$
 - Mostly related to overshoot/undershoot, undefined parameters in SMDs

DLA Specific Activities

ESD Changes Summary (Already Implemented by DLA)

• Ref: 38535 Revision L, Dated December 6, 2018

- Para 2.3. Updated HBM, added CDM
- o Para 3.2.1. Added S20.20 as an alternate
- Para 3.12. Updated program control requirements
- Para 3.6.7.2. Updated sensitivity identifiers for HBM, added CDM
- Para 4.2.3. Updated ESD requirements
- o Para A.3.4.1.4. Updated references
- Para A.3.6.9.2. Updated test requirements
- o Para 4.4.2.8. HBM update
- Table H-IIA. Updated HBM reference
- Table H-IIB. Updated HBM reference

Updated MIL-STD-883, Test Method 1014

 Added Para 2.2.1d. "ESD Protective Tubes shall be utilized to ensure the system is ESD safe..."

• Added requirement in 38535K for post column attach electricals

To catch handling/ESD related problems

DLA Specific Activities (Cont'd) ESD Changes Summary (Submitted to DLA)

MIL-PRF-38535 updates for ESD wording:

◦ Current Rev:

4.2.3 Electrostatic discharge (ESD) sensitivity. ESD sensitivity testing shall be performed in accordance with TM 3015 of MIL-STD-883 and the device specification. The testing procedure defined within ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) may be used as an option in lieu of TM 3015 for applicable devices (e.g. high pin count devices wherein parasitic charge may effect ESD failures). However, manufacturers shall document such ESD testing procedure in the QM plan that require QA approval. The reported ESD sensitivity classification levels shall be documented in the device specification (see 3.6.7.2). In addition, unless otherwise specified, Human Body Model (HBM) and Charge Device Model (CDM) tests shall be performed for initial qualification and product redesign as applicable. If manufacturer is using the HBM or CDM or both method for ESD classification, it shall be reported in the device specification or standard microcircuit drawing (SMD) devices certificate of compliance (CofC).

DLA Specific Activities (Cont'd)

• Proposed clean re-wording:

4.2.3 <u>Electrostatic discharge (ESD) sensitivity</u>. ESD sensitivity testing shall be performed in accordance with TM 3015 of MIL-STD-883 and the device specification. The testing procedure defined within ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM)-may be used as an alternate in lieu of TM 3015. Testing for Charge Device Model (CDM) sensitivity shall be performed in accordance with ANSI/ESDA/JEDEC JS-002. Human Body Model (HBM) and Charge Device Model (CDM) tests shall be performed for initial qualification and product redesign as applicable. The reported ESD sensitivity classification levels shall be documented in the device specification (see 3.6.7.2). The manufacturer shall report the test method(s) used for ESD sensitivity classification in the device specification or standard microcircuit drawing (SMD) devices certificate of compliance (CofC).

• Proposed update to ESD definition to define HBM and CDM:

 6.4.18 <u>Electrostatic discharge (ESD) sensitivity</u>. ESD sensitivity is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESD classification testing and is used as the basis for assigning an ESD classification for the Human Body Model (HBM) or the Charged Device Model (CDM).

DLA Specific Activities (Cont'd)

- Human Body Model (HBM): One of the most common causes of electrostatic damage is the direct transfer of electrostatic charge through a significant series resistor from the human body or from a charged material to the electrostatic discharge sensitive (ESDS) device. The Human Body Model is the oldest and most commonly used model for classifying device sensitivity to ESD. The HBM testing model represents the discharge from the fingertip of a standing individual delivered to the device. It is modeled by a 100 pF capacitor discharged through a switching component and a 1.5 kohms series resistor into the component. Testing for HBM sensitivity is defined within MIL-STD-883 Method 3015 and within ANSI/ESDA-JEDEC JS-001.
- Charged Device Model (CDM): The transfer of charge from an ESDS device to a conductive material is also an ESD event. A device may become charged, for example, from sliding down the feeder in an automated assembler. If it then contacts the insertion head or another conductive surface, which is at a lower potential, a rapid discharge may occur from the device to the metal object. This event is known as the Charged Device Model (CDM) event and can be more destructive than the HBM for some devices. Although the duration of the discharge is very short (often less than one nanosecond), the peak current can reach several tens of amperes. The device testing standard for CDM is ANSI/ESDA JS-002. The test procedure involves placing the device on a field plate with its leads pointing up, then charging it and discharging the device.

Note: need to fix typo in section 6.8

• List of acronyms has "HAST" listed for "Human body model" – it should be "HBM".

DLA Specific Activities (Cont'd)

• ESD Changes (Submitted)

- Suggested solution: Replace "Devices" with "Wafers/Dice/Devices" such as in Para A.4.4.2.8:
- A.4.4.2.8 Electrostatic discharge (ESD) sensitivity.

......Wafers/dice/devices shall be handled in accordance with the manufacturer's in-house control documentation, which shall be maintained by the manufacturer......



Human Body Model (HBM) 883 vs JEDEC Test Methods

- Per MIL-PRF-38535, they are equivalent.
- 883 requires 3 zaps per pin, JEDEC 1 zap per pin. No data showing equivalency. NASA did limited testing.

Initial Results of ESD Testing

- Tests performed on
 - Parts from same manufacturer
 - Same function
 - Same lot
 - Testing done in increments of 250V
- o Test Results
 - Human Body Model (HBM) per MIL-STD-883
 - 3 units tested
 - All 3 failed at 250V
 - Human Body Model (NBM) per JEDEC standard
 - 3 units tested
 - 2 units failed at 250V
 - 1 unit failed at 500V

Discussion

Misclassification is a concern

• Next Step

• Test additional units at smaller voltage increments?

Human Body Model (HBM) MIL-STD883 vs JEDEC Test Methods

- Repeat experiment using smaller voltage increment (50V, 100V, 200V, 300V...) instead of +250V increment
 - Same test house, same test procedure, same date code.
 - MIL-STD883 = 3 consecutive pulses per polarity per pin (1 second interval)
 - JEDEC = 1 pulse per polarity per pin (0.3 second interval)

Results

- Part failed HBM based on MIL-STD883. Best is 200V
- Part demonstrated 50V HBM based on JEDEC. Best is ~500V
- MIL-STD883 is more sensitive → gross ESD failures across majority of I/O pins.
 Need to specify test method when quoting value for HBM
- Both methods identify a common weak ESD protection network located in upper section of the chip.
 - Proper ESD handling necessary as per NASA/JPL Doc 34906 ESD Technical Requirements Rev-N.

Discussion

- Additional data needs to be taken by the community/manufacturers
- A major manufacturer has agreed to take data
 - Testing will be done when they qualify a new device later this year

Summary

SN M1					SN M2					SN M3						
Pins	50V	100V	200V	300V	Pins	50V	100V	200V	300V	Pins	50V	100V	200V	300V		
1	Failed	NA	NA	NA	1	Failed	NA	NA	NA	1	Pass	Pass	Pass	Failed		
2	Failed	NA	NA	NA	2	Pass	NA	NA	NA	2	Pass	Pass	Pass	Pass		
3	Failed	NA	NA	NA	3	Failed	NA	NA	NA	3	Pass	Pass	Pass	Failed		
4	Failed	NA	NA	NA	4	Failed	NA	NA	NA	4	Pass	Pass	Pass	Failed		
5	Failed	NA	NA	NA	5	Failed	NA	NA	NA	5	Pass	Pass	Pass	Failed		
6	Failed	NA	NA	NA	6	Failed	NA	NA	NA	6	Pass	Pass	Pass	Failed		
7	Failed	NA	NA	NA	7	Failed	NA	NA	NA	7	Pass	Pass	Pass	Failed		
8	Failed	NA	NA	NA	8	Failed	NA	NA	NA	8	Pass	Pass	Pass	Failed		
9	Pass	NA	NA	NA	9	Failed	NA	NA	NA	9	Pass	Pass	Pass	Failed		
11	Pass	NA	NA	NA	11	Pass	NA	NA	NA	11	Pass	Pass	Pass	Pass		
12	Pass	NA	NA	NA	12	Failed	NA	NA	NA	12	Pass	Pass	Pass	Pass		
13	Pass	NA	NA	NA	13	Pass	NA	NA	NA	13	Pass	Pass	Pass	Pass		
14	Failed	NA	NA	NA	14	Failed	NA	NA	NA	14	Pass	Pass	Pass	Pass		
15	Pass	NA	NA	NA	15	Pass	NA	NA	NA	15	Pass	Pass	Pass	Pass		
16	Failed	NA	NA	NA	16	Failed	NA	NA	NA	16	Pass	Pass	Pass	Pass		
17	Failed	NA	NA	NA	17	Pass	NA	NA	NA	17	Pass	Pass	Pass	Pass		
18	Pass	NA	NA	NA	18	Pass	NA	NA	NA	18	Pass	Pass	Pass	Pass		
19	Pass	NA	NA	NA	19	Pass	NA	NA	NA	19	Pass	Pass	Pass	Pass		
20	Failed	NA	NA	NA	20	Failed	NA	NA	NA	20	Pass	Pass	Pass	Pass		
SN 11					SN 12					SN 13						

Pins	50V	100V	200V	300V	400V	500V	600V	Pins	50V	100V	200V	300V	400V	500V	600V	Pins	50V	100V	200V	300V	400V	500V	600V
1	Pass	1	Pass	Pass	Pass	Pass	Pass	Pass	Pass	1	Pass	Pass	Pass	Pass	Pass	NA	NA						
2	Pass	2	Pass	Pass	Pass	Pass	Pass	Pass	Pass	2	Pass	Pass	Pass	Pass	Pass	NA	NA						
3	Pass	Pass	Pass	Pass	Pass	Pass	Failed	3	Pass	Pass	Pass	Pass	Pass	Failed	NA	3	Pass	Failed	NA	NA	NA	NA	NA
4	Pass	Pass	Pass	Pass	Pass	Pass	Failed	4	Pass	Pass	Pass	Pass	Pass	Pass	Failed	4	Pass	Failed	NA	NA	NA	NA	NA
5	Pass	Pass	Pass	Pass	Pass	Pass	Failed	5	Pass	Pass	Pass	Pass	Pass	Pass	Failed	5	Pass	Failed	NA	NA	NA	NA	NA
6	Pass	Pass	Pass	Pass	Pass	Pass	Failed	6	Pass	Pass	Pass	Pass	Pass	Pass	Failed	6	Pass	Failed	NA	NA	NA	NA	NA
7	Pass	Pass	Pass	Pass	Pass	Pass	Failed	7	Pass	Pass	Pass	Pass	Pass	Failed	NA	7	Pass	Failed	NA	NA	NA	NA	NA
8	Pass	Pass	Pass	Pass	Pass	Pass	Failed	8	Pass	Pass	Pass	Pass	Pass	Pass	Failed	8	Pass	Pass	Pass	Pass	Failed	NA	NA
9	Pass	Pass	Pass	Pass	Pass	Pass	Failed	9	Pass	Pass	Pass	Pass	Pass	Pass	Failed	9	Pass	Pass	Pass	Failed	NA	NA	NA
11	Pass	11	Pass	Pass	Pass	Pass	Pass	Pass	Pass	11	Pass	Pass	Pass	Pass	Pass	NA	NA						
12	Pass	12	Pass	Pass	Pass	Pass	Pass	Pass	Pass	12	Pass	Pass	Pass	Pass	Pass	NA	NA						
13	Pass	13	Pass	Pass	Pass	Pass	Pass	Pass	Pass	13	Pass	Pass	Pass	Pass	Pass	NA	NA						
14	Pass	14	Pass	Pass	Pass	Pass	Pass	Pass	Failed	14	Pass	Pass	Pass	Pass	Pass	NA	NA						
15	Pass	15	Pass	Pass	Pass	Pass	Pass	Pass	Pass	15	Pass	Pass	Pass	Pass	Pass	NA	NA						
16	Pass	16	Pass	Pass	Pass	Pass	Pass	Pass	Failed	16	Pass	Pass	Pass	Pass	Pass	NA	NA						
17	Pass	17	Pass	Pass	Pass	Pass	Pass	Pass	Failed	17	Pass	Pass	Failed	NA	NA	NA	NA						
18	Pass	18	Pass	Pass	Pass	Pass	Pass	Pass	Pass	18	Pass	Pass	Pass	Pass	Pass	NA	NA						
19	Pass	19	Pass	Pass	Pass	Pass	Pass	Pass	Pass	19	Pass	Pass	Pass	Pass	Pass	NA	NA						
20	Pass	20	Pass	Pass	Pass	Pass	Pass	Pass	Pass	20	Pass	Pass	Pass	Pass	Pass	NA	NA						
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- Top row MIL-STD-883, S/Ns M1, M2, M3
- Bottom row JEDEC, S/Ns J1, J2, J3

NEPAG

Failure Criteria = ±15% tolerance between pre- and post-zapped

JC-13/ESD Activities

• JC-13 Started a Task Group on ESD

- The fact that it is a JC-13 task group means that it has the highest level of attention and applies to all commodities
- o Last meeting in Jan. 2020

• JEDEC/ESDA Are Continuing Joint Effort

- JESD 625B and S20.20 Harmonization telecons and face-to-face meetings
- Participation by NASA and Aerospace Corporation

Facilitated Technical Talk on ESD

- o By On Semiconductor
 - ✤ At January 2020 JC-13 meeting

Leveraging ESDA Standards Meetings

- The recent meetings in Riverside, Ca covered topics such as
 - ✤ Automotive (WG 27)
 - Finger cots and gloves (WG 15)
 - ✤ High reliability (WG 19)
 - ESD wafer foundry parameters (WG 22)

ESD Outreach by NASA

• NASA Is Highlighting ESD in *EEE Parts Bulletins*

- Released three special editions on ESD.
- The first dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment.
- The second ESD special issue focused on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The second issue also included an important reminder about regular ESD testing.
- The third issue provided an example demonstrating the importance of maintaining ESD discipline and a high-level risk analysis related to electrostatic discharge.
- The fourth issue was a Compendium.
- A guidelines document is planned next.

• Invited ESD Talks

 NASA has been instrumental in arranging invited talks at JC-13/CE-12 meetings.

NASA ESD Surveys of Microcircuit Supply Chain

NASA ESD Surveys

- Benefits not only NASA but the whole community
 - Especially vendors processing very expensive new technology parts (where the per unit price could approach \$200k)
- o Candidate companies are identified during DLA audits—but not a DLA activity
- Conducted by NASA ESD experts
 - The survey findings and corrective actions have been merely suggestions for improvements (but, in all cases, were implemented by the vendors)
- \circ Very well received
 - Some vendors have requested re-surveys every two years
- Working with Suppliers and DLA to incorporate NASA ESD Surveys into DLA audit agendas
 - Make efficient use of resources
 - Was done a few times, worked well

NASA ESD Surveys Are Meeting Greater ESD Challenges for Electronic Parts

Examples of NASA ESD Survey Findings

Findings

- ESD Protected Areas (EPAs) were not designated as such
- The so called ESD-safe curtains and cabinets were not safe! They needed shielding/grounding
- In several cases, chairs were noted to be non-ESD Safe
- Non-ESD items found on ESD work benches
 Sinders, plastic bottles, mouse pads
- CRT monitors were found near parts in engineering test. These are charge generators. CRT displays are not recommended.
- Cloth wrist straps were used typically. Prohibited per JPL 34906.
- Operator retraining certifications had lapsed
- Waste Bins/Bin Liners were found to hold or generate charge
- Ionizer generated + 2000V spikes when tested

JC-13/ESD Activities (Cont'd)

Continuing NASA ESD Surveys

- Conducted by NASA experts
- A major finding: The manufacturers are spending money to buy ESD safe material but those products need to be validated – our limited testing found the so called ESDsafe curtains, and cabinets were not safe!

Launch of the ESA/NASA Solar Orbiter mission to study the Sun from Cape Canaveral Air Force Station in Florida on Feb. 9, 2020.

Source: NASA Website

Photo credit: Jared Frankle



Electronic Parts and ESD FY20

Recently Reported ESD Issues

- Supplier A (JPL QA for ASL)
 - Ionizer generated +2000V spikes when tested. There were other findings as well.
 - Refer to audit report for details
- Supplier B (R. Evans and JPL QA, for JPL projects)
 - Not using ionizers where ESD sensitive parts are built
 - Evans to make recommendations
 - Brought up on Dec 18, 2019 NEPAG telecon
- Limited ESD Testing (ATL for NEPAG)
 - HBM testing shows interesting result
- COTS, 2.5D/3D and ESD (ECOTS)
 TBD

Potential ESD Issue Identified During Customer Source Inspection (CSI)

Cleanroom Humidity Nonconformance

- o A customer source inspection (CSI) was performed recently
- During the routine check of temperature and relative humidity in the cleanroom, humidity was seen to be 26.5%
 - ✤ Mil spec requires 35-65%
- o The manufacturer to notify DLA of their nonconformance
- o Further follow-up thru NEPAG
 - A NASA ESD Survey was conducted and recommendations were made

Device Design Enhancements – An Ongoing Process

• A major manufacturer enhanced ESD protection networks

- $\circ~$ To improve thresholds for HBM and CDM
- $\circ~$ To get higher yields
- $\circ~$ Four devices affected
- Qualification data was reviewed by microcircuits Qualifying Activity (QA) which includes DLA, The Aerospace Corporation and NASA

NASA ESD Mitigation Going Forward

- Mitigate Existing and Possible Future ESD Issues by Supporting Efforts in Six Categories:
 - 1. NASA ESD surveys
 - We would like to see the requirements documented in M38535 so DLA can take over oversight responsibility at least for QML suppliers.
 - Responsibility for mitigating the risks from non QML, COTS sources will require a different approach and we know in a significant number of cases, we will not be permitted access to monitor such facilities. This is a significant gap!
 - Independent evaluations of new technologies (e.g., high speed and high power microcircuits, GaN devices, SiC devices). Characterization of ESD thresholds per Human Body Model (HBM) and Charged Device Model (CDM) for new devices
 - 3. Independent evaluations of 883 vs. JEDEC test method equivalencies for HBM
 - 4. Low-ESD-threshold parts mitigation, e.g., GaN, very high speed ICs (GHz range) -- conduct limited tests to make recommendations
 - 5. Interfacing with industry groups (e.g., JC13, JC14, ESDA, EC-11, EC-12)
 - 6. Harmonizing ESDA 20.20, JEDEC 625, and other ESD standards

• Note: NASA Is Part of the Qualifying Activity (QA) for Space Microcircuits

Summary

- NASA brought many ESD concerns to the attention of the parts community
- All types of commodities affected for both military and commercial parts
- COTS hardware could be affected more severely
- Harmonization of 625 and 20.20 is in progress.
- NASA to continue ESD Surveys

NEPA

- Parts community must promote an ESD-safe environment!
- Unknown ESDS of Class Y, 2.5D/3D, others...
- Low measured values for older technologies
- M38535 has added a number of ESD updates but more needs to be done. There are other military documents that will require updates.
- Be mindful of ESD when shipping / handling parts and hardware!
- Develop next generation of ESD engineers.



BACK – UP

EEE Parts Bulletin ESD Special Issues

EEE Parts Bulletin Electrostatic Discharge Special Issue (Part 1)

NASA EEE Parts Bulletin (January – July 2016)



January-July, 2016 · Volume 8, Issue 1, Revision A, January 26, 2017 ecial Edition on Electrostatic Discharge (ESD) (The NASA EEE Parts Bulletin has been published since 2009)

Note: This revision adds a number of details and corrects ambiguities in the original issue that was released August 31, 2016 (the K. LaBel article on partnering and the back-page material were not changed).

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. We plan to release two issues. This first special issue deals with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This issue also includes an article about partnering in radiation and reliability testing. The second special issue will describe examples of ESD-related problems. Figure 1 is an example of damage caused by ESD



- Figure 1. Examples of ESD damage to microcircuits (Images courtesy of JPL Analysis and Test Laboratory)
- A static random access memory (SRAM) device with 5-micron features was deliberately exposed to an 8000-volt pulse from a 100-picofarad capacitor. This produced an approximately 5.3-ampere peak current pulse lasting just under one microsecond. Melting of conductive traces is typical of such ESD damage and creates an open circuit path.
- b) An undefined microcircuit with 1-micron line widths that failed in service after being exposed to a pulse of approximately 500 volts. This caused a breakdown of the SiO₂ layer and a short circuit in the part.

Upgrading ESD Control: Its Importance and **Possible Strategies**

A. What Is ESD and How Are ESD Controls Applied?

Electrostatic discharge or ESD in electronic parts is an electrical sparking event that functions like a tiny version of lightning. When two objects with different potentials are brought sufficiently close, a current flows toward the

ground equalizing the potential. These differences can be caused by friction of dissimilar materials (shoes on a carpet is a classic example), but even the difference in potential between a human body and an object may be enough to initiate an ESD event.

For electronic parts, built to carry minute amounts of current, tiny lightning bolts are a cause for concern. If such an errant current flow of an ESD goes along the outer case of a part or the outside of an ESD-resistant (antitatic) bag or shipper, there may be no problem. However, such a current goes through the part, serious damage ay result. ESD damage can include catastrophic damge and/or latent damage. Catastrophic damage is immeiately detectable by the resulting loss of function and ofen visible damage. Latent damage is not immediately deectable because there is no loss of function and often no isible sign of damage. However, the part has been weakned and may fail in the field or (worse) in space.

his has always been a serious concern for electronic arts, but it has grown steadily more urgent.

he purpose of this article is to sensitize the entire space ommunity, and in particular, the standards-developingodies to the fact that the ESD requirements must be learly specified in such standards documents so that verybody handling microcircuits, from manufacture to fial use can minimize ESD damage. Furthermore, the tandards must be updated to reflect the present level of echnology

this context, the role of DLA (Defense Logistics gency) for the department of defense (DoD) becomes tal. The standardization branch of DLA develops and aintains the military (MIL) standards, which are used for aintaining high-reliability quality parts production for the oD and for NASA. In addition, manufacturers and non-IIL standards organizations provide inputs to the stand-

hese standards are often enforced by periodic audits of arts manufacturers and their supply chains. The audit ranch of DLA officially conducts official enforcement. ASA actively supports DLA in both of these activities.

or the purposes of this article, we are focusing on monlithic microcircuits. The standard most commonly used the U.S. space community for high-reliability microciruits is MIL-PRF-38535, Integrated Circuits (Microciruits) Manufacturing, General Specification for. Any mirocircuit parts produced under the military system must e in compliance with the requirements of this document.

he 38535 is the periodically changing overall document ontrolling microcircuit quality and reliability. The ESD asects of the document clearly need updating. For audita, the requirements must be flowed down to the working udit, and it must be reflected in each manufacturer's ality management (QM) plan.

addition, the ESD-related standards used by other oranizations may provide ideas for upgrades to the MIL tandards. Conversely, it would be highly beneficial if the IL standard upgrades could be coordinated with those the other standards bodies so that practices throughout e industry might be as similar and interchangeable as ossible

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B. Why Improved ESD Control Practices Are Crucial

Microcircuit densification has increased pin counts significantly in the last decade, particularly for communication and computing products. NASA and the space community are using 1752-pin counts, and higher counts are growing more common in the general market.

Current ESD rating methods were developed with typical pin counts in the twenties. Applying these old device testing standards to modern high-pin count products can cause severe problems. Testing times increase dramatically. Worse, wear caused by repeatedly stressing the same path and the increasing influence of tester parasitic losses (parasitics) can lead to false-positive failures.

The increased capabilities attained by increasing parts density has come at the cost of greater sensitivity to ESD. Thus, it becomes increasingly important to implement better methods of controlling potential damage from ESD. A wide assortment of books and journal papers provides information on methods for mitigating ESD.

For high-reliability microcircuits (where a part may cost as much as tens of thousands of dollars), organizations often develop and enforce required policies and procedures designed to mitigate ESD. These policies and procedures are codified in standards

Furthermore, the landscape of microcircuit part production, handling, and shipping has changed radically. Because of the increased complexity of parts, the paradigm of a manufacturer shipping directly to a customer has largely given way to a highly dispersed production environment, which in turn, often requires highly dispersed ESD control among a number of organizations. Table 1 shows all the steps at which production or use of a microcircuit might be done by shipping to another facility. (The most extreme cases of maximum dispersion are more likely with new products such as flip chips.) Moreover each of the steps involves at least one environment each for working on the part, storing the part, and shipping the part to the next step in the production.

Much as increased pin counts increase the susceptibility to ESD, increasing the number of shipping steps in the supply chain increases the number of points where ESD damage may occur.

It is important to recognize and fully address all the risk points to which ESD sensitive parts are subjected: from when they are fabricated and delivered from the original component manufacture's (OCM) site; through supply chain avenues to user inventories; then on to kitting and upper-level printed circuit board (PCB) level assembly, sihle test and verification; and eventually to final box level assembly, test and final system level test. This is particularly important for handling, packaging, and shipping of ESD Class 0A devices (<125 volts in the Human Body Model).

models?: Those models are 1) human body model (HBM) based on people accumulating electric charges; 2) charged device model (CDM) based on materials becoming charged after they rub against other materials; and 3) machine model (MM) [designed to simulate a machine discharging through a device to ground].

- Do we want a standard for reducing the number of pin combinations required for testing?
- Would statistical pin testing be a good approach?
- How can the testing time be reduced without losing useful information (and significantly impacting the test data)?
- Should the MIL standards be expanded to include charged device model (CDM) testing?
- How do the new 2.5D and 3D configurations affect ESD testing?

We need to consider future trends when revising test standards. This issue is growing more important because the unit cost of contemporary devices are very high (and are growing costlier as more functionality is added), on the order of several tens of thousands of dollars per unit. Poor ESD environment for such products creates possibility of damage/ latent damage to them, both of which could be very expensive. Costs for implementing an ESD-prevention program are miniscule compared to the overall cost incurred in dealing with ESD damage.

The above concerns were presented by NASA representative Michael Sampson at the June 2016 G12 Space Subcommittee meeting. He proposed that the military documents that control the ESD requirements for testing and rating ESD event severity be reviewed and updated as a first step. As part of this update process, he suggested that Defense Land and Maritime (DLA), which serves as the qualifying authority to maintain the MIL system of parts qualification, perform an engineering practice (EP) study on ESD to detail these issues and compare possible specification changes with those being imple mented or proposed by other organizations, in particular the NASA Inter-Agency Working Group related to ESD (NASA IAWG-ESD), Ideally, coordination among the various standards-setting organizations would result in updated ESD standards with a great deal of commonality DLA shared the results of their EP study at the JEDEC meeting held in January 2017. Based on the EP study and responses to it, JEDEC (JC-13) has opened a task group to resolve issues related to ESD.

These document changes will require review and coordination with associated reference documents from other organizations to bring consistency

· Are all three commonly used ESD models still valid or should the standards focus on one or two

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EEE Parts Bulletin Electrostatic Discharge Special Issue (Part 2)

NASA EEE Parts Bulletin (August 2016 – May 2017)



August 2016-May 2017 • Volume 9, Issue 1 (Published since 2009), June 16, 2017 Second Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This second ESD special issue focuses on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The issue also includes an important reminder about regular ESD testing and a table of standard microcircuit drawings that were recently reviewed,

Figure 1 is an example of damage that was probably caused by ESD



Fig. 1. Detailed view of a damaged site on a metal oxide semiconductor field-effect transistor (MOSFET) probably caused by ESD.

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ESD, the Silent Killer-

A. Background

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There are several great points to consider with respect to ESD knowledge, practice, and compliance. However, the key for ESD program success is consistency. If we detect the results of an event, then, we [the operational group] should be able to ascertain and confirm that we never have any lapses in the program implementation. With systematic practices, we should be able to surmise that there

is no way any events can occur on the organizational proiect watch.

ESD is the silent killer in electronics, and the resulting impacts are hidden project costs that are the motivator to address project risk cost and schedule impacts. When an ESD event occurs, one of three scenarios may play out.

1) There is no impact, and no detrimental result. 2) There is a catastrophic strike and the immediate

failure is detected, isolated irs may be easy or done at nev are done.

le event may happen. Undene or more parts results in laare either detected during ns or (worse yet) during misen any resulting failures may

pens in the product life cycle e project cost for repair. Laion is weak due to lack of acmalfunctioning hardware for

we need the highest possible D program compliance at all

only include part costs, which (for a typical active part) to orogrammable gate arrays, labor and mission assurance real hidden costs can potening the diligence to complete failure analysis, possibly nuview boards and completion disposition of the ESD failure

alone associated with all the uthorities, subject matter exvare assembly personnel attings can in most cases out of the damaged part alone. so participate in system tearpart screening/testing of the e new part, reassembly, and em. Therefore, prevention is

of some metallic oxide semistor (MOSFET) devices that ssembly of a recent space tion (ISS) support instrument d, in ESD protective packagard-level assembly soldering d-assembly-level verification ting ruled out design or operational issues. The suspect parts were removed, tested,

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and shipped off for failure analysis.

Figure 2 shows the PCB assembly with two noted nonfunctional parts circled in red. Although not conclusive, the corner location of damaged parts on the board was thought to be important to the forensics analysis. One theory implied that handling of the board (by the perimeter) allowed for the ESD event to contact these parts directly. During transport, the board is handled only inside an ESD-approved materials bag. There were questions as to the integrity of these transport bags. Due to bag traceability and reuse issues, there was no definite conclusion on this concern.

Figures 3 thru Figure 7 Show the die and damage areas from various photographic and radiographic perspectives. During upper-level assembly circuit troubleshooting, the potential for design or operational damaging voltages to the MOSFET gates were conclusively ruled out. The circuit was incapable of generating the necessary damaging voltages that would have the effect observed.

C. Investigation Conclusion

The conclusion of this ESD failure investigation was that failure was attributed to user error but review of all ESD compliance logs showed that all precautions were taken during operator handling. Due to lack of further evidence. the OCM and the PCB assembly operation were not ruled out as possible culprits, but neither could be confirmed.

Under these circumstances the team was advised of the event and warned of the total cost for repair and the need to double check all future handling procedures. The board was repaired with same lot date code parts, and there were never any repeat operational issues with that PCB assembly nor at the box operational level. The "Silent Killer" only struck once on that program. At least as far as can be determined at this time.

Figures 1 through 7 (provided courtesy of NASA Langley Research Center) were generated by Hi-Rel Labs as par of a project Component Failure Investigation at Langley.

For more information, contact John E. Pandolf 757 864-9624



ircled in red.



Fig. 3. Optical micrograph of the die in the failed device. The red arrows indicate the damage sites.



Fig. 5. SEM image of one of the damage sites. The arrow indicates the area where the damage originated



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ET after delayering. The arrows indicate the damage at the ends of the gate runners.

damage sites on the die

Fig. 7. SEM image of another damaged area on the die. Note that the gate polysilicon fused during the failure, which is why the oxide is visible.

NASA Parts Bulletin

NASA EEE Parts Bulletin (August 2017 – May 2018)



August 2017 - May 2018 • Volume 10, Issue 1 (Published since 2009), July 17, 2018 Third Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. This is the third issue on the subject. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. The second ESD special issue focused on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The second issue also included an important reminder about regular ESD testing. This third issue provides an example demonstrating the importance of maintaining ESD discipline and a high-level risk analysis related to electrostatic discharge. Figure 1 shows a maior failure caused by ESD



Figure 1. An ESD event of roughly 2.3 kV struck an RF transistor. The current caused a hole penetrating the underlying diffusions and an accumulation of material that re-solidified and shorted between the emitter and the collector (image courtesy of Hi-Rel Laboratories).

ESD Issues and Specification Updates in Progress

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passed on to the space and military community. The many community standards organizations are the Soc of Automotive Engineers (SAE) and the JEDEC (not an Figure 2 summarizes the flow process developed to acronym), which have various committees involved with address major issues such as multiple conflicting ESD parts standards. The standards organizations may decide standards. In the figure, two paths lead from DLA audits to form a task group to further study issues raised, update and NASA ESD surveys to eventual changes in standards existing standards, or develop new standards. The manrelated to updates in ESD practices. The organizations ufacturers (JC-13) and users (SAE, CE-11, and CE-12) involved are the Defense Logistics Agency (DLA with its meet three times a year to discuss and update the elecengineering practice studies) in the upper path. The lower tronic parts standards. The standards organizations path includes the NASA Electronic Parts Assurance provide a forum in which parts suppliers. DLA NASA the Group (NEPAG, with its Government Working Group, military services, and other users discuss ways to modify GWG), the NASA ESD surveys, and the NASA EEE Parts the parts standards and specifications to deal with those Bulletins. The two paths converge with the findings issues

Standards Organizations · Society of Automation Engineers (SAE) · JEDEC (Not an Acronym) DLA Engineering Practice (EP) with DLA-VA Present Form Task study Information a Group(s) JC-13/CE-11/ Continue to CE-12 work with NASA c Parts NASA Parts community ass it on to the Bullotin Group to arrive at community Special AG) & NASA Edition ESD surveys reparation for Proposed Changes -Doing Homework

lards as a sample of how observations from DLA audits and NASA ESD surveys raise veloped for those issues

	fore the parts community tary document MIL-PRF-	F
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	(e.g., 883 vs. JEDEC of respectively, for human	F
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	Method 3015 items that	M
	own to 45 nm)	
pri-	contacts/pins (previous	F
ut an	pins, now many more,	

linx FPGA). This greatly

(e.g., 2.5D, 3D) have not

nds when revising test more important because vices are very high (and ctionality is added), on inds of dollars per unit. ch products creates the amage to them, either of Costs for implementing e miniscule compared to

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the overall cost incurred in dealing with ESD damage. NASA is working with the community on electronic parts

and ESD. DLA has issued a marked-up version of MIL-

PRF-38535 to Revision L. It includes many updates on ESD requirements. NASA is continuing to perform ESD surveys of the supply chain. There is also an effort to harmonize JEDEC JESD 625 and the Electrostatic Discharge Association (ESDA) 20.20 documents.

Reference

MIL-STD-883K, Test Method Standard, Microcircuits, Defense Logistics Agency, Columbus Ohio, April 25, 2016

MIL-PRF-38535K, Integrated Circuits (Microcircuits) Manufacturing, General Specification for, Defense Logistics Agency, Columbus Ohio, Dec. 20, 2013.

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Lessons Learned on the Importance of ESD Training and Hardware Access Limitations for CubeSat-Level Projects

In order to minimize the chance of an electrostatic discharge (ESD) event occurring and damaging hardware, it is extremely important to keep hardware access limited to those experienced with ESD precautions and/or trained to ESD control standards such as ANSI S20.20.

An example of this manifested on a small project using a comparably small supplier. The project was a six-unit CubeSat a 20 X 30 X 10 cm spacecraft that was deployed from the International Space Station (ISS) with a short mission duration of 90 days.

> For more information, contact Amanda Donner 818-393-8636

with a cost of less than \$10 number of sophisticated h came from suppliers to the small projects, many people this extends to CubeSat of these suppliers do not have ent system (QMS); rather they ed experience.

ear QMS level and can be ithout additional support. The lities may need ESD guidance

of the small suppliers was a ip providing a subsystem for development group needed

software. However, software as experienced with handling are more intimately involved ng of said hardware. Under le pressure, the software task needing regular access ifficiently instructed as to the r the ESD controls required.

electronics board to the testing, and during this testing ng. The root cause was not low-up investigations strongly s were not properly exercised during testing. One individual wrist strap while powering ining and experience of these ESD controls was clearly controls probably resulted in using significant schedule and

t. Possibly, the damage could subsystem had processes for teams and monitoring their

ere learned. First, a project check the ESD practices of all ond, that surveying activity evel teams or individuals who he hardware in addition to all embly and test personnel. truct their supplier to upgrade and possibly even provide

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tection of Electrical and blies and Equipment (Exted Explosive Devices), Association, 2014

A Risk Analysis Related to Electrostatic **Discharge and Other Failure Mechanisms**

A. Failure Reports Analyses and Results

The data analyzed for this study originated in failure reports spanning a period from January 2001 through September 2013. These reports were created when a system development project requests the failure analysis lab to perform a detailed analysis of a failed electrical component.

Background information for each is included describing the situation that led to the failure (e.g., failed a visual inspection or electrical testing). Occasionally, detailed information regarding the assembly history is included; for example, an incident occurring at initial power up or following environmental of electrical testing, or a unique situation such as testing following a component repair/replacement.

A total of 283 reports were reviewed. Data from 232 of these reports were categorized for this analysis. The remaining 51 reports described instances where the initial failures during system testing were not confirmed at the failure analysis lab. Situations where this could have occurred include undetected defects in the component mounting (e.g., an improper solder joint that was no longer present after the component was removed) or an intermittent fault. Figure 3 shows the number of failures that occurred per year, with a mean of 18 failures per year.



Figure. 3. Number of failures per year.

All of the failure reports were carefully examined to diagnose the root cause of the failure. In order to ascertain trends and causes, the failures were sorted into the following categories: electrostatic discharge, electrical overstress, thermal overstress, mechanical overstress, foreign material, and chemical reaction.

Electrostatic discharge (ESD) is the failure mechanism that occurs when there is evidence on the semiconductor die of severe, localized damage. The indication is typically in the form of a crater or eruption through the insulating oxide layer seen only using extremely high magnification such as a scanning electron microscope

Incidence of ESD damage involves almost instantaneous transfer of electrical energy coupled with a very high static potential. Thermal damage is minimal as compared to electrical overstress. Some reports mentioned instances in which device or circuit board handling was suspect with

NASA Parts Bulletin

NASA EEE Parts Bulletin (June 2018 – September 2018)



June 2018 - Sept. 2018 • Volume 10, Issue 2 (Published since 2009), April 30, 2019 Compendium Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. The EEE Parts Bulletin has released three special issues on ESD, and this issue is a compendium of these three issues plus an overall view of the subject matter. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured stored or prepared for shipment. The second ESD special issue focused on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The second issue also included an important reminder about regular ESD testing. The third issue provided an example demonstrating the importance of maintaining ESD discipline and a high-level risk analysis related to electrostatic discharge. This compendium issue begins with an overview of the subject of electronic parts and ESD. Figure 1 provides a reminder that the familiar static sparking from rugs or rubber combs can generate ESD effects. ESD damage can easily go undetected



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Figure 1. Electrostatic discharge is everywhere (image courtesy of Hi-Rel Laboratories).

Gaps and Mitigation Strategies for ESD

Progressively smaller and more complex microelectronic parts have grown steadily more susceptible to ESD. Consequently, they require more testing effort.

Furthermore, ESD damage can easily be too small for detection by many typical methods. As Figure 2 shows, serious ESD damage can be invisible to optical viewing and even to 6400 X by scanning electron microscope (SEM). In this instance, only a 33,000 X SEM view made the damage visible





Not Visible at 6400 x In SEM



Damage Visible at 33.000 x In SEM

S-00000 P-000 3. OKX 10KU ND: 9MM



ESD damage to most semiconductors is often so subtle that it cannot be seen without very high magnification (image courtesy of Hi-Rel Laboratories)

Such ESD damage affects all types of commodities for both military and commercial parts, and the lesscontrolled commercial-off-the-shelf (COTS) parts may be affected more severely than the military.

The parts community must promote an ESD-safe environment. Such efforts must extend from parts fabrication, through shipping, and all the way through installation of parts in the final products.

NASA has supported this effort first by bringing ESD concerns to the attention of the parts community. Mitigation strategies have been developed in response to this rising threat. Mitigation strategies include NASA ESD surveys, observations during audits, standards updates (including harmonization of standards), and outreach to the military and space communities

NASA has been supporting Defense Logistics Agency charge EC JS-(DLA) audits of the supply chain for many years. During the audits in recent years, the auditors observed that the as an MIL-PRF-38535 requirements were practically nonexistent regarding ESD aspects of electronic parts.

Hence integrating ESD requirements into d 3015 MIL- PRF- 38535 has become a key goal for the electronic parts community. The current qualification standards for MII-PRE-38535 and related standards were developed years ago with pin counts in the twenties. Now, pin counts are in the hundreds or more. For instance. Virtex field-programmable gate arrays (FPGAs) have 1752 columns, and manufacturers are striving for even higher counts.

Applying the old device testing standards to modern highpin count products can cause severe problems. Testing times and costs can increase dramatically. However, costs also drive the need for adequate quality assurance. Per-unit prices for advanced devices are approaching \$200K, and the costs would multiply for failures discovered after a part was mounted or (worse) was in the field... or worst of all, in space.

Another issue is that multiple organizations have developed ESD mitigation standards/specifications. Gaps have evolved not just because of new technology, but also because of inconsistencies of standards development

For the military and space community, the most glaring lumar issues are as follows Model

MIL-STD-883. Test Method 3015 Issues:

Too old

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- Does not include the charge device model (CDM), only the human body model (HBM)
- The test method needs to be revisited for smaller feature sizes down to 30 nm
- · The test method needs to be revisited for large numbers of contacts/pins, and vastly increased

- Continuing to conduct NASA ESD surveys.
- Interfacing with industry standards groups (e.g., JC-13, JC-14, ESDA, EC-11, EC-12).
- · Working especially with the JC-13 newly-formed task group to address ESD issues. [JC-13 defined in the bullet above-just added standards.1
- Harmonizing ESDA 20.20, JEDEC 625, and other ESD standards.

Final ESD Reminders

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- · ESD is a serious and growing risk for electronic parts use.
- Updated standards are coming, and they will help mitigate ESD risks
- However, the most important point to remember is that mitigation of ESD risk requires continuous vigilance in identification of risks and discipline in maintaining safeguards.

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