NEPP studies on The Reliability of Flip Chip Solder Joints and 2.5/3D Packaging

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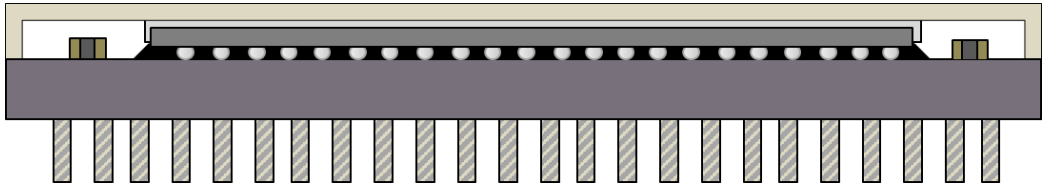
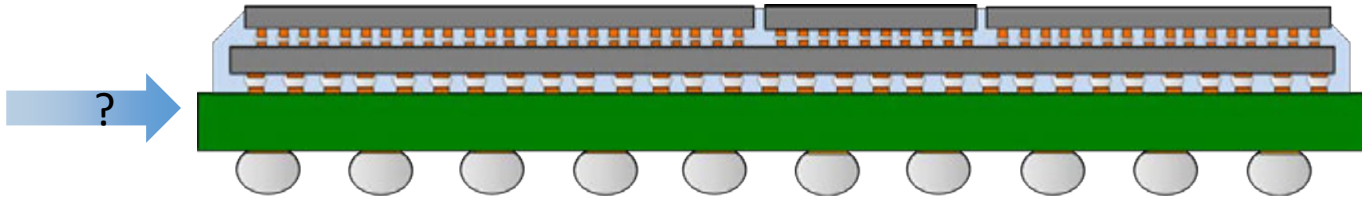
Introduction



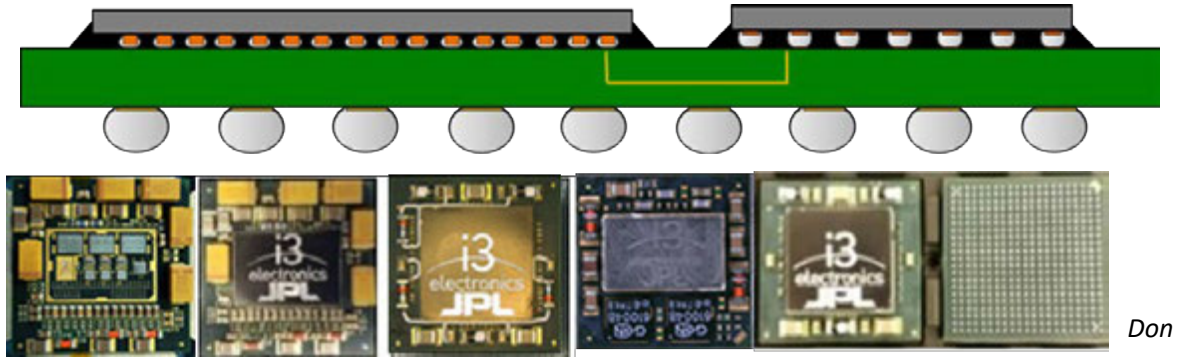
Class-Y Non-hermetic flip chip package



2.5D Package

- New NEPP task with Georgia Tech Packaging Research Center on 2.5/3D packaging
- This presentation
  - Implementation considerations of 2.5D packaging in space applications
  - What we can leverage from previous NEPP tasks and existing studies in terms of reliability
- "Heterogeneous Integration"
  - Broad definition : "Using a packaging technology to integrate dissimilar chips, photonic devices, or components"
  - Does not necessarily mean 2.5D/3D packaging.

*(*John Lau, Chip Scale Review, 2019)*

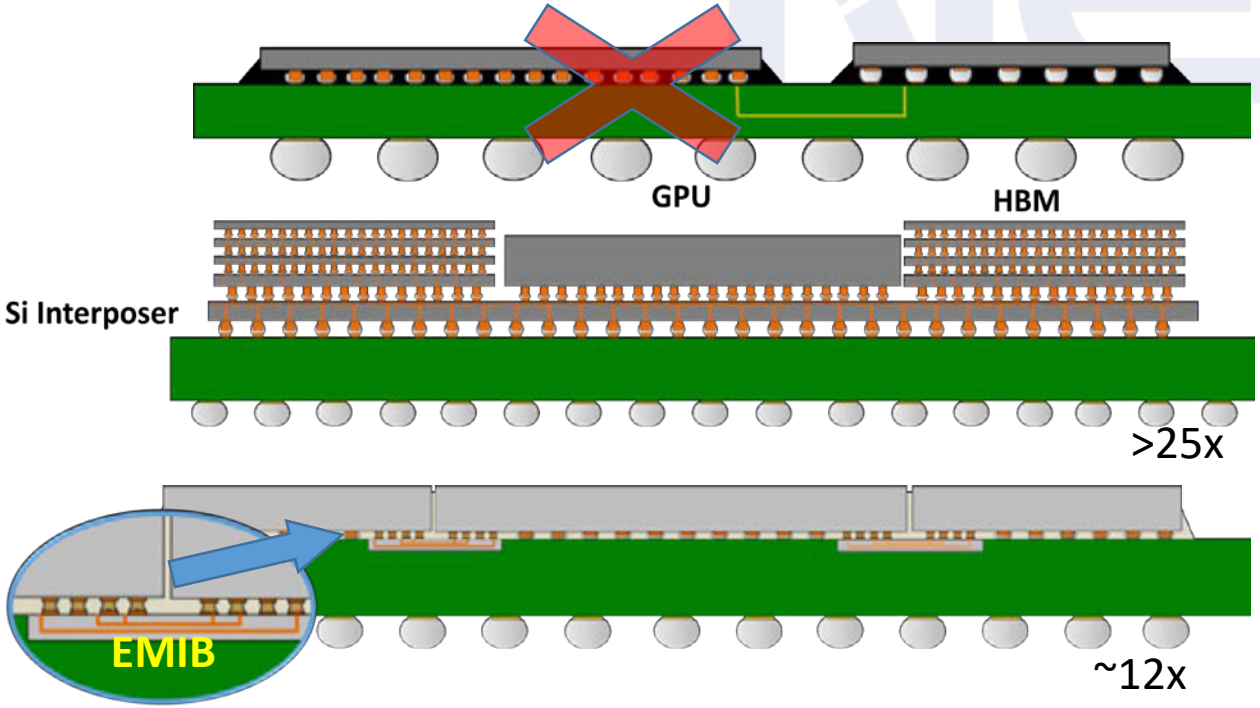


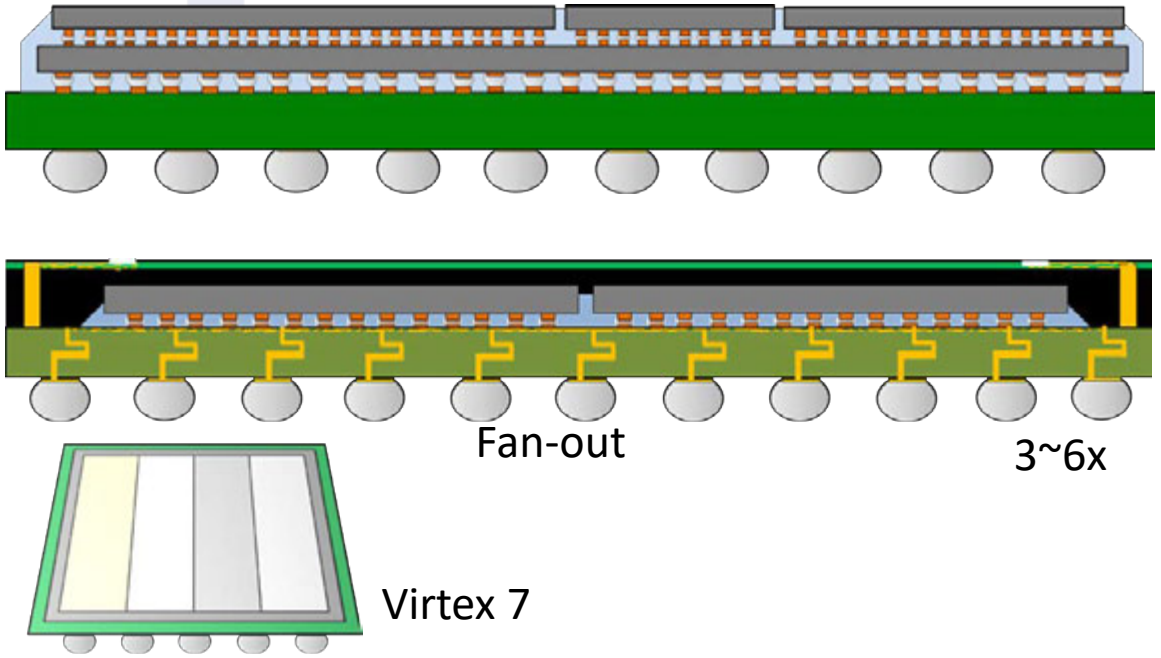
Don Hunter, Gary Bolotin, Doug Sheldon et al, 2018 ECTC

HIPER (Heterogenous Integrated Packages for Extreme Radiation)

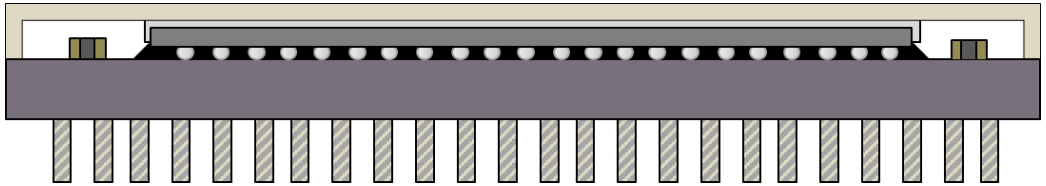
2.5/3D Level Heterogeneous Integration

- Heterogeneous Integration
  - In the context of describing 2.5D/3D packaging level of technology
    - Integrating dissimilar chips using a packaging technology with I/O density higher than organic substrate. (Feature size smaller than organic substrate, or 3D die)
    - Technology drivers :
      - **High bandwidth** between the processor and the HBM.
      - Integration of dies and **chiplets** with diverse IPs.
      - Improvement of **yield** by integrating smaller segments of die (Virtex 7).





Prerequisite Technologies for 2.5D Parts for Space: 1. Substrate



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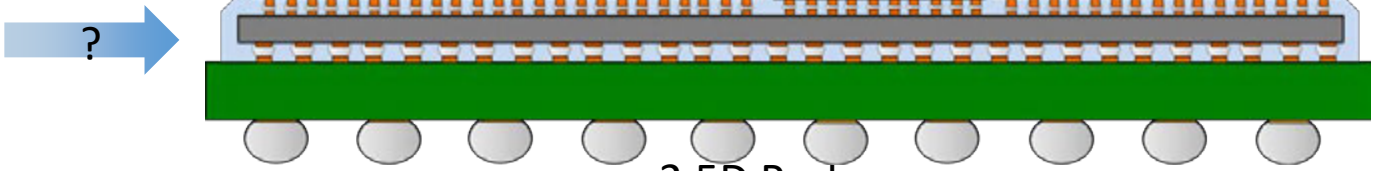


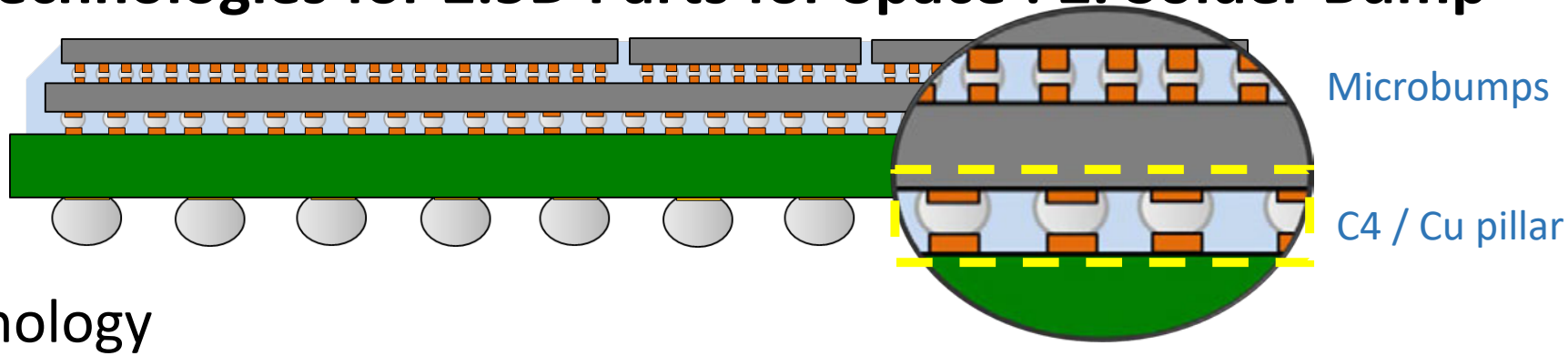
2.5D Package

1. Substrate

- Ceramic to Organic :
  - Organic substrate can support the feature size
  - Organic substrate can potentially enable better signal speed.
  - NEPP-Cobham collaboration task : JEDEC working group in progress for organic flip chip. (Lead : Scott Popelar)

	Ceramic (HTCC)	Organic
Bump Pad Diameter (µm)	~150	>60
Bump Pad Pitch (µm)	~250	>120
Trace Line Width (µm)	100~125	9~15
Trace Line Spacing (µm)	100~125	12~15
Via Diameter (µm)	125~200	50~65 (12mil for core)
Via Pitch (µm)	250~640	100~125 (40mil for core)
Dielectric Const.	8.5~10	3.2~4.8
Dielectric Loss Angle	0.0005~0.007	0.019~0.248
Trace Sheet Resistance (mΩ/sq)	8~17	3

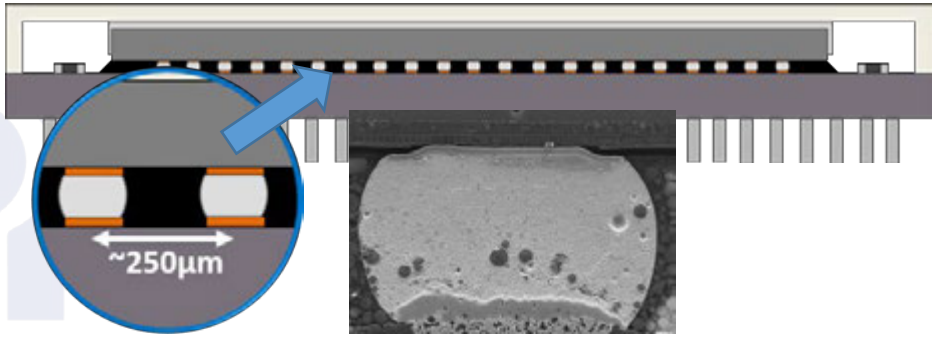
Prerequisite Technologies for 2.5D Parts for Space : 2. Solder Bump

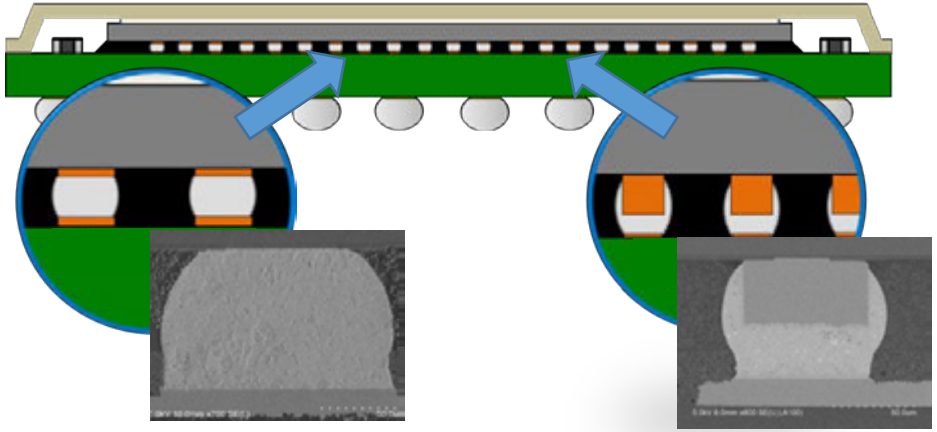


2. Solder Bump Technology

(between interposer and substrate)

- Current state of art for space parts
  - Ceramic packages
  - Class-Y (Non-hermetic), Class-V (Hermetic))
  - C4 bump (~250µm pitch)
- Organic substrate to die/interposer
  1) C4 bump
  2) Cu pillar bump (smaller pitch size than regular C4)
     - Organic package offers smaller feature size than ceramic.



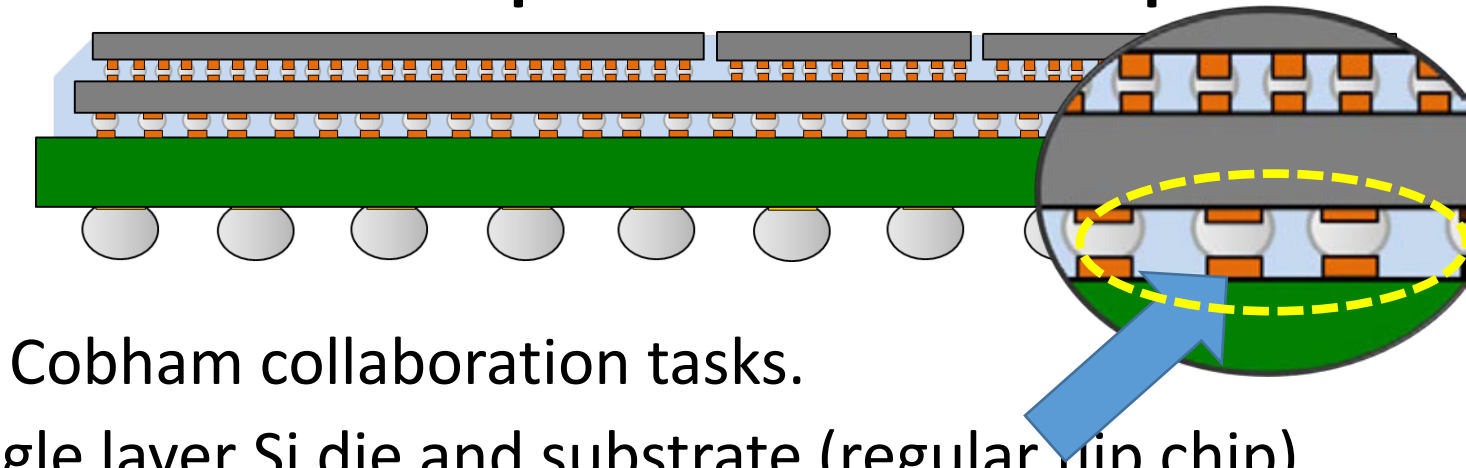


	Ceramic (HTCC)	Organic
Bump Pad Diameter (µm)	~150	>60
Bump Pad Pitch (µm)	~250	>120

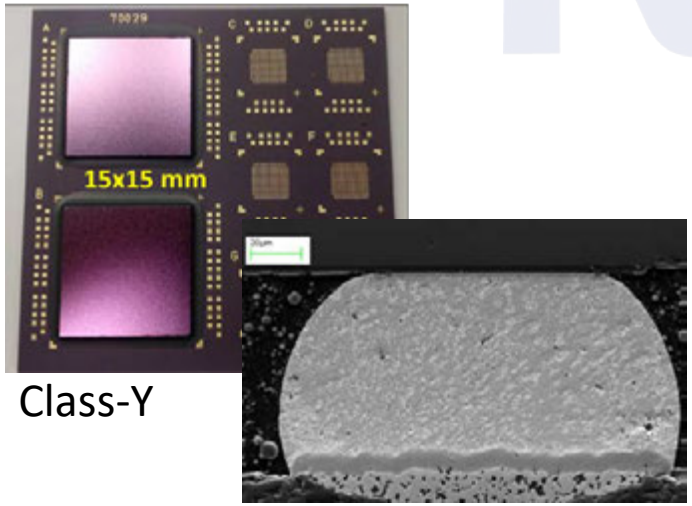
Prerequisite Technologies for 2.5D Parts for Space : 2. Solder Bump

Solder bump reliability

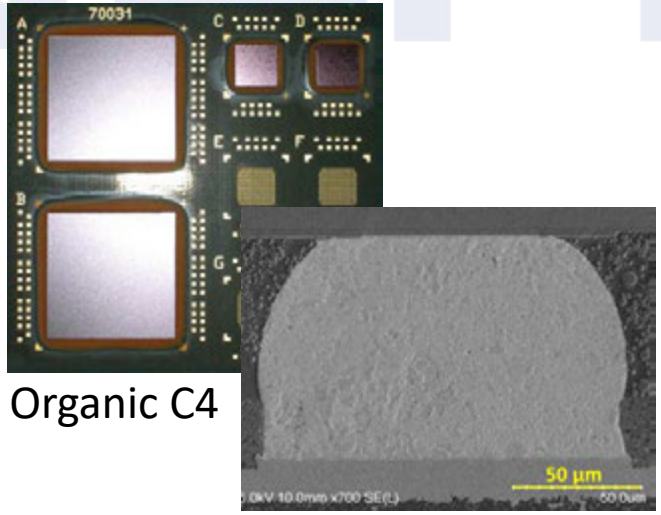
(between interposer and substrate)



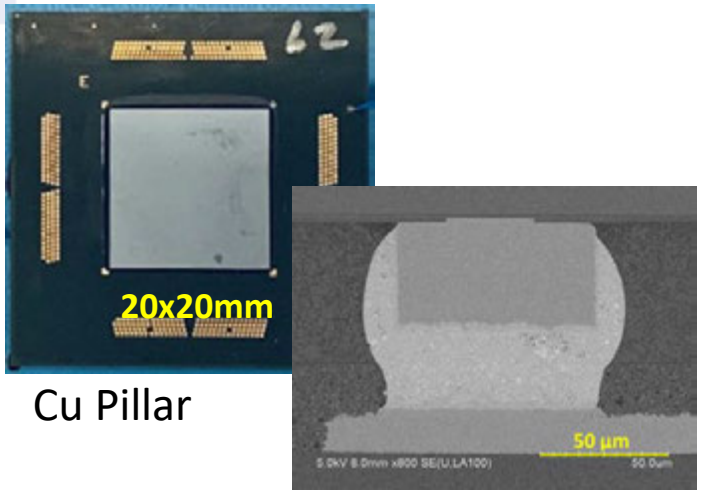
- Extensive studies through 3 NEPP – Cobham collaboration tasks.
- Solder bump reliability between single layer Si die and substrate (regular flip chip)
  - Test to failure



Class-Y



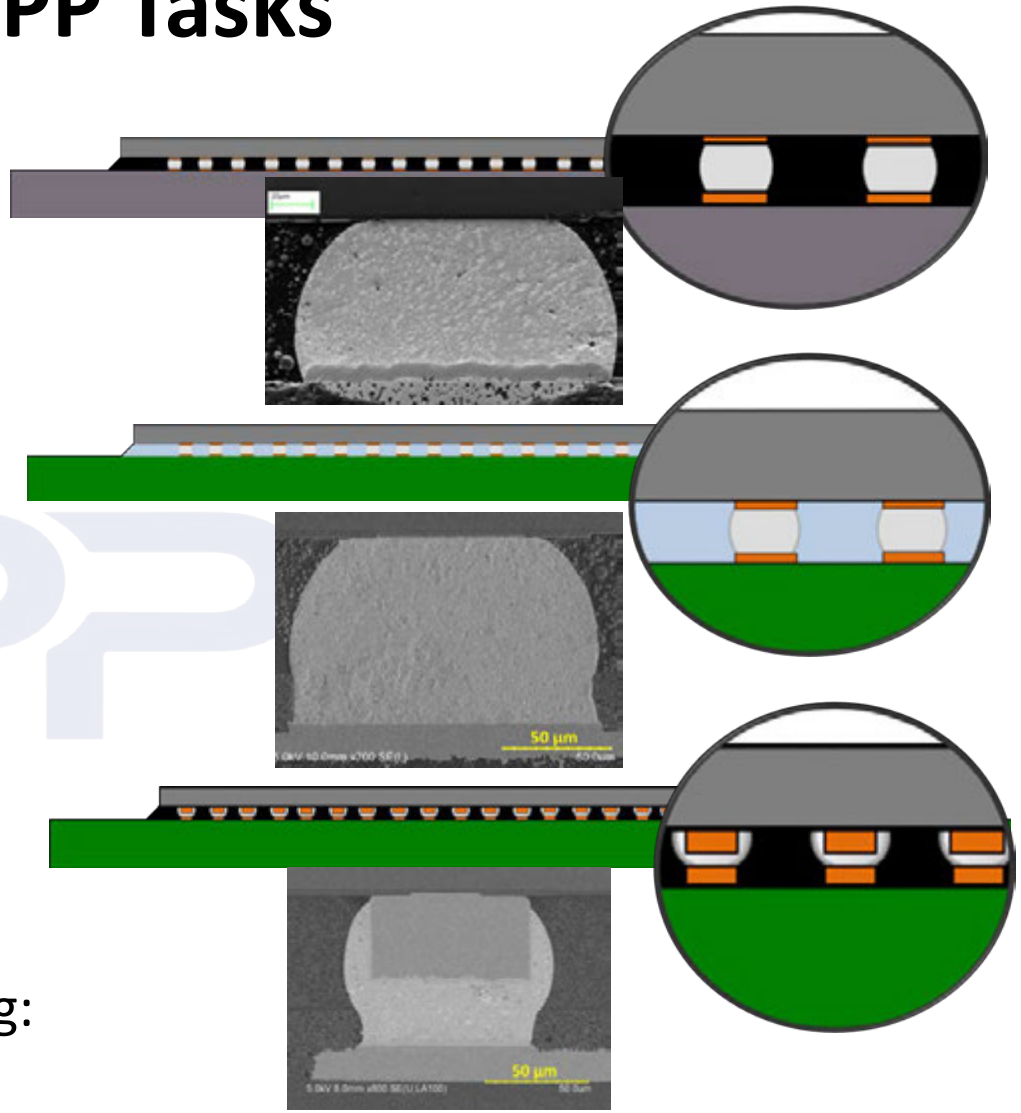
Organic C4

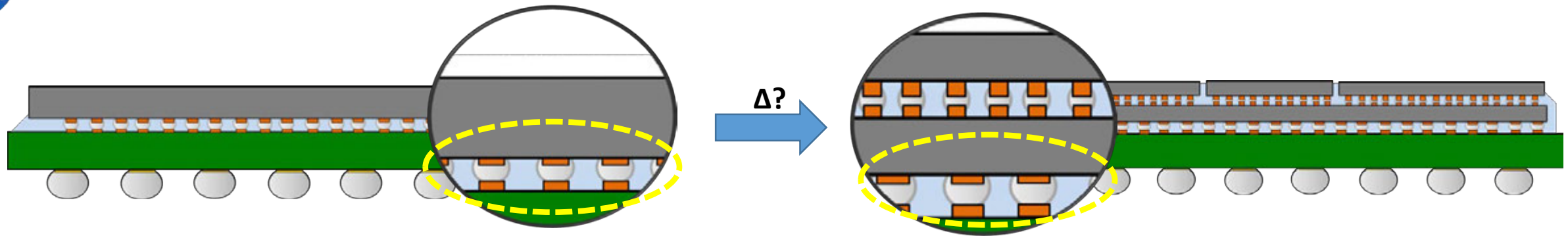


Cu Pillar

Variables Covered in Previous NEPP Tasks

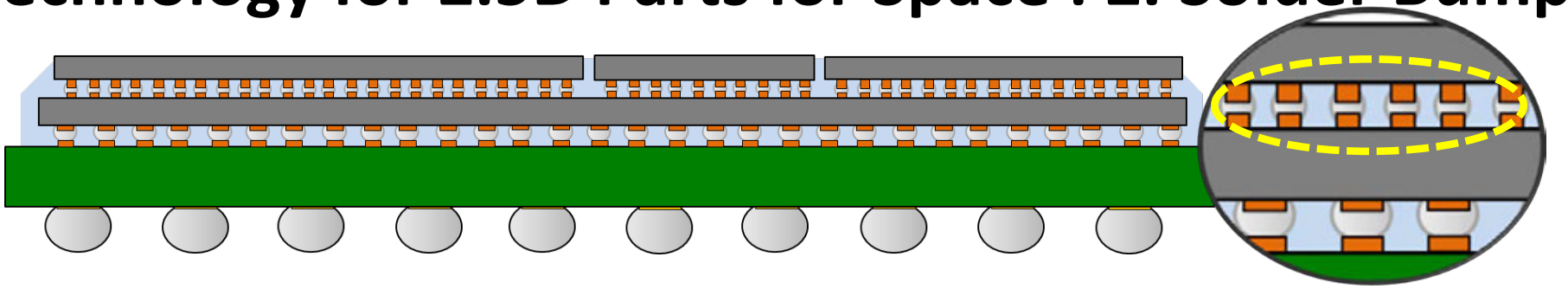
- Die Size
  - 5x5, 10x,10, 15x15, 20x20 mm
  - Level of stress in bumps
- Substrate material
  - Ceramic vs Organic
    - CTE and stiffness
    - Warping behavior
- Underfill materials
  - 3 different underfill
    - CTE, Tg, modulus, adhesion, etc
- Bump types
  - C4 vs Cu pillar – different size, pitch, and geometry
- Effect of environment exposure / pre-conditioning
  - Humidity, long term vacuum, multiple reflow, electromigration
- Main failure initiator or organic flip chips during temp cycling:
  - Fatigue delamination of underfill, causing solder joint failure.
- Organic C4 and Cu pillar can be as reliable or more reliable than Class-Y, if right underfill material is used with good workmanship.
  - Finding the right underfill by analysis is very difficult.





- Interactions of different materials at different stack-up and geometry
- Interposer thickness and stacked die.
  - Interposer is thinner than flip chip die.
- Effect of substrate warping due to the presence of PCB and extra dies.
  - Substrate inherently warps due to CTE mismatch with die.
  - Presence of PCB affects the substrate warping.
- Effect of using NCP/NCF instead of underfill.

Prerequisite Technology for 2.5D Parts for Space : 2. Solder Bump

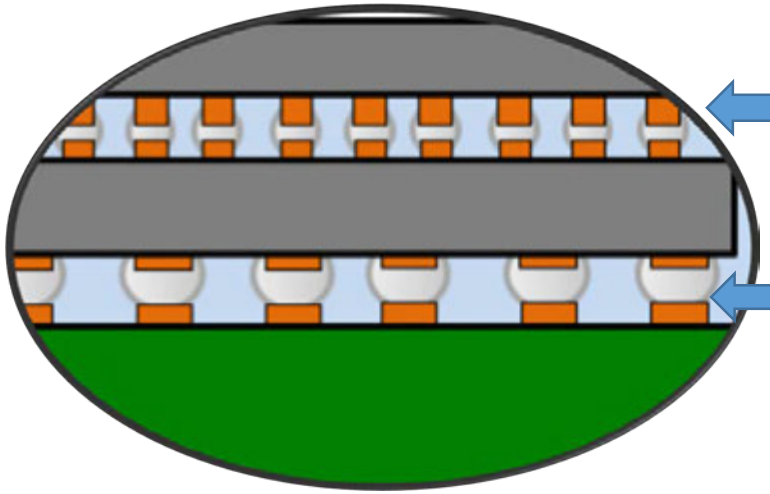


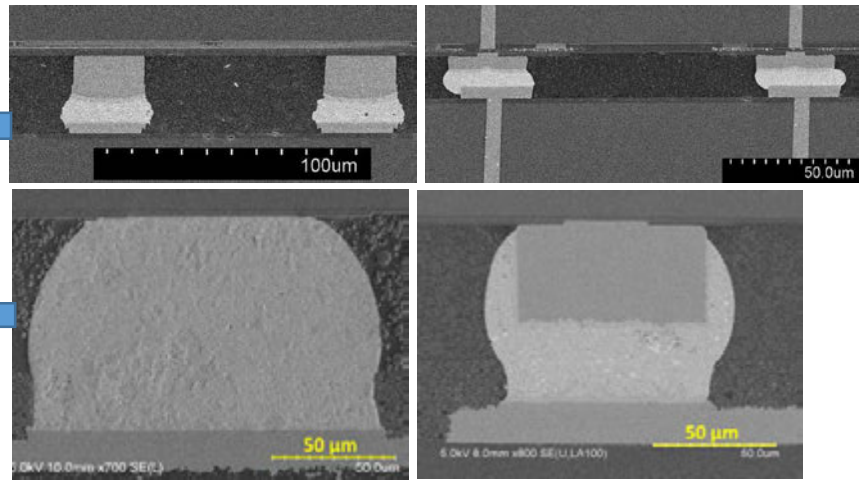
2. Solder Bump Technology

(Between dies and interposer)

- Fine pitch bump technologies.

1) C2 Copper pillar bump
2) Thermocompression bump



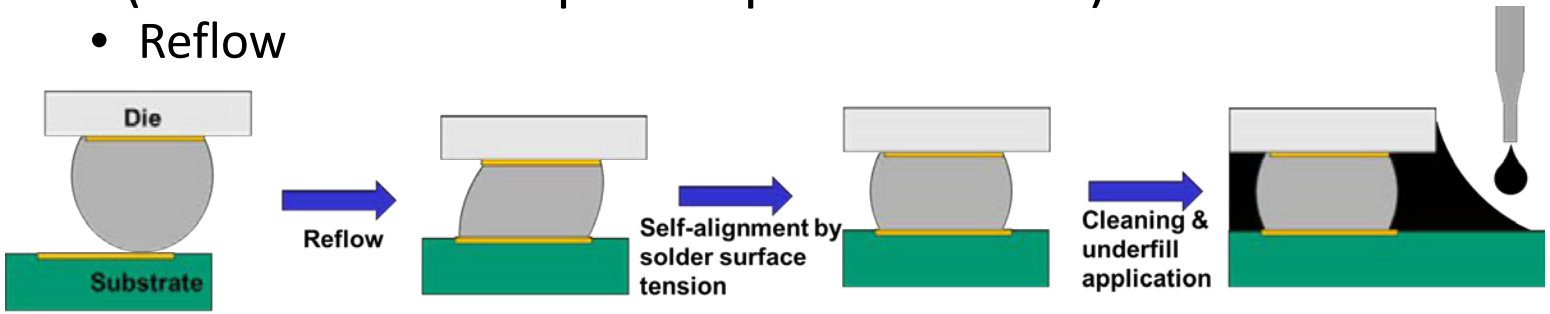


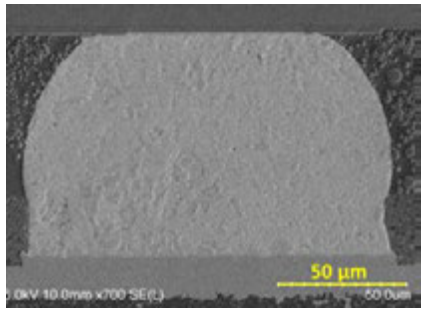
(Same scale)

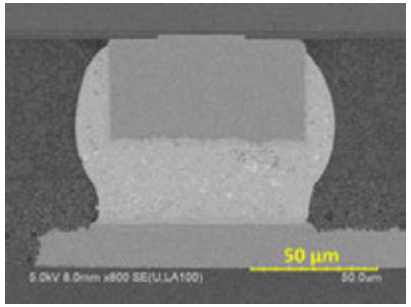
Very different assembly process

Prerequisite Technology for 2.5D Parts for Space : 2. Solder Bump

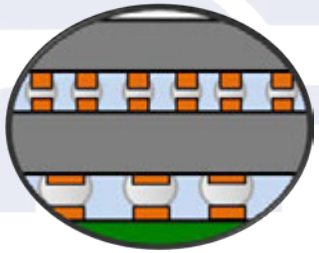
- C4 (Controlled Collapse Chip Connection)
  - Reflow

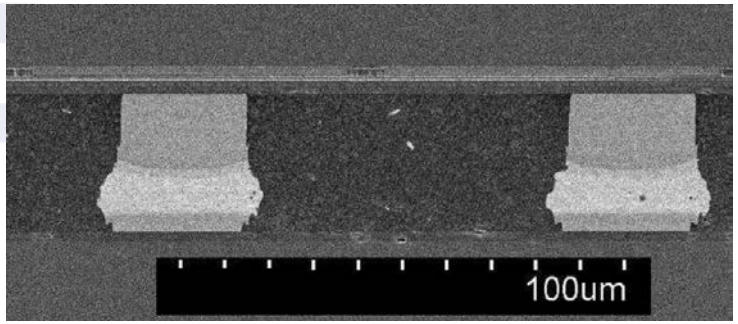






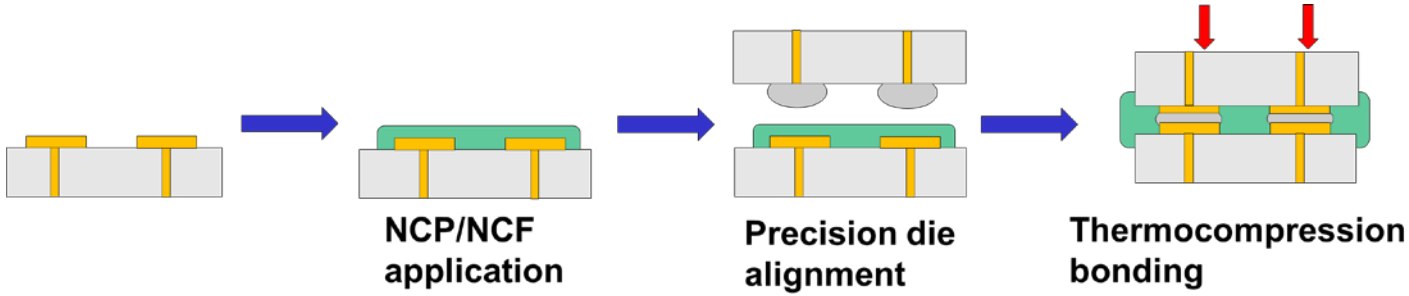
- C2 (Chip Connection)
  - Not enough solder volume to self-align.
  - Reflow or thermocompression bonding.

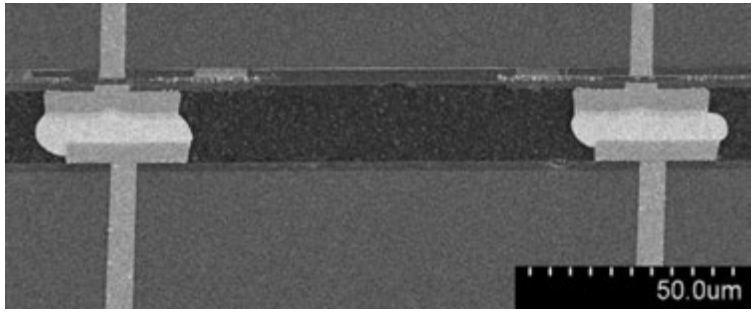




- Thermocompression bump.
  - Necessary technology for microbumps ~50µm pitch.
  - May need to use NCP/NCF instead of underfill for TC bumps.
  - Need different infrastructure and material than flip chip bumps.

**Thermocompression bumps are sometimes used between die and substrate.*

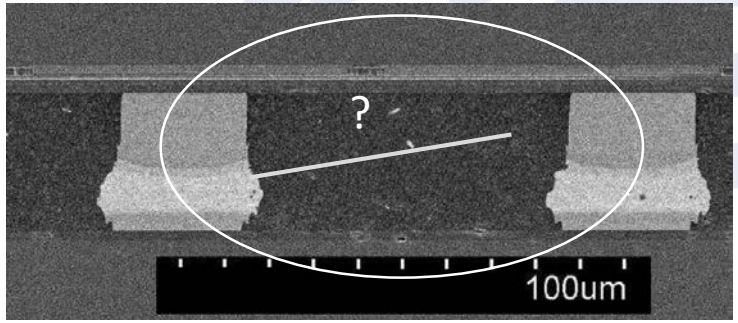


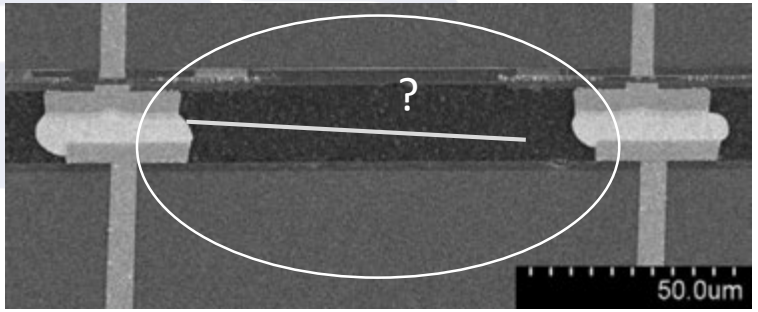


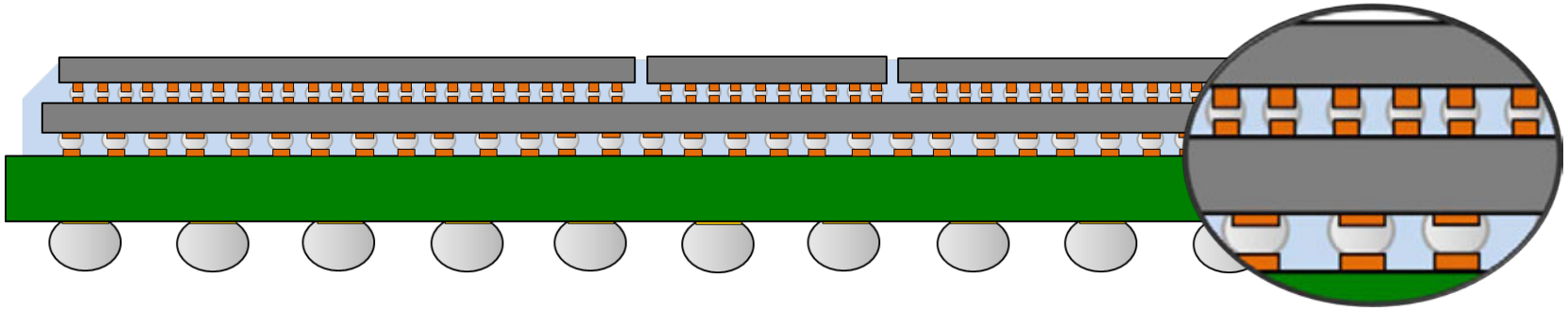
Prerequisite Technology for 2.5D Parts for Space : 3. Pb-free Microbump

3. Pb-free Technology

- Microbumps are Pb-free
- Do we need “0%” underfill/NCF void bridging 2 or more bumps requirement for whisker prevention?

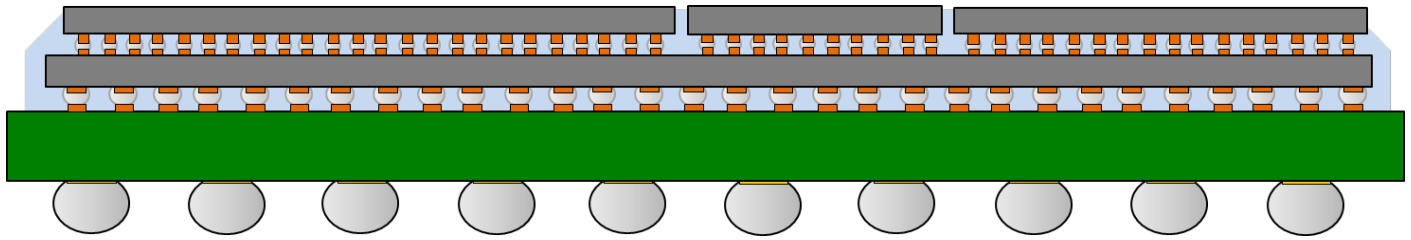






Heterogenous Integration Technologies and Die Screening/Burn-in (1/3)

- Screening / Burn-in for heterogenous integrating multiple dies.
  - Burn-in **before or after** integration?
    - “Integrated” dies
      - Electrical : Single entity
      - Reliability : “Weakest link” situation
  - Integration first, burn-in later:
    - How do we know if all the dies are burned-in to the right parameter?
    - If one die fails during burn-in, you lose all dies.

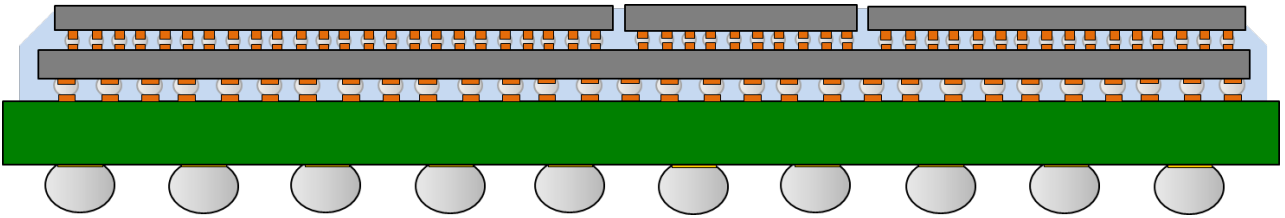


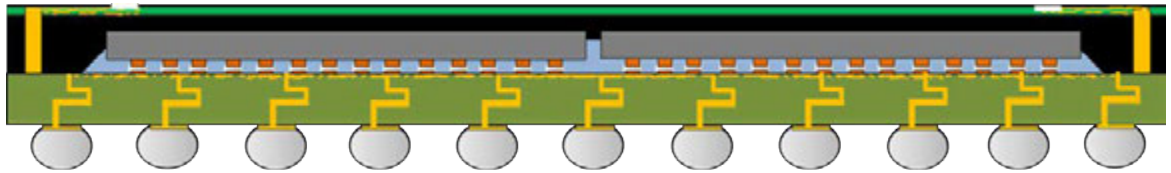
Heterogenous Integration Technologies and Die Screening/Burn-in (2/3)

	Si interposer or stacked die			Glass Interposer	Organic Interposer			Si BEOL + Organic sub	Fan-out			
Technology	CoWoS	Foveros (3D)	3D SoC (3D)	Glass Interposer	APX	i-THOP	RDL Interposer	EMIB	SWIFT	InFO_PoP	InFO_oS	FOCoS
Company	TSMC	Intel		Georgia Tech Consortium / Hynix	Kyocera	Shinko	Samsung	Intel	Amkor	TSMC	TSMC	ASE

- Chip-first vs Chip-last
  - Chip-first completes package or interposer after dies are already attached.
    1) Attach dies to partially built interposer (wafer) or fan-out package
    2) Complete the interposer or fan-out package
  - Even packages with very similar structures are built with different process flow.
    - The same technology can also have 2 versions.

(Should there be different QML flows for chip-first and chip-last?)





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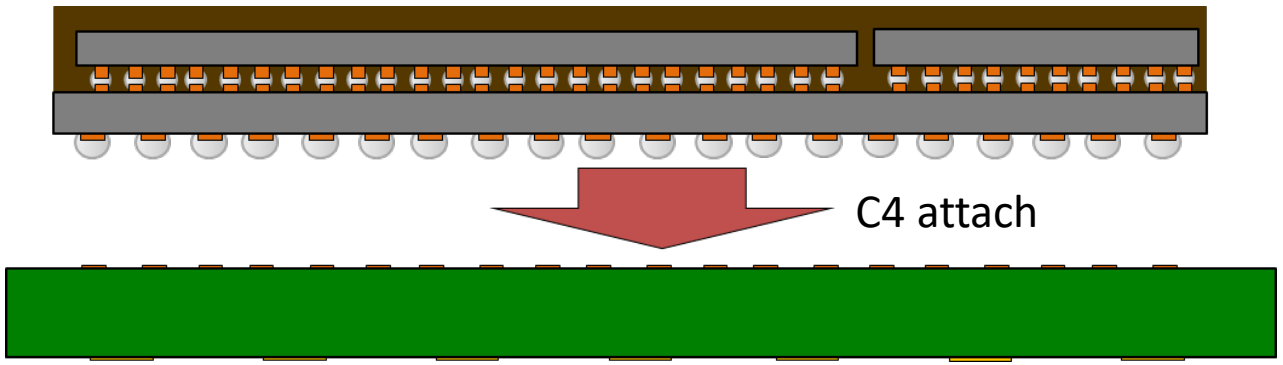
- Integrating already screened and burned-in dies via chip-first:
  - Schedule & cost are already spent on screening and burn-in.
  - Risk in attaching “known good dies” to “may or may not become good interposer/package”.
- Although chip-first has risk associated with integrating known good dies, some chip-first technologies have advantages.

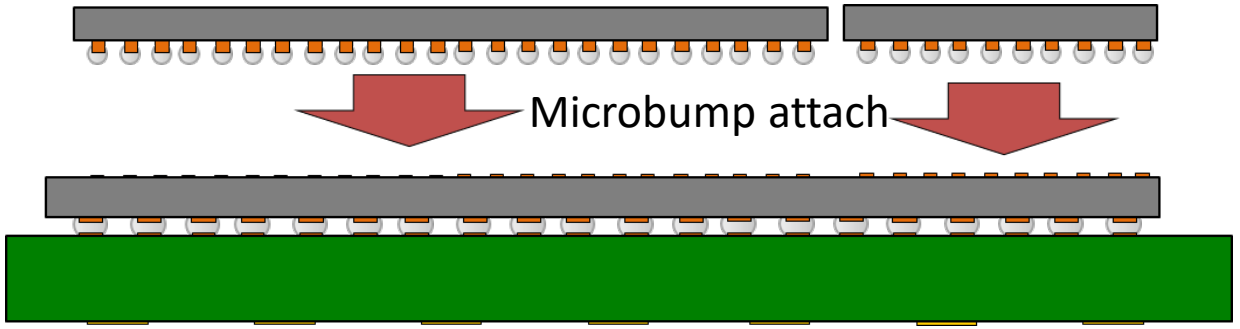
  ex) CoWoS : In customer’s perspective : ease in handling /assembly, more choice of packaging shops, can attach to a HDI board.
- When integrating already screened and burned-in dies, chip-first vs chip-last needs to be evaluated.
  - Yield/quality risk during packaging vs schedule and cost

CoWoS

Easier to assemble

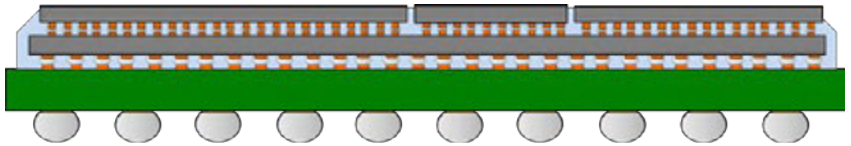


Easier to standardize

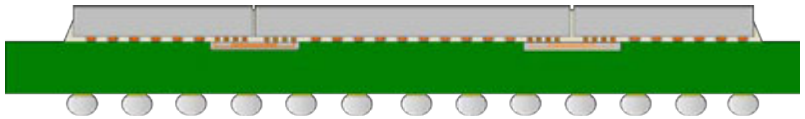


2.5D Package Study Direction of Current NEPP Task

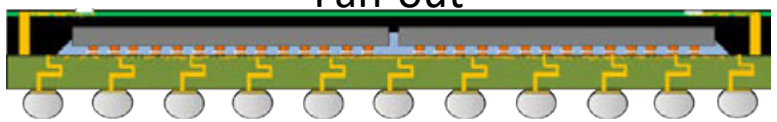
- Implementing heterogenous technologies for high reliability space application:
  - Fan-out :
    - It is not certain same QML flow can be applied to all fan-out packages.
      - Difference between each vendors' technology is large.
    - Rate of technology evolution may not be compatible with space parts life cycle.
      - (Time scale of technology lifespan) <= (time required for QML qual) ?
  - EMIB :
    - Intel-specific technology. May not be suitable for chiplet type integration.
  - Interposer-based chip-last packaging technologies:
    - Easier to standardize
    - Vendor process change cycle can be matched to space parts.
    - Difference between vendors can be small enough to setup QML flow.



EMIB



Fan-out



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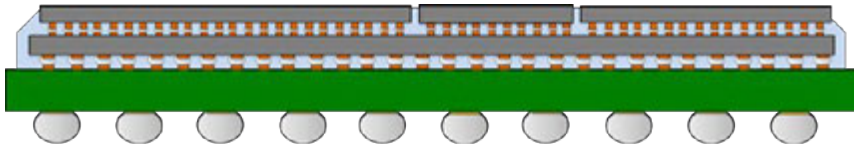
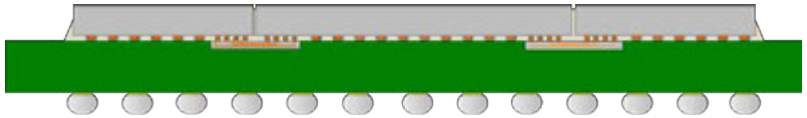
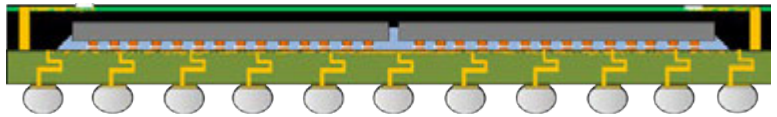
NEPP Glass Interposer Task

- Si interposer issues
  - Supply chain availability issue and high cost
    - Triggered development of alternate heterogenous integration technologies.
    - The supply chain availability is also a real issue for the space industry.
- Glass interposer
  - Can resolve the supply chain availability issue of Si interposer.
- Study will focus on reliability

  Ex) How different elements in 2.5/3D packaging stack-up interacts with each other and creates potential reliability issues.



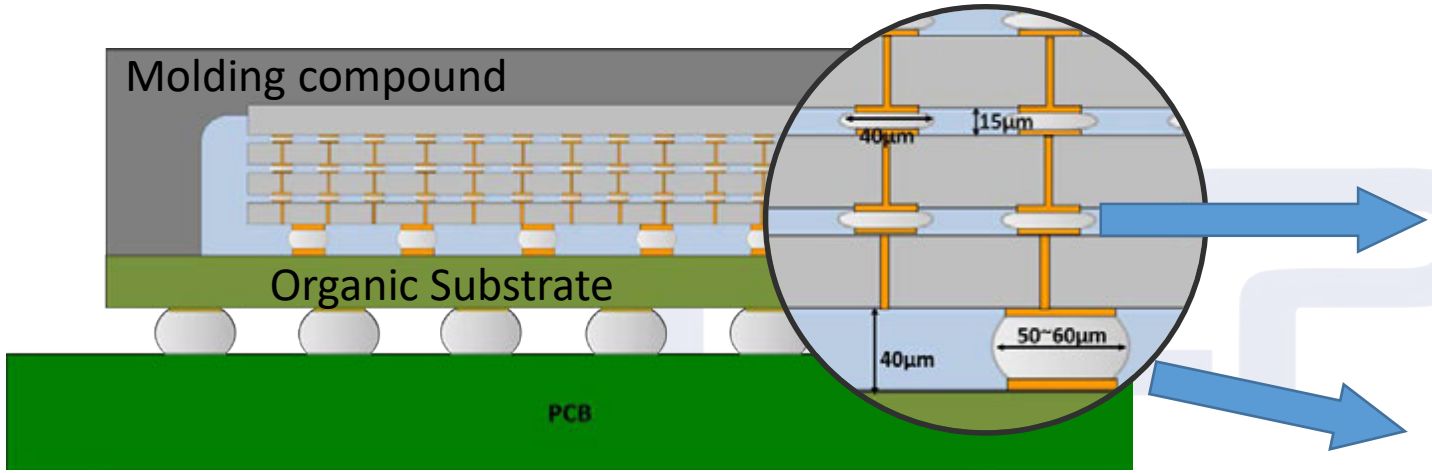




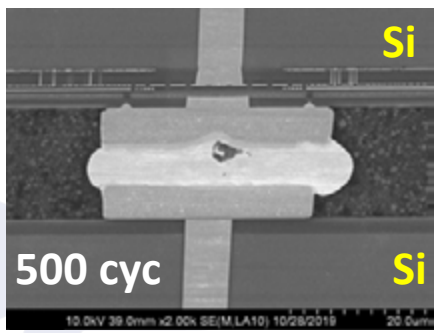
	Si interposer or stacked die			Glass Interposer	Organic Interposer			Si BEOL + Organic sub	Fan-out			
Technology	CoWoS	Foveros (3D)	3D SoC (3D)	Glass Interposer	APX	i-THOP	RDL Interposer	EMIB	SWIFT	InFO_PoP	InFO_oS	FOCoS
Company	TSMC	Intel		Georgia Tech Consortium / Hynix	Kyocera	Shinko	Samsung	Intel	Amkor	TSMC	TSMC	ASE

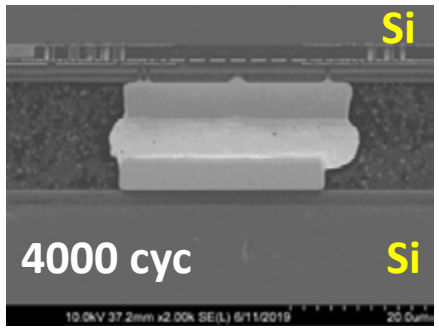
Example of CTE/warpage Effect on a 3D Device

- Cross-section were taken after TC testing of 3D memory module (note substrate in this case is a typical organic substrate used for BGA devices)

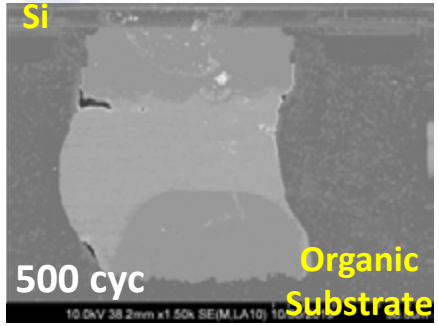


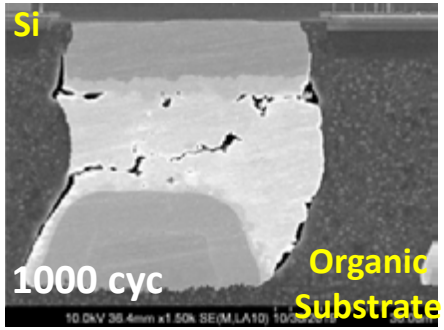
CTE matched





CTE unmatched

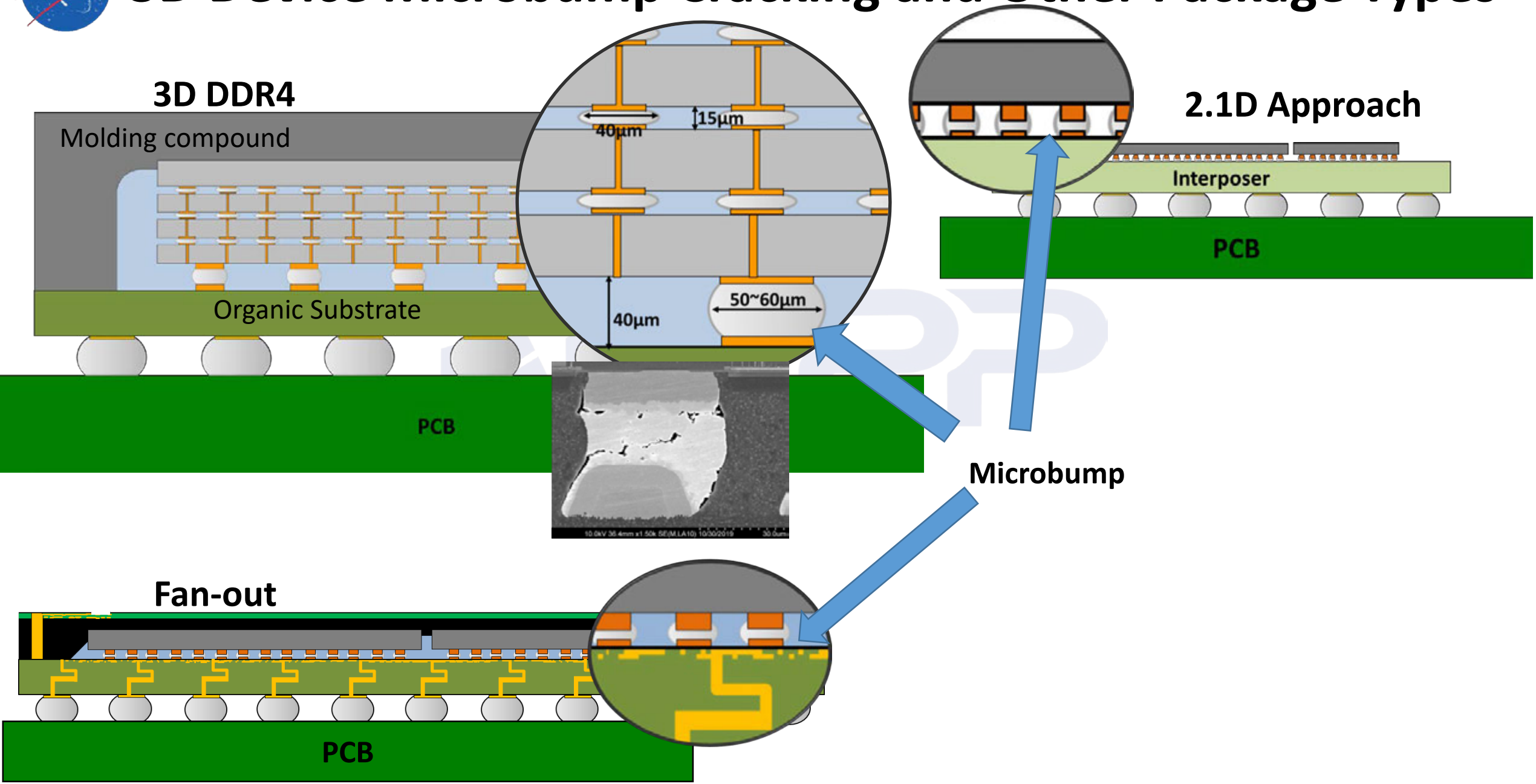




- Complete cracks were found at Si to substrate between 500 and 1000 cycles of -55 to 125C

- Device bump failed after board level failure, but at less than 1000 cycles bump reliability does not show margin usually expected

3D Device Microbump Cracking and Other Package Types



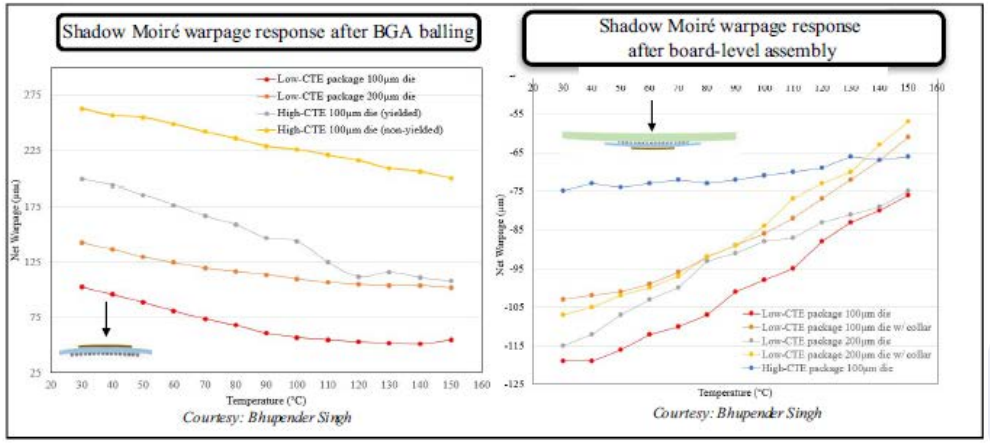
Summary of Interposer Influence on 2.5/3D Reliability

Contributions of Interposer to 2.5/3D Reliability		
Element Concern	Failure Mechanism	Influence of Interposer
Thin Die	performance impacted by device warpage	CTE; modulus; and flatness of interposer
Thermal	multiple die or stacked die increase heat and increased thermal path	Thermal conductivity of interposer; size/density of copper through vias and copper distribution
Through vias	Crack in copper (open), crack in interposer dielectric (possible shorts)	through via formation process, properties of copper; adhesion/barrier layers
Interposer RDL	Electrical Leakage Open	quality and behavior of passivation, consistency of spacing; adhesion of RDL; cleanliness Poor photolithography process; poor formation of vias; high stresses from poor material/process combinations
Chip to chip attach	warpage impacts on attach for chip last approaches	CTE; modulus; and flatness of interposer
C4/Copper pillar	cracks in the C4/copper pillar attach of die to interposer	warpage; CTE-modulus-reflow combined effects; underfill/NCP with interposer/die properties combined effects
Board level	Cracks in BGA due to warpage of device	CTE; modulus; material/stackup combined effects on warpage

- Interposer impact on reliability can viewed from 2 aspects
  1) Is the interposer (include though vias and RDL) reliable when subjected to manufacturing and environmental conditions?
  2) How will the intrinsic properties and design of the interposer impact the reliability of the 2.5/3D product?

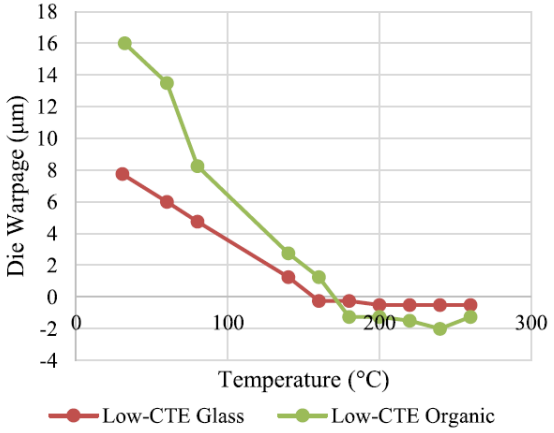
Some Measurements of Warpage with Different Interposers

GT Comparison of Si on Low and High CTE Glass Interposer



Jayaram et al, 2017

GT Comparison of Si Low CTE Glass and Organic Substrates



McCann et al, 2017

Xilinx Test Vehicle with Si on Si Interposer on Organic Substrate with Lid

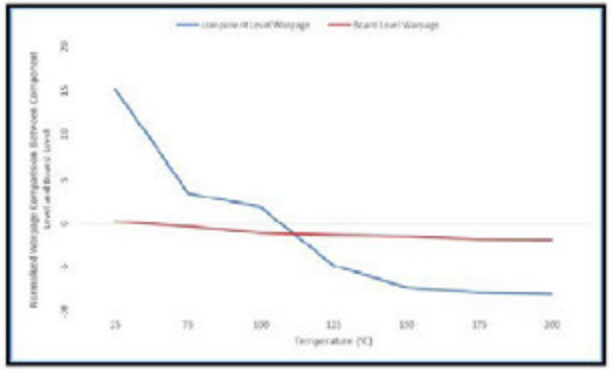


Figure 1: Normalized warpage comparison of an independent 3DIC device and one mounted on board

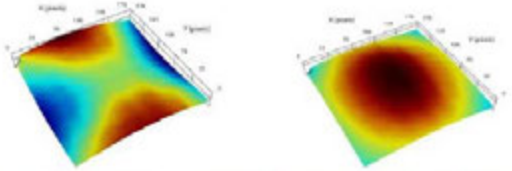


Figure 2: Warpage comparison at room temperature

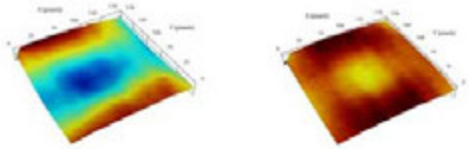


Figure 3: Warpage comparison at high temperature

Hariharan et al, 2017

- Interposer CTE is a big driver of warpage
  - This is critical to both board level and part level reliability
- Interposer stiffness is a key factor on warpage
  - Can vary warpage up to 2x over reflow
- Warpage of device after attached to board is significantly changed
  - Test vehicles should be attached to a circuit board

Testing Interposer Reliability in 2.5/3D Products

Contributions of Interposer to 2.5/3D Reliability		
Element Concern	Failure Mechanism	Influence of Interposer
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Board level	Cracks in BGA due to warpage of device	CTE; modulus; material/stackup combined effects on warpage

Interposer should have standalone test data for design rule set, material, and manufacturing flow.

Modelling is key to understanding interposer impact (which is only one of several major elements). Modelling should have a similar test vehicle to validate. Test vehicle should have functional die with similar technology to help detect such aspects of cracking of low k dielectric or thermal effects.

A set of test vehicles and analysis is needed to have an effective packaging design kit.

Future Work Focus Area

- Understand from first principles stresses and warpage caused by interposer, underfill, lid, and manufacturing flow process to help define a design kit for NASA 2.5/3D packaging.
  - Modeling and experimental studies on interactions between interposer, underfill, lid and manufacturing process.
  - Variables : design and material
- Better understanding on microbump process and reliability.
  - C2 bump
  - Thermocompression bump
- Screening & in-process control methodology for reliability.