High Density Packaging Technologies

Through Silicon Via (TSV)

by

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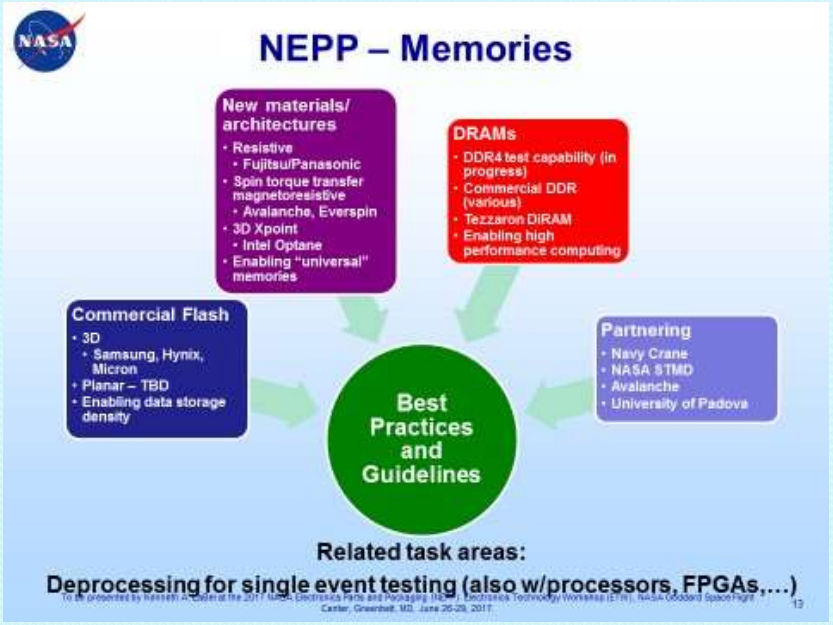
http://nepp.nasa.gov

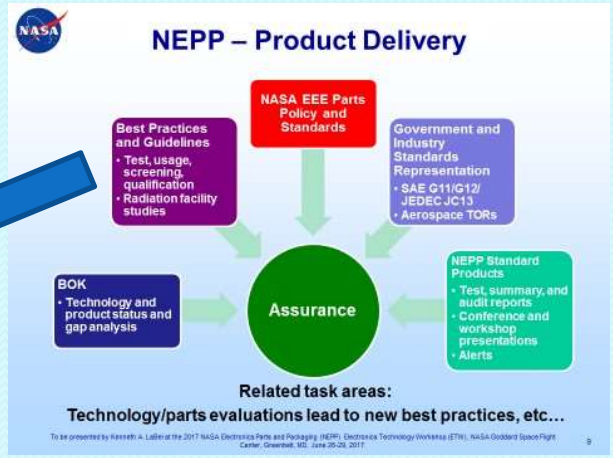
Outline

- 2.5/3D Packaging Trends
  - NEPP Task Deliverable: TSV Evaluation
  - Industry 2.5/3D Packaging Technologies
  - NEPP on High-Density Packaging Technologies: Current and Previous
    - PoP/3D
    - SiP
    - TSV-Through Silicon Via Daisy-Chain Evaluation
- PoP/3D Reliability under Thermal Cycling
  - PoP: 4 assembly configurations
  - PoP: Thermal cycle (-55/125°C)- Results & failures
  - 3D : Single and double-side under thermal cycles (-55/100°C)
- SiP Reliability under Thermal Cycling
  - Flip chip and BGA on BGA Interposer
  - Thermal cycle (-40/125°C) TC & failures
  - Weibull plots and the effect of BGA underfill
- TSV Daisy-Chain Evaluation
  - TSV Daisy-chain concept
  - 3TSV build with two interposers
  - PCB Design for WLP & TSV
- Summary

TSV

NEPP Packaging Evaluation





Test Results on NEPP Website

Best Practices and Guidelines

- **Test, usage, screening, qualification**
- **Radiation facility studies**

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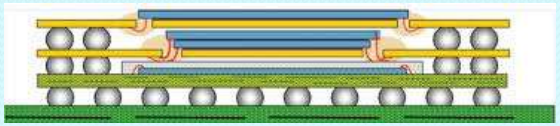
2.5D/3D
Packaging Technologies

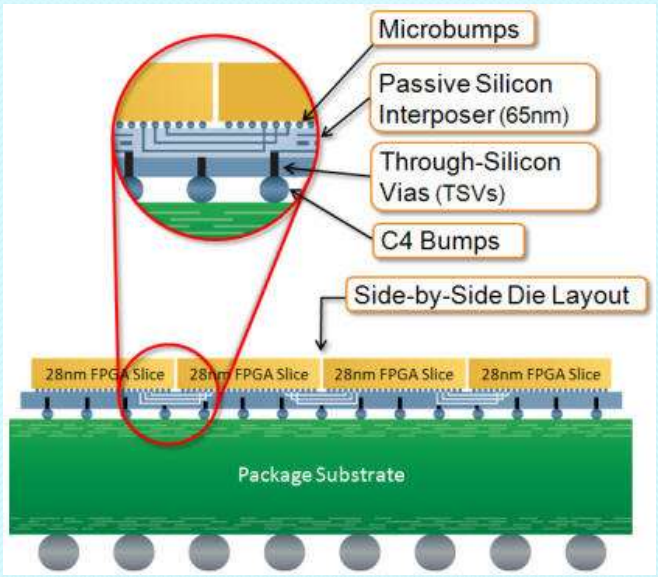
Stack Die
PoP

Package on Package (PoP)

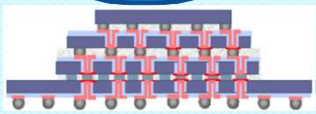


3D Wire Bond

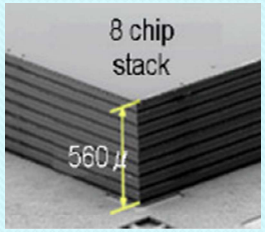
*2D to 2.5 D**
Single Chip to Multi-chip
TSV for Interposer



2.5D to 3DTSV
3D SIP

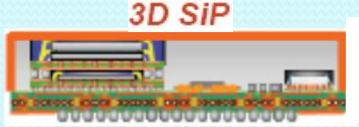


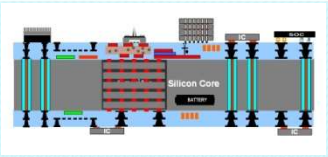
3D Wafer-level Packaging



Through-silicon Via

3D SiP





* 2.5D now 2DS (on silicon substrates) and 2DO (on organic substrates)

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Nomenclature Converges

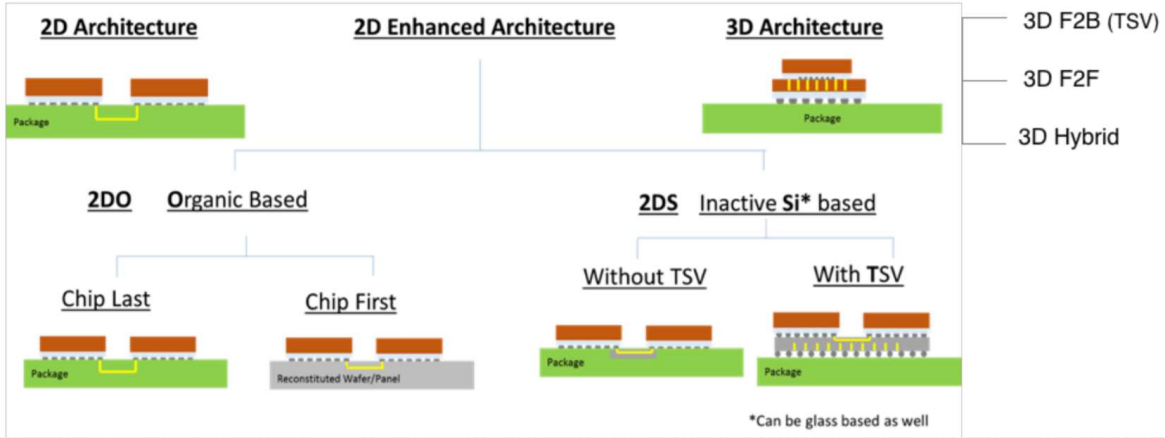
2DO/2DS & 3D

- ✓ **A 2D architecture is defined where two or more active silicon devices are placed side-by-side and are interconnected on the package**
  - ✓ 2DO (2D Organic) uses an organic medium
  - ✓ 2DS uses an inorganic medium (e.g. a silicon/glass/ceramic interposer or bridge)
- ✓ **A 3D architecture is defined where two or more active silicon devices are stacked and interconnected without the agency of the package**

Converged Nomenclature Framework for 2D & 3D Architectures

HETEROGENEOUS INTEGRATION ROADMAP

Previous Nomenclature	2D	2.x D (x=1, 3, 4, 45, 5)	3D
Definitions	*Side by side active Silicon interconnected on the package*	*Side by side active Silicon interconnected at higher densities…*	*Active Silicon stacked and interconnected on active Silicon without agency of the package*



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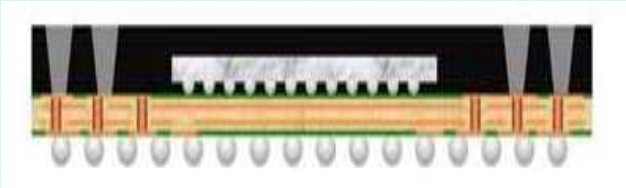
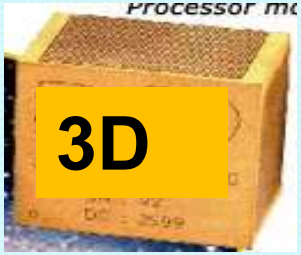
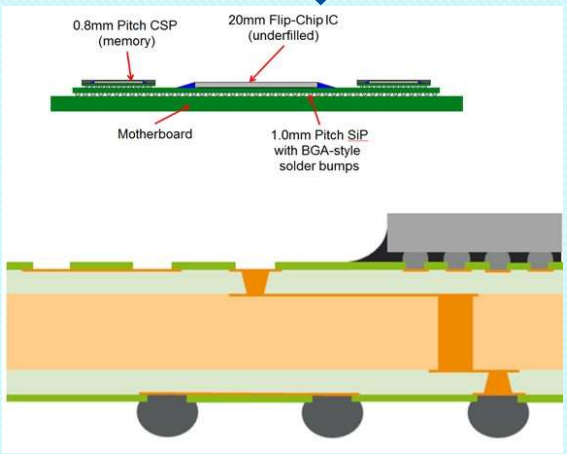
NEPP Packaging 3D Evaluations

PoP/3D

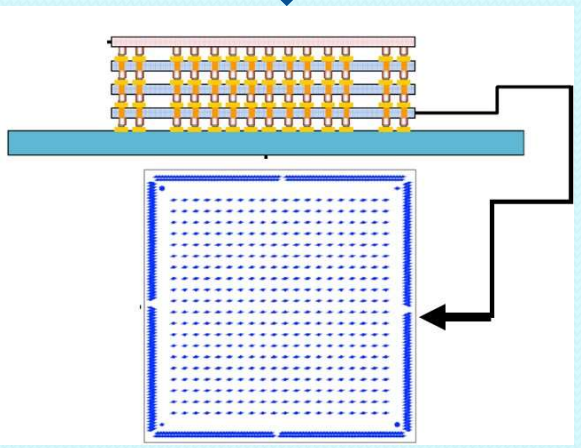




2.5 D/ SIP



3D TSV



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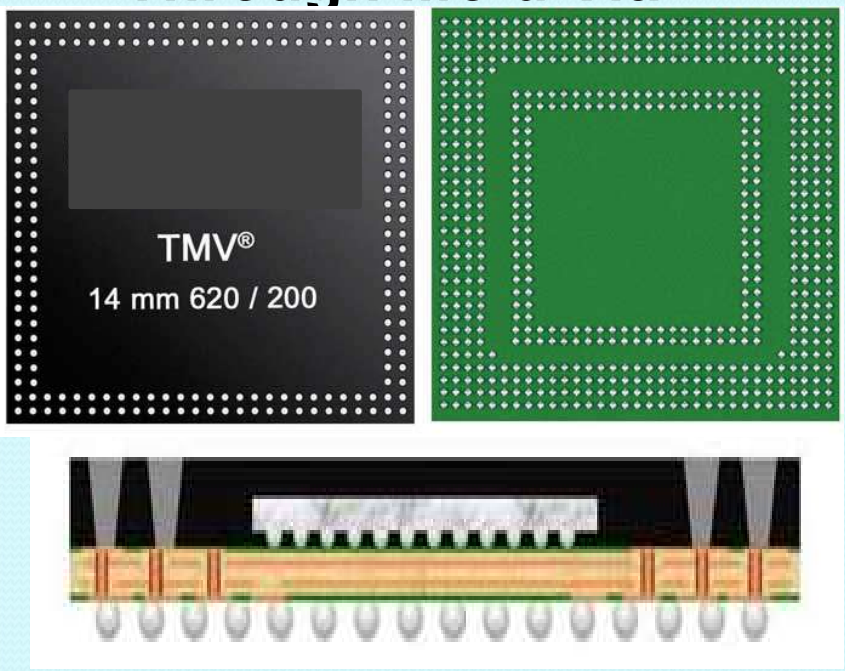
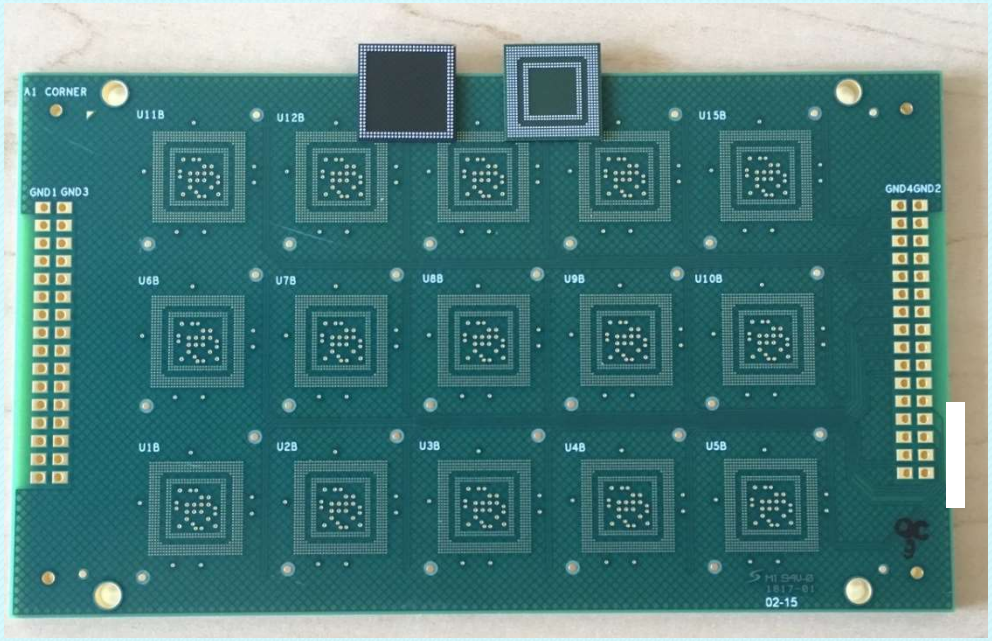
NEPP Packaging PoP Evaluation

PoP

Through Mold Via





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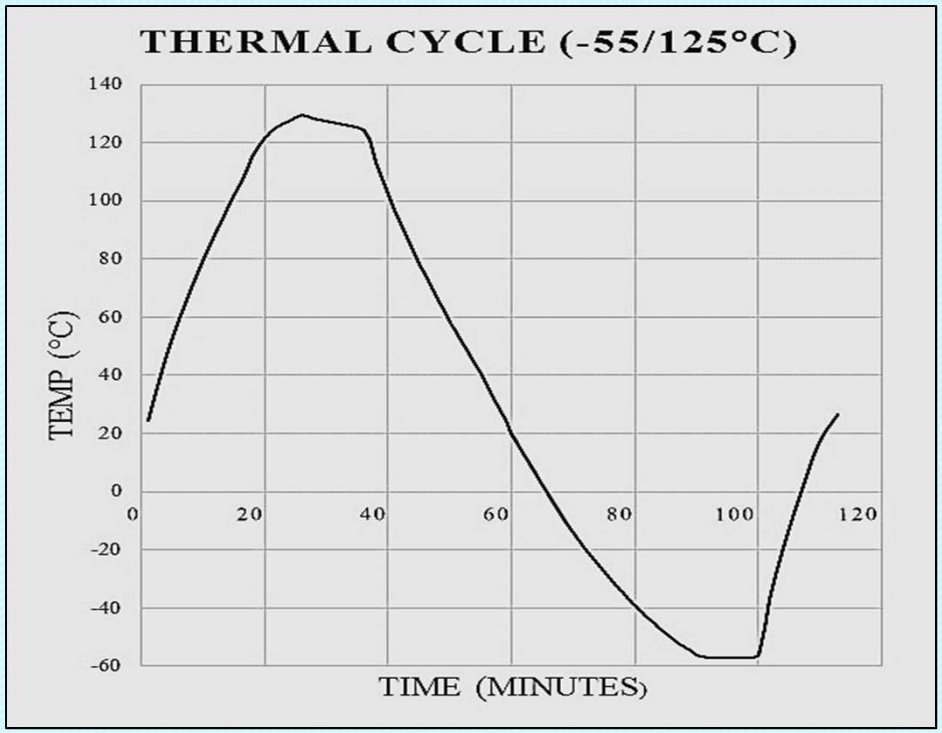
PoP Evaluation

Assemblies

- ✓ Top flux/Bottom SnPb paste onto PCB
- ✓ Top paste/Bottom SnPb paste onto PCB
- ✓ Top paste/Bottom SAC305 paste onto PCB
- ✓ Top paste reflowed. PoP onto SnPb paste onto PCB

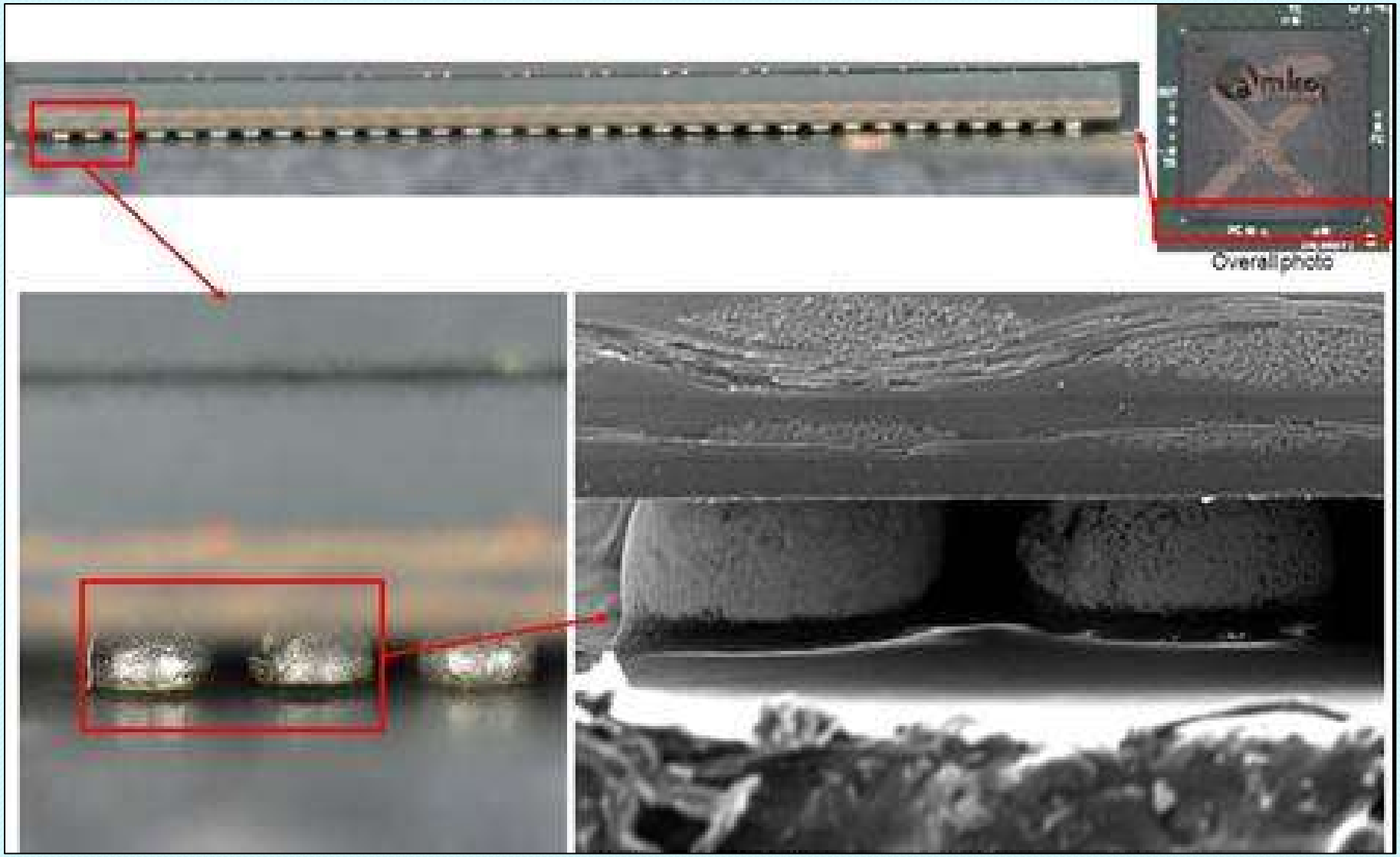
Thermal Cycles

- ✓ ATC, –55°C to 125°C
- ✓ ATSC, Shock cycles



PoP Evaluation

SEM Inspection after ATC



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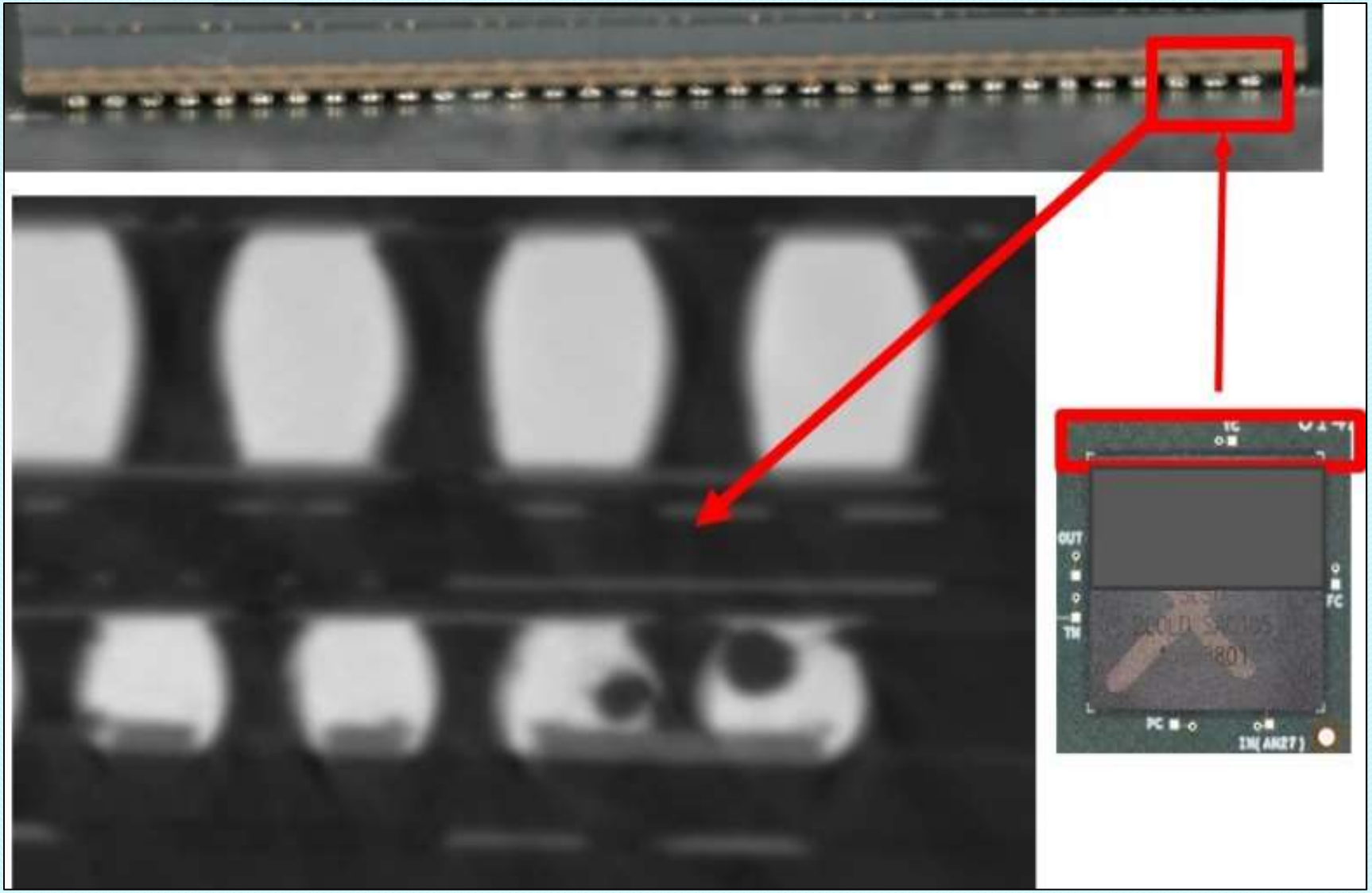
PoP Evaluation

3D X-ray Inspection after ATC



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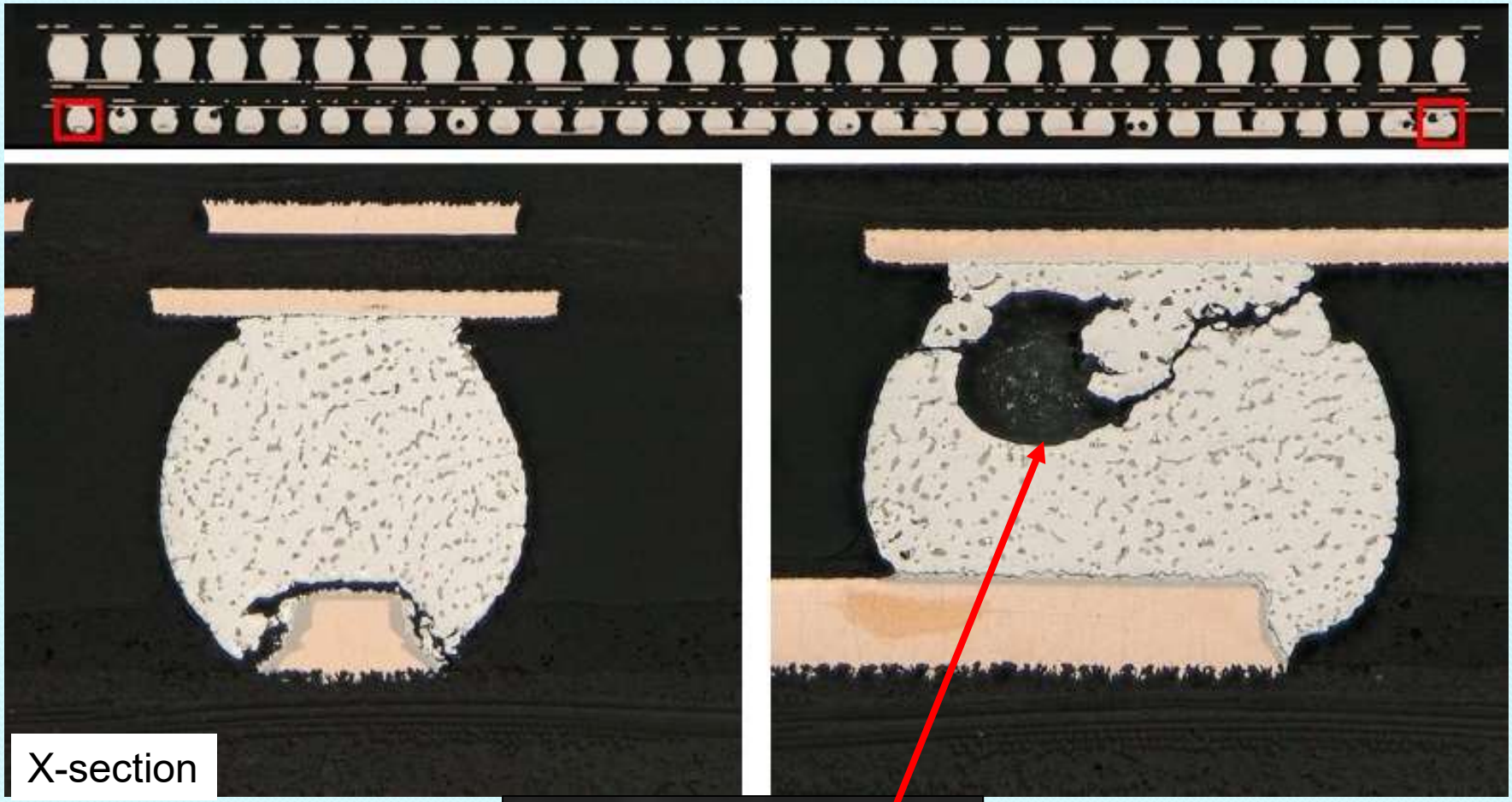
PoP Evaluation

X-section Verified



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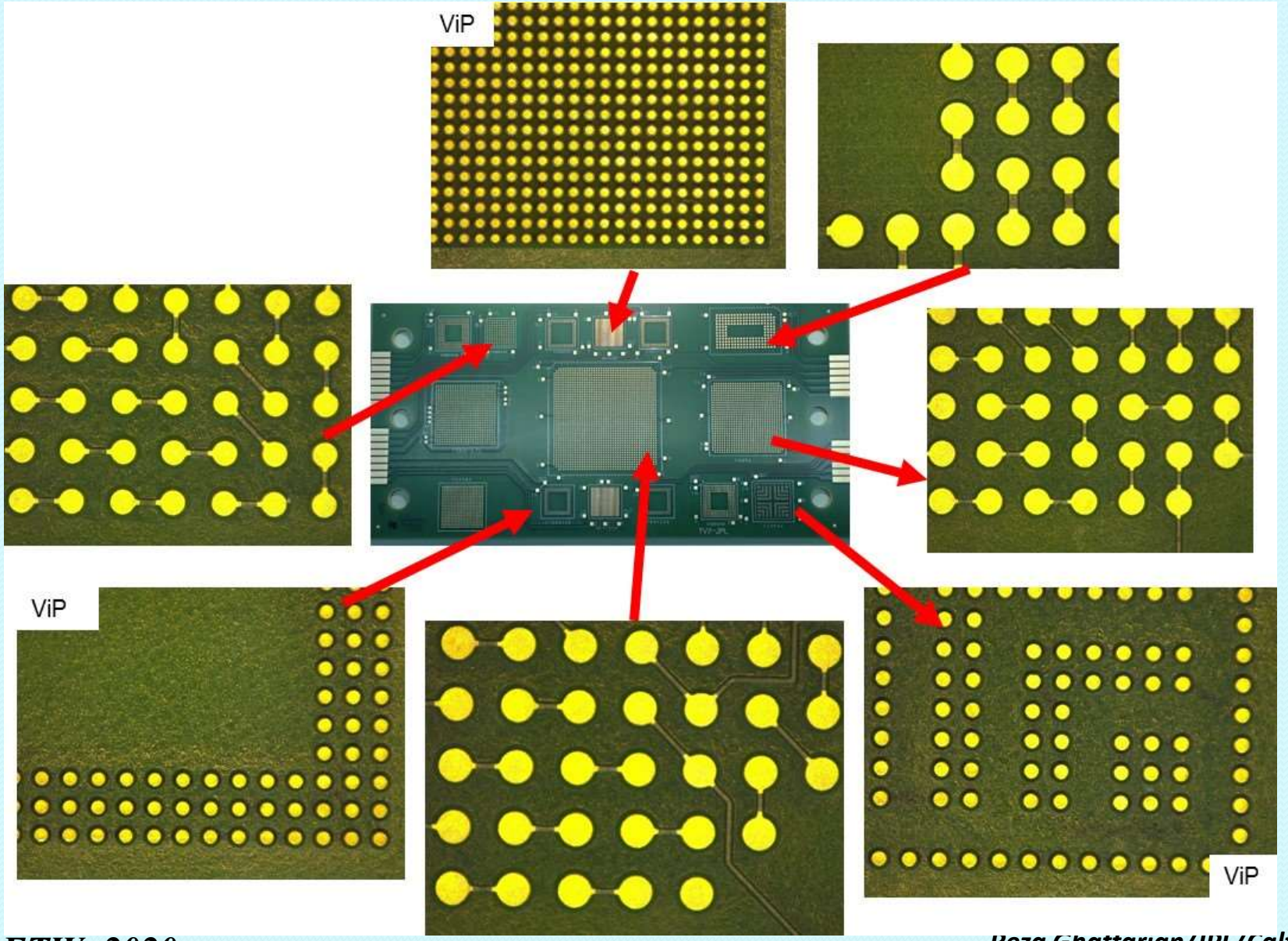
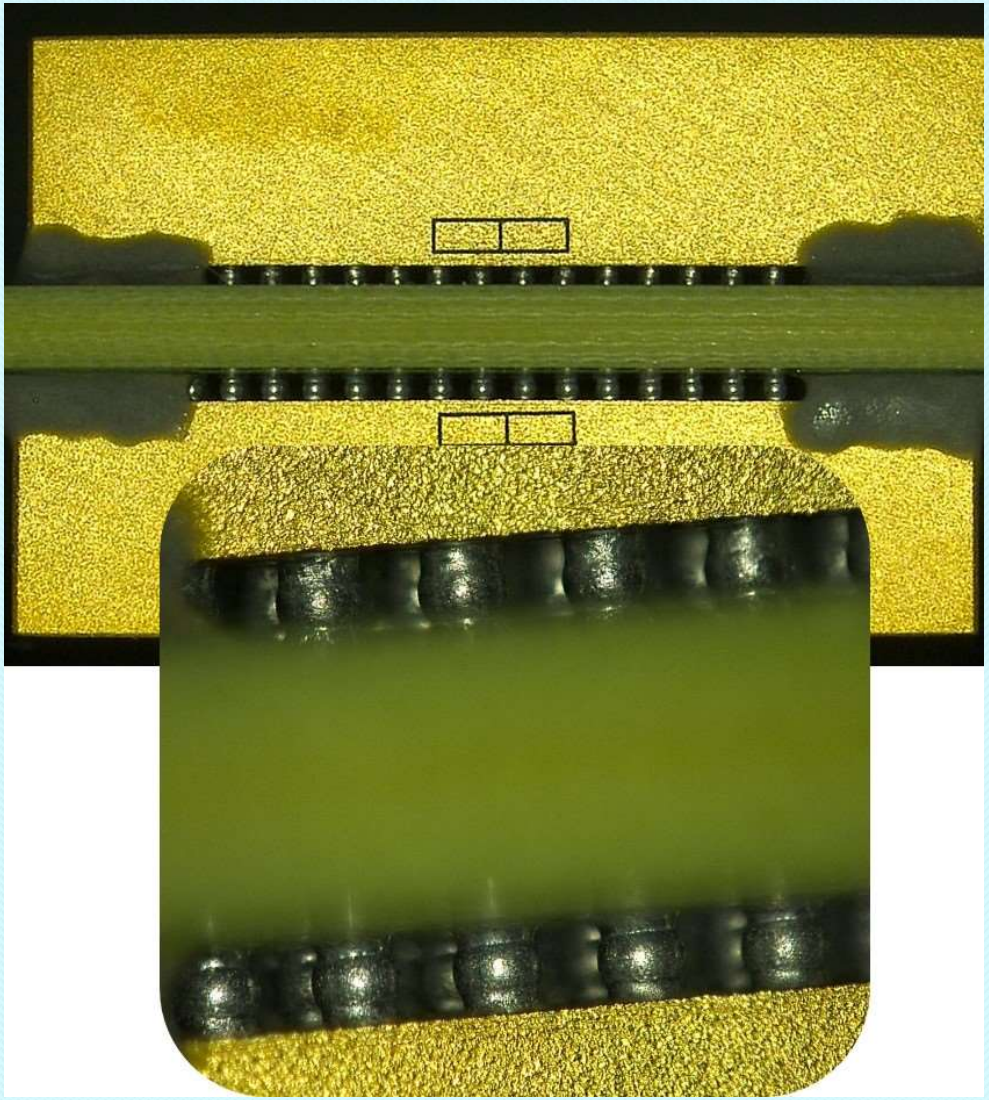
3D Evaluation

Area Array Packages



3D Evaluation

Single & Double-sided



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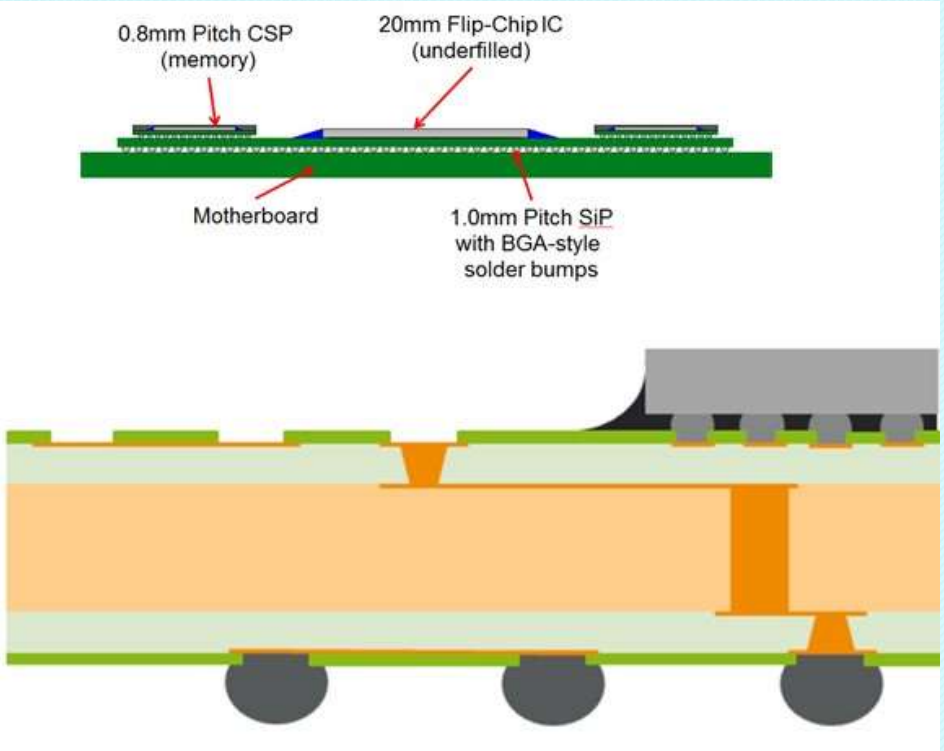
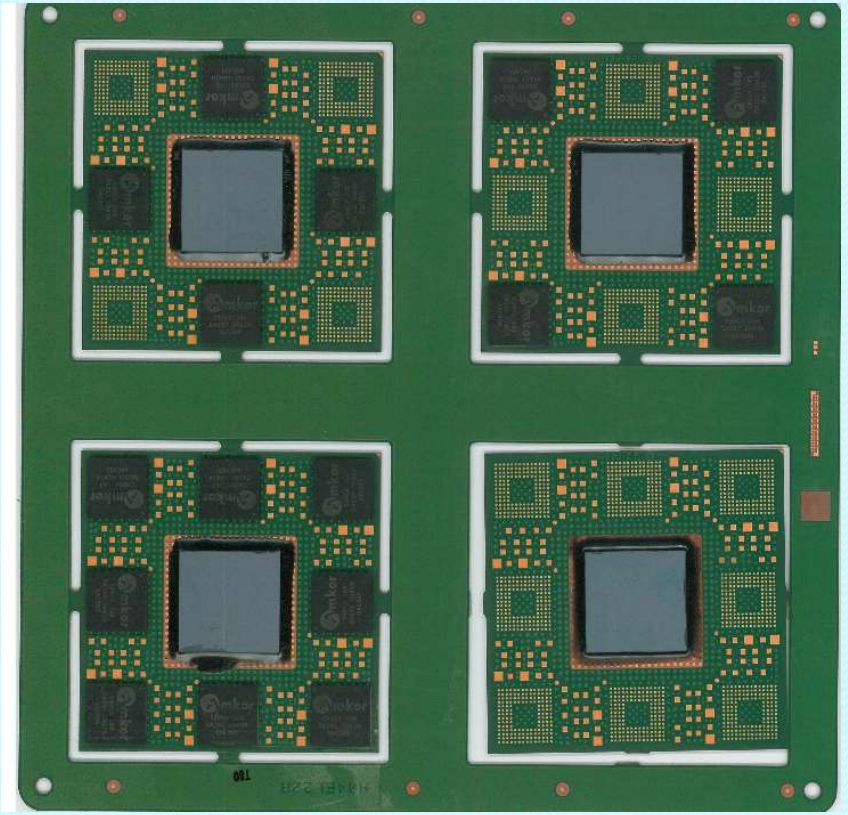
NEPP Packaging SiP Evaluations





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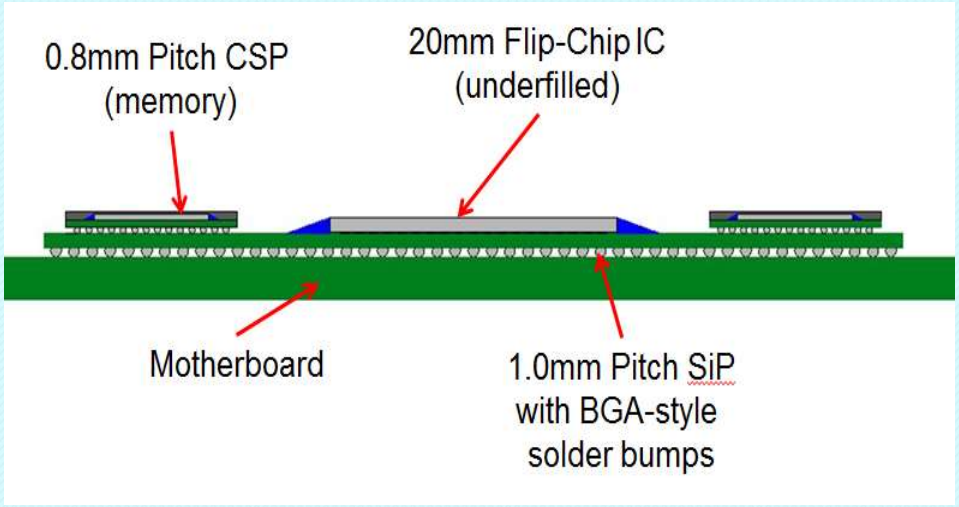
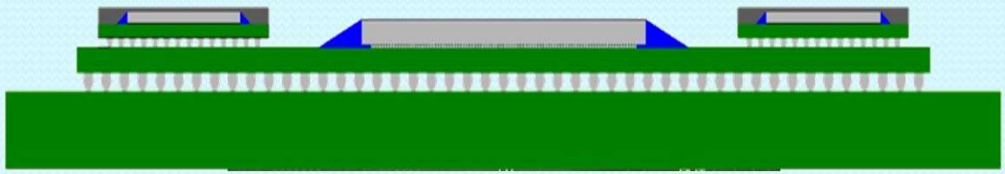
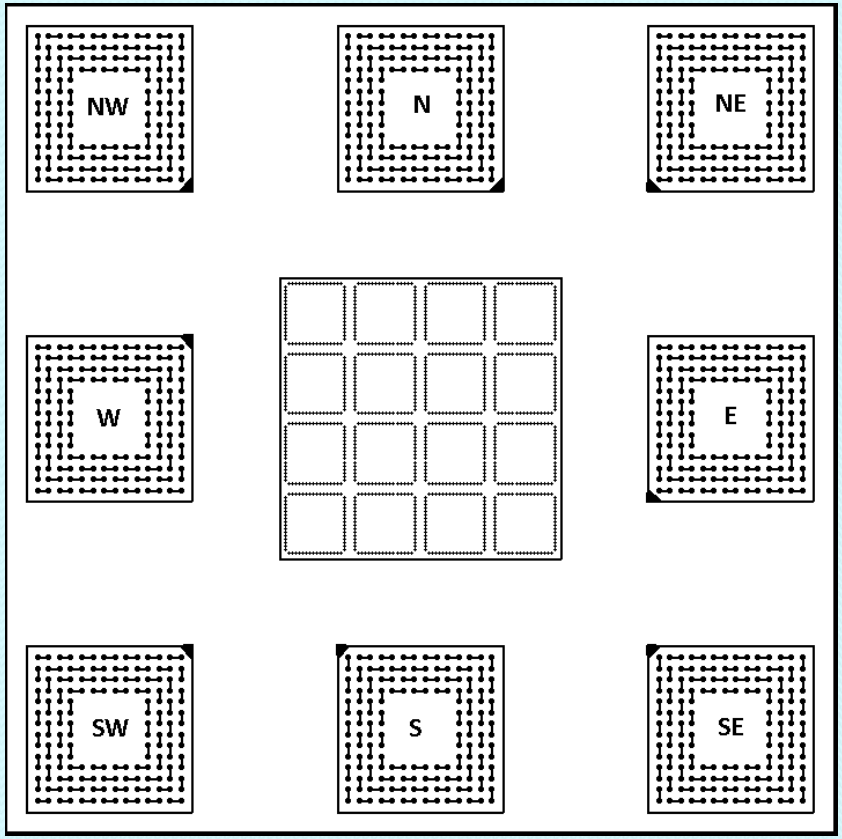
SiP TC Evaluation

- 8 CABGA 160 I/O, 12x12 mm, 0.8 mm pitch
- 1 flip-chip at the center (20x20 mm)
- SAC305 & SnPb, 3364 balls, 60x60 mm, 1.0-mm pitch







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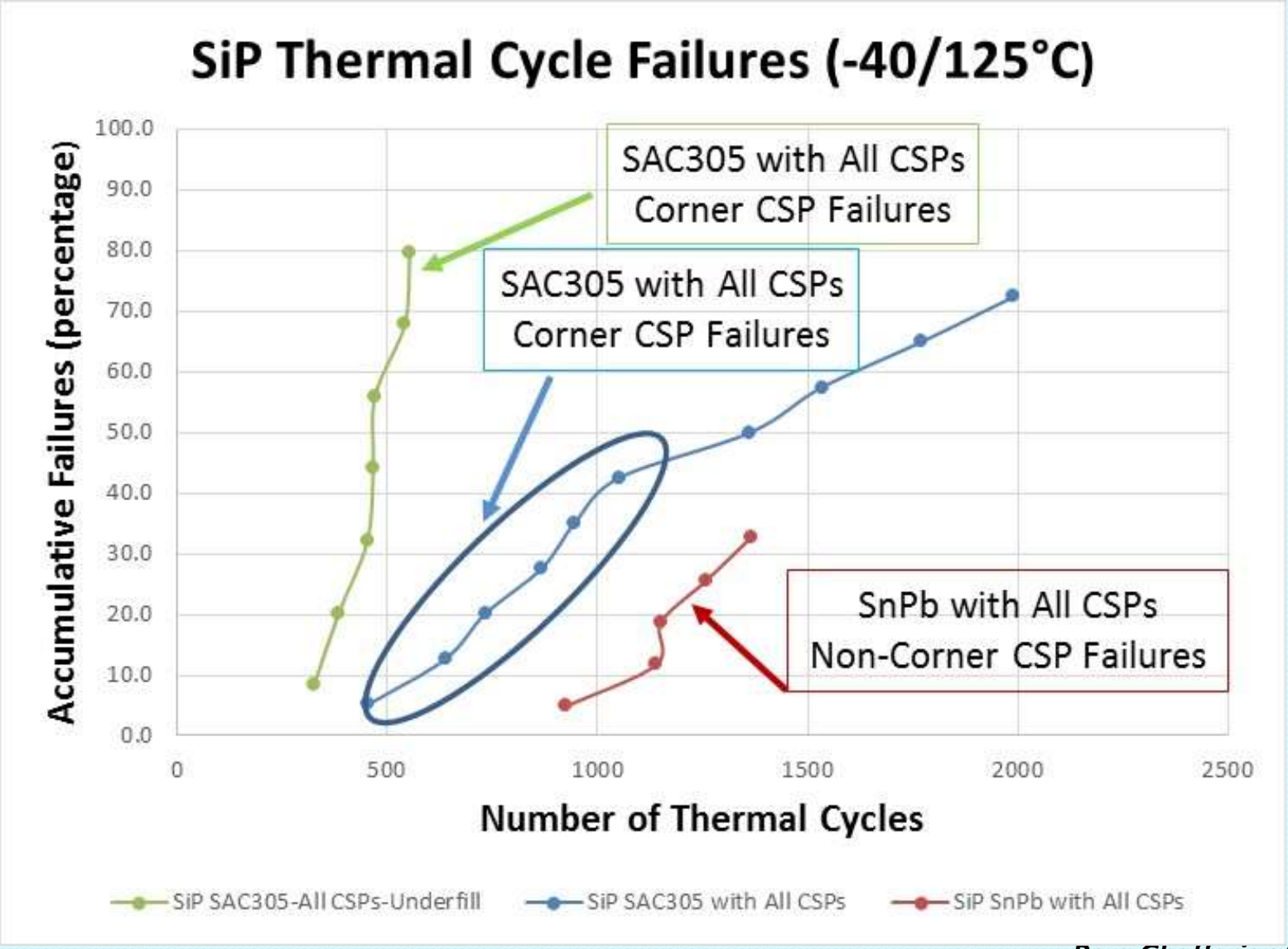
SiP TC Evaluation

Weibull Plots



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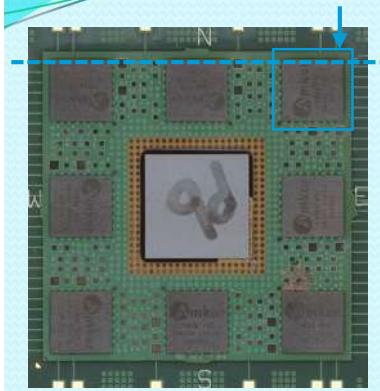
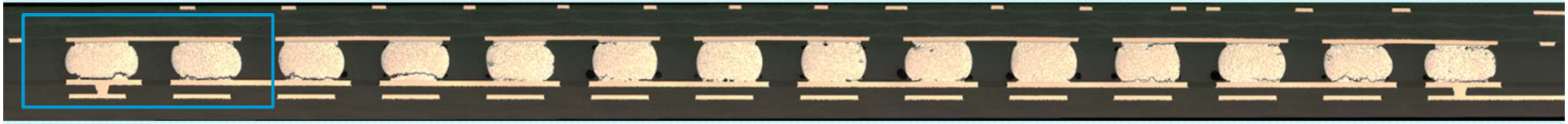
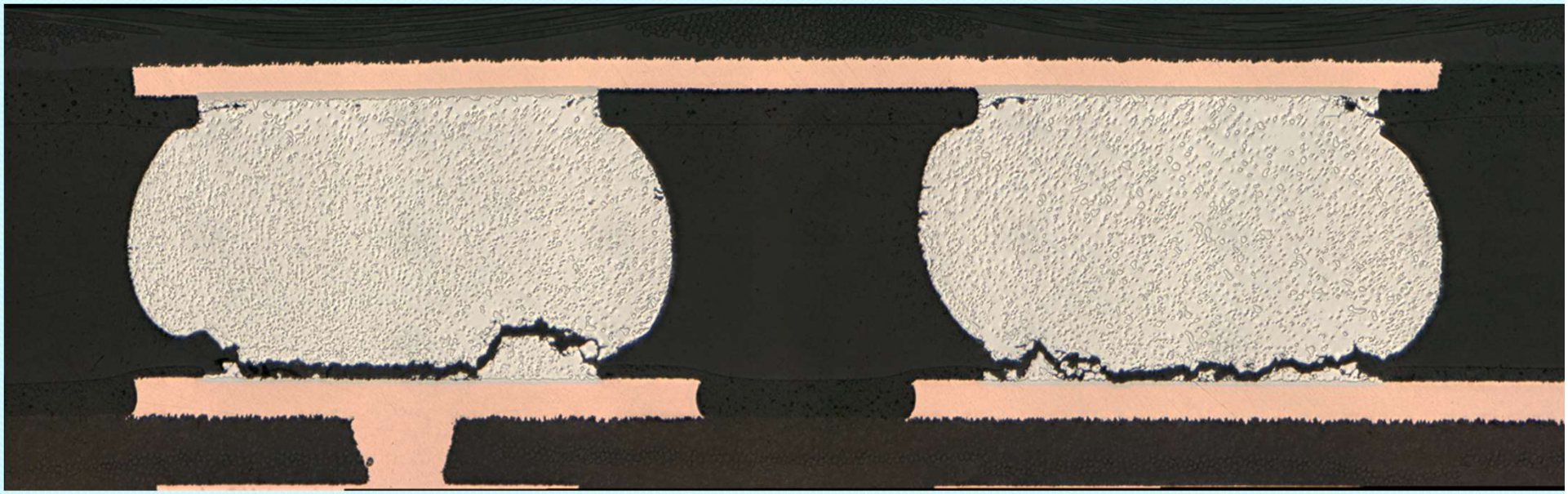
SiP Evaluation

Optical Images/X-section SiP SnPb with All CSPs

2838 Cycles (-40°C/125°C)







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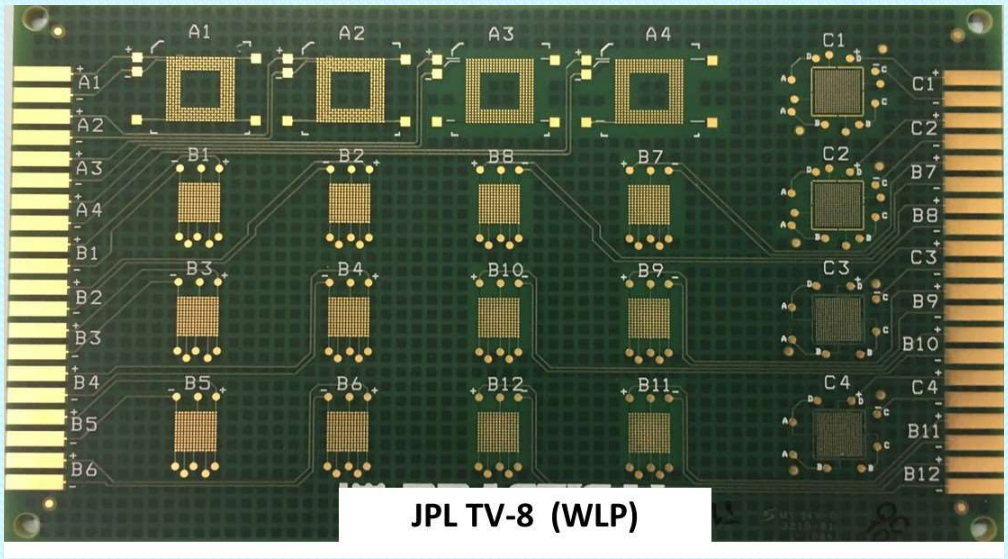
NEPP Packaging Single/3D TSV

WLP
PCB

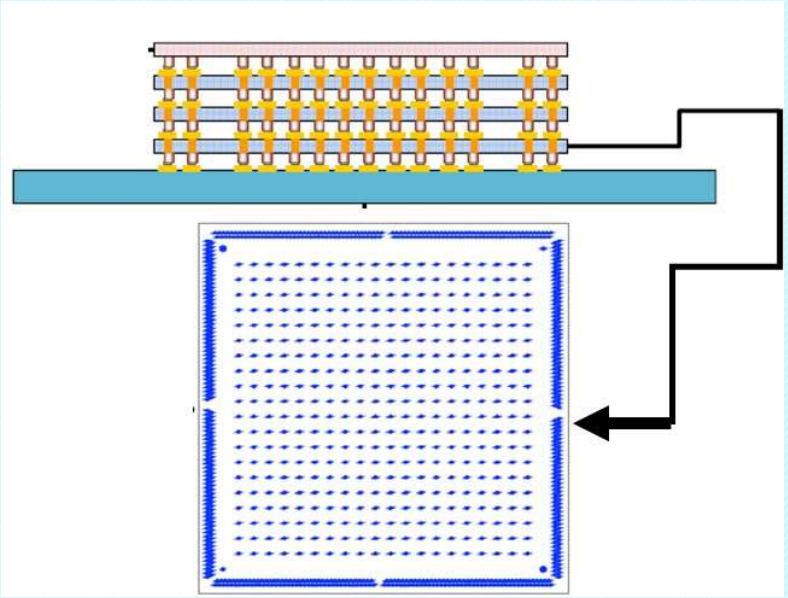
Fine Pitch BGA and WLP Onto Printed Circuit Board/PCB

2.5 D/SIP
Previous NEPP Report

3D TSV
Daisy-Chain Pattern



JPL TV-8 (WLP)



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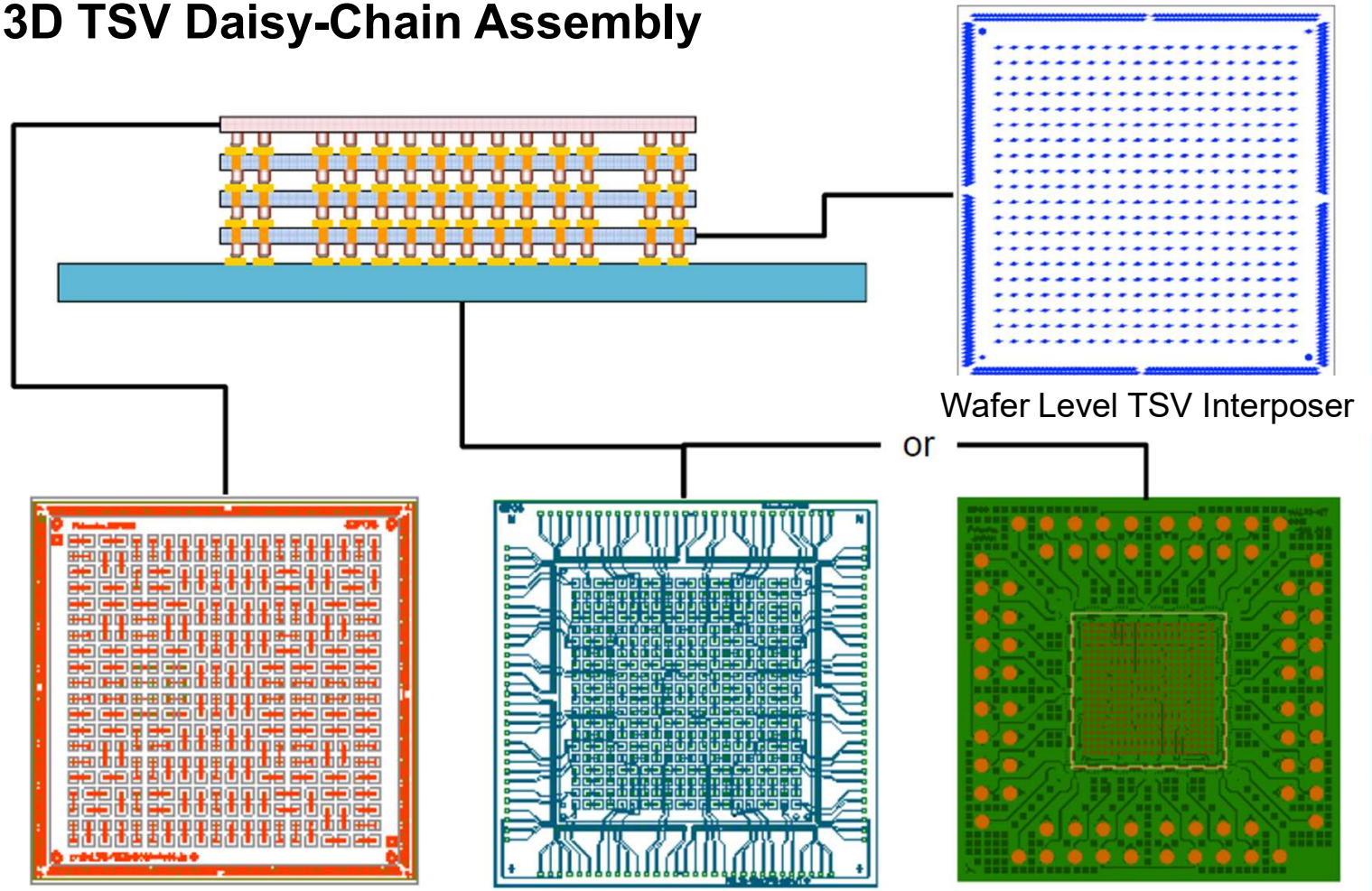
TSV Evaluation

Daisy-Chain Concept

3D TSV Daisy-Chain Assembly



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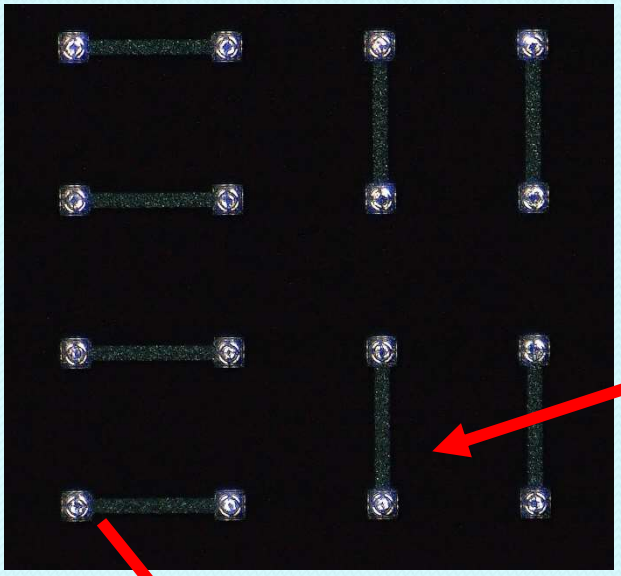
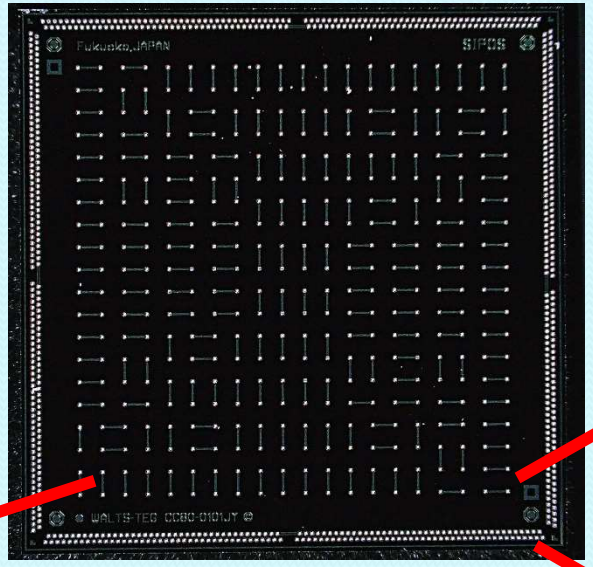
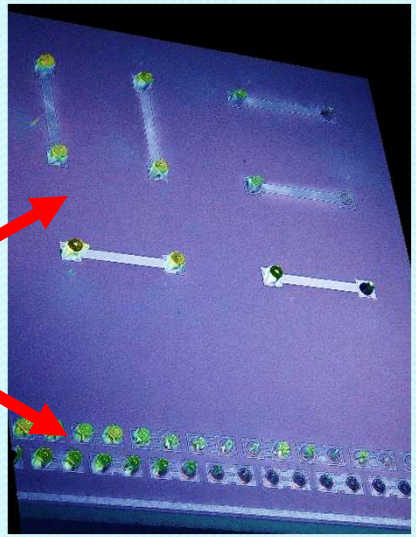
TSV Evaluation

Copper Pillar Daisy-Chain







Flip-Chip
Cu-pillar

Cu-pillar

Daisy-chain trace

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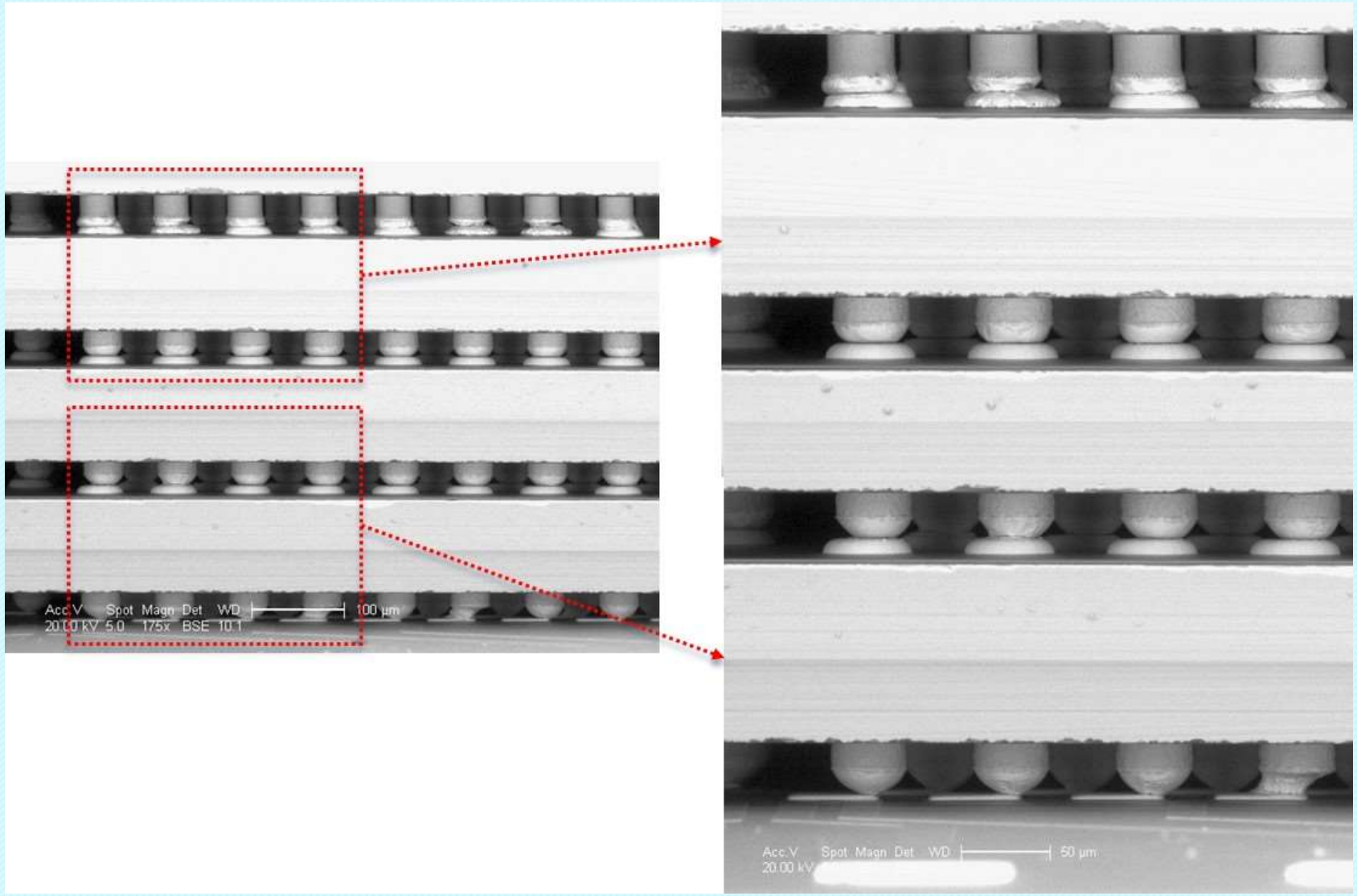
TSV Evaluation

3D Interposer Package Build Challenges



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Summary

- Reviewed NEPP Tasks on 2.5/3D Packaging
  - PoP/3D
  - SiP
  - TSV-Through Silicon Via Daisy-Chain Evaluation
- Evaluate PoP/3D Reliability under Thermal Cycling
  - No failure of 4 PoP assembly configurations
    - 200 thermal cycle (-55/125°C)
    - Bottom package failed first, failure from solder joint
  - No failure of 3D : Single and double-sided assemblies
    - 200 thermal cycles (-55/100°C)
  - Internally: Potential for Head-on-Pillow (HoP) failure
    - Daisy-chain drawback: No internal die
- SiP Reliability under Thermal Cycling
  - Warpage challenge for assembly and new finding on underfill effects
  - No failures to 200 thermal cycles (-40/125°C) of BGAs onto interposer or onto PCB
  - Weibull plots narrowed to show the effect of interposer's BGA underfill
- TSV Daisy-Chain Evaluation
  - Designed TSV daisy-chain for package build and assembly onto PCB
  - Characterize TSV and showed challenges in build with two interposers
  - Further evaluation both for package and PCB
- **Next**
  - **Optimization of TSV daisy-chain and reliability evaluation**

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Thank You!

Reza Ghaffarian/JPL/Caltech