Greetings from

Georgia Tech

3D Systems Packaging Research Center

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Georgia Tech
PACKAGING RESEARCH CENTER

Georgia Tech Institute for Electronics and Nanotechnology

Outline

- PRC – An Overview
- Heterogeneous Integration
- Glass Interposer Technology
- Glass Interposers for Space Applications
- Summary

Packaging Research Center (PRC)

Graduated NSF Engineering Research Center

26 Faculty (ECE, MSE, ChE, ME)

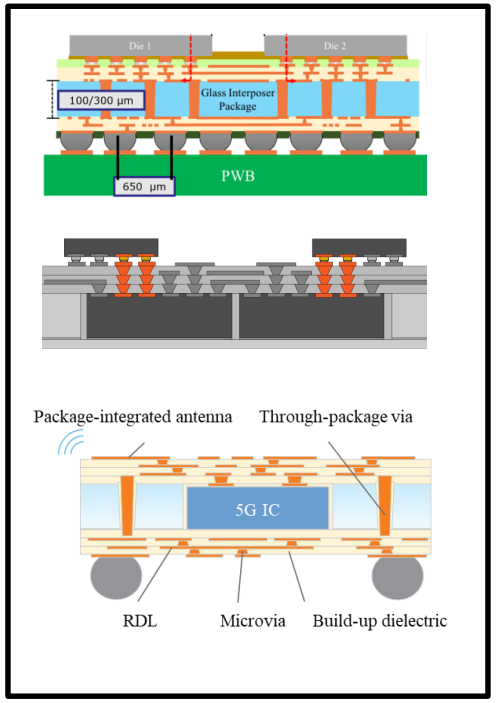
11 Staff (Research & Admin)

40+ G Students (+ UG)

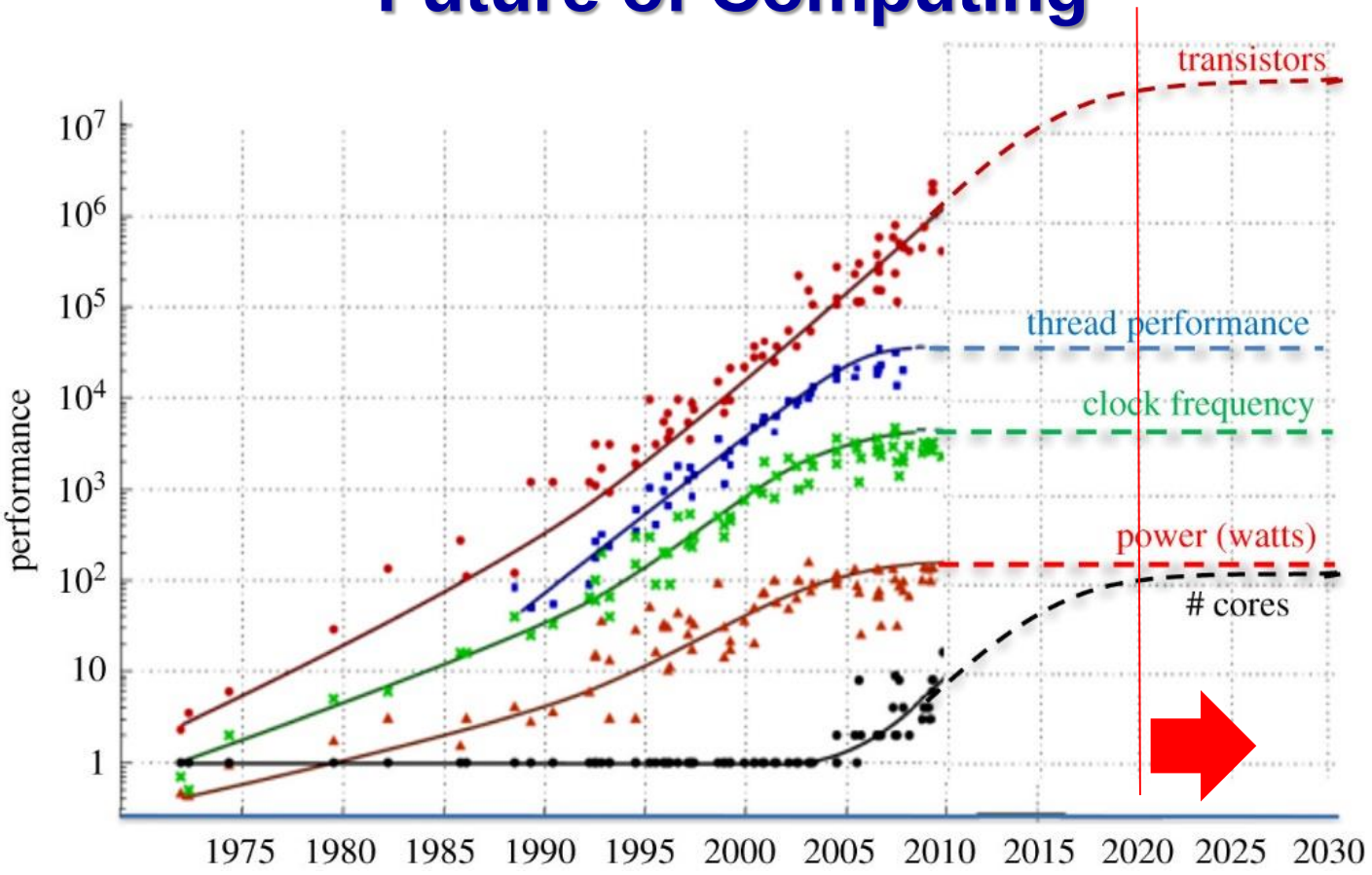
33 Collaborators (Industry/Govt. Labs)

3 Visiting Engineers on Campus

Advanced Packaging & System Integration



Future of Computing

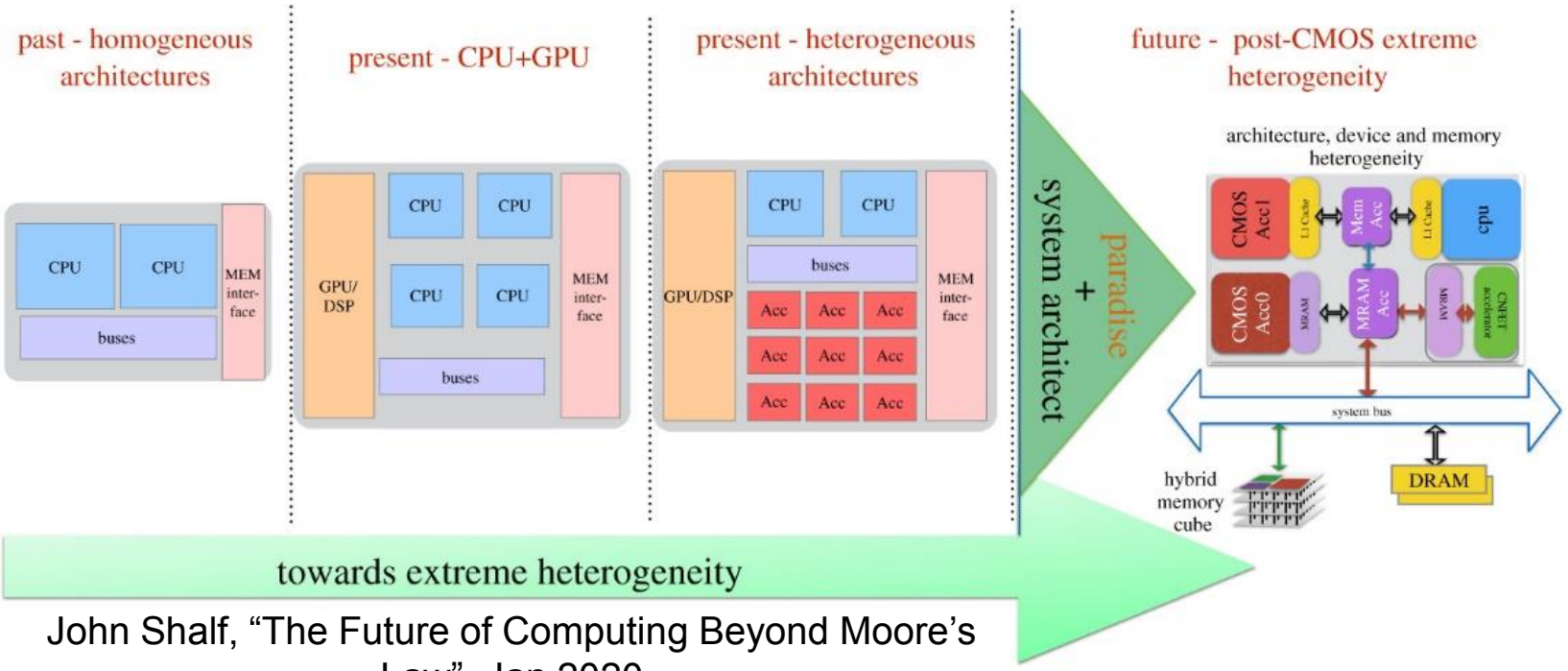


Moore's Law slowing down

John Shalf, "The Future of Computing Beyond Moore's Law", Jan 2020
https://doi.org/10.1098/rsta.2019.0061

- ❑ Path Forward
  - More efficient architectures & advanced packaging (next 10 years)
  - New materials & devices (20+ years)
  - New models for computation (Future ex: quantum computing)

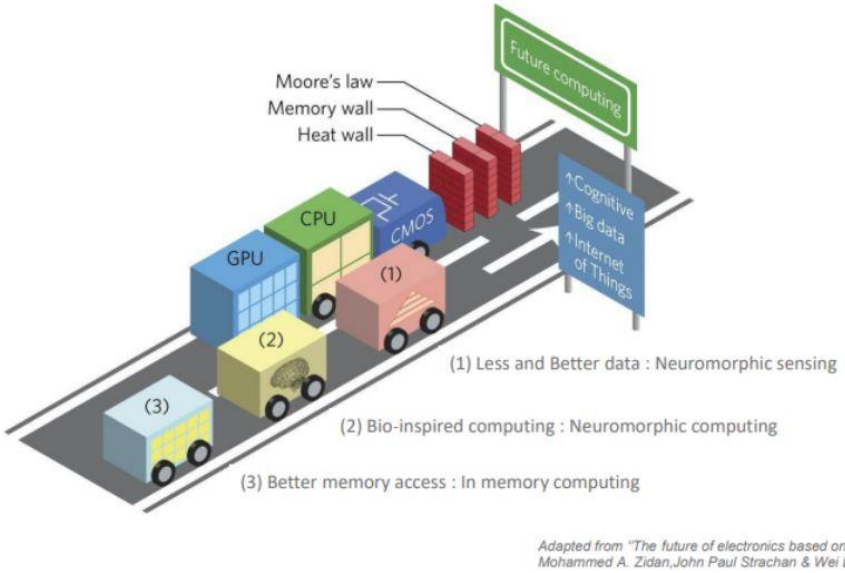
Future of Computing (cont.)



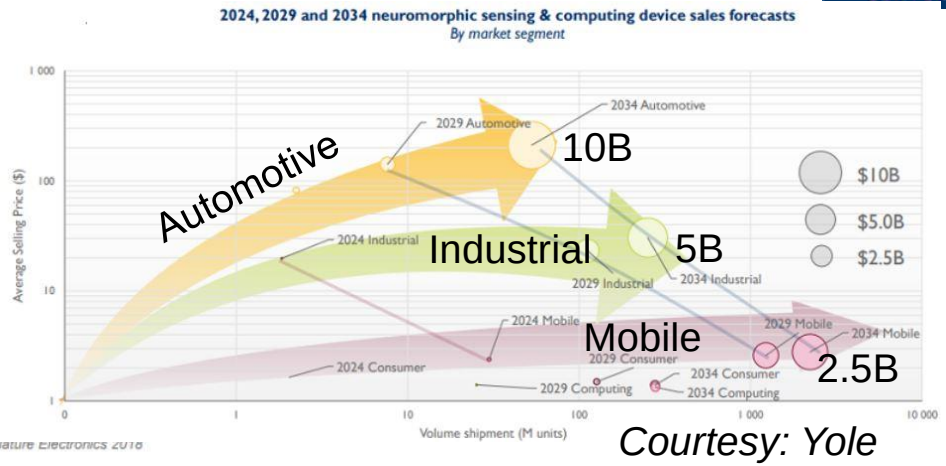
John Shalf, "The Future of Computing Beyond Moore's Law", Jan 2020

- ❑ Architectural innovations
  - Use of <u>Accelerators</u> (chiplets in-between a CPU & ASIC with IP Reuse)
- ❑ Extreme Heterogeneity
  - <u>Smaller Dies</u> from different advanced process nodes to reduce die cost
- ❑ Data movement
  - <u>Low</u> Energy/Bit (EPB) with <u>high</u> Bandwidth density

Artificial Intelligence

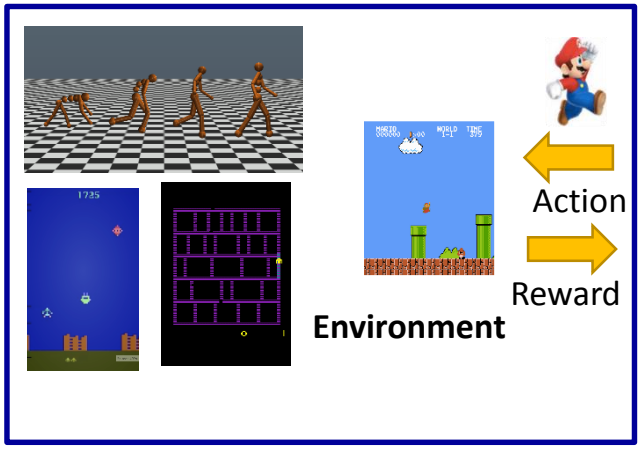


Adapted from "The future of electronics based on memri
Mohammed A. Zidan,John Paul Strachan & Wei D. Lu, Nature Electronics 2018



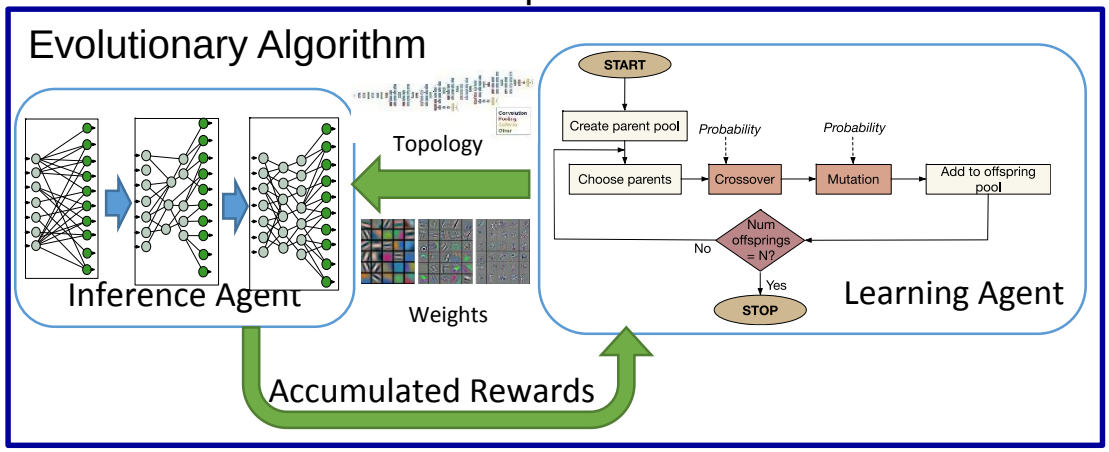
Courtesy: Yole

Wireless



Data Movement: Long Distances

Compute



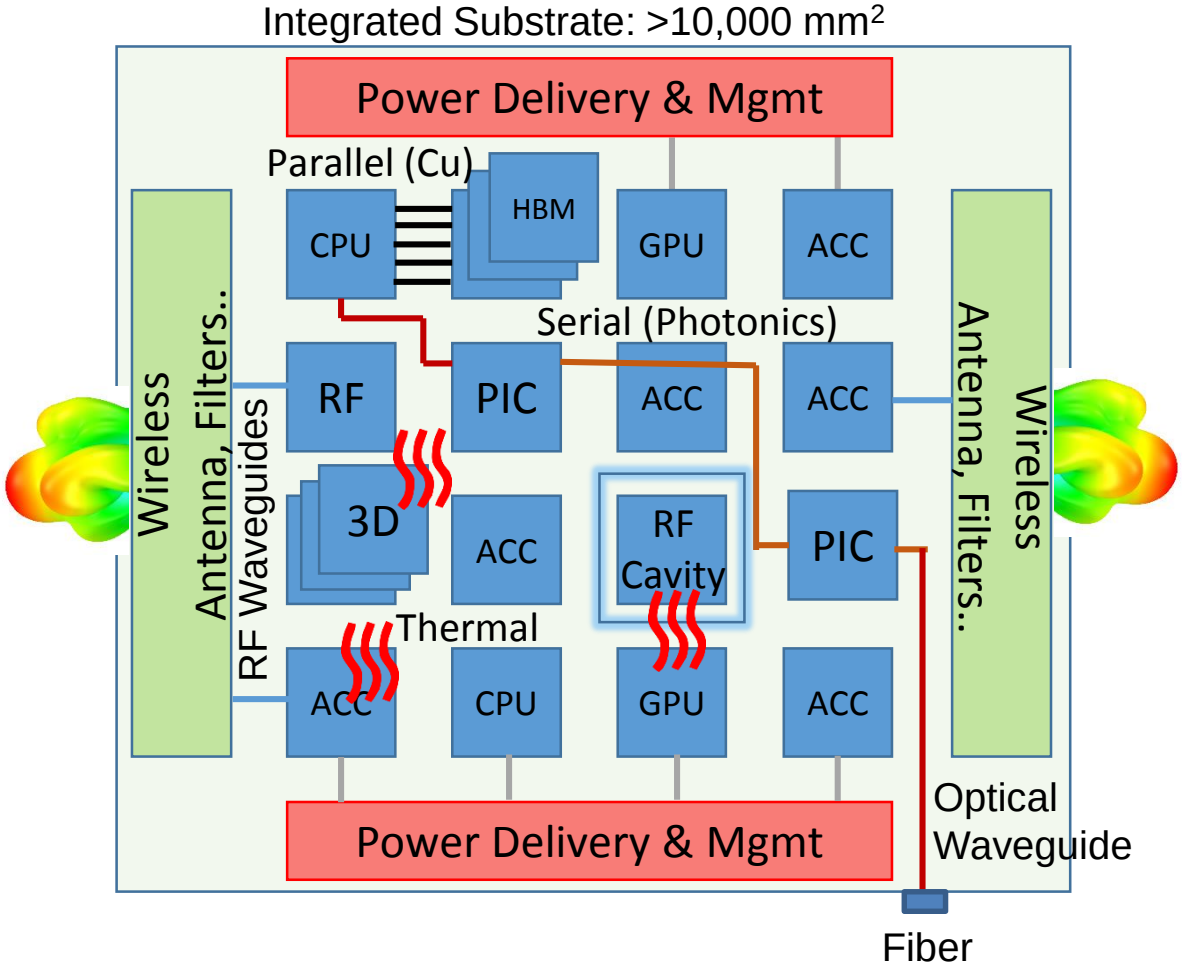
Data Movement: Short Distances

Courtesy: T. Krishna, GT

- Challenge: Digital & Wireless Integration on a Single Module

Heterogeneous Integration

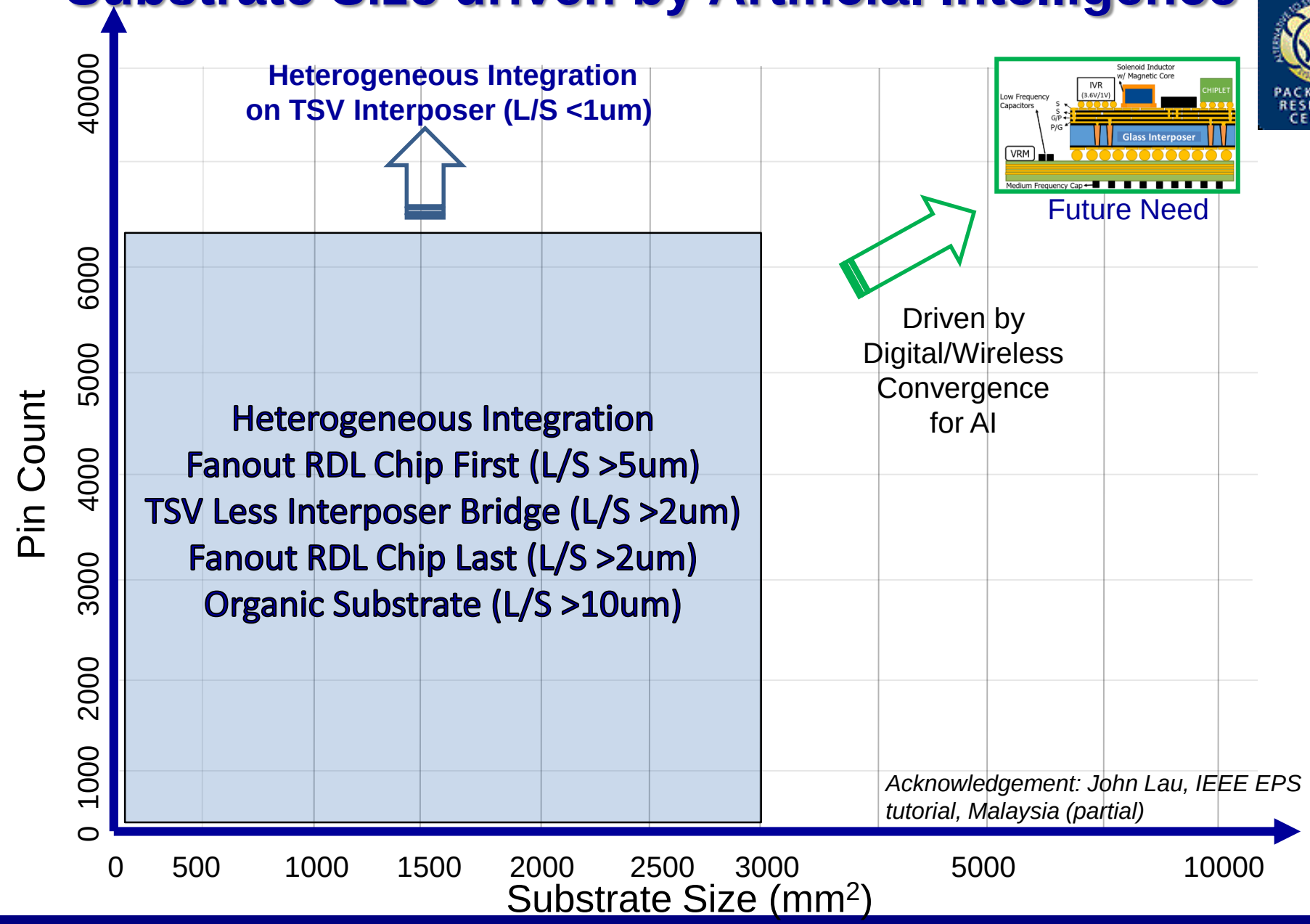
- Multitude of chips from different process nodes, wafer sizes, foundries & domains



- Compute
  - Electronics
    - Parallel I/O
    - High BW Density
    - <3mm length
  - Photonics
    - Serial I/O
    - High BW
    - >200mm length
- Wireless
  - Massive MIMO
    - High Data Rate
    - >20m

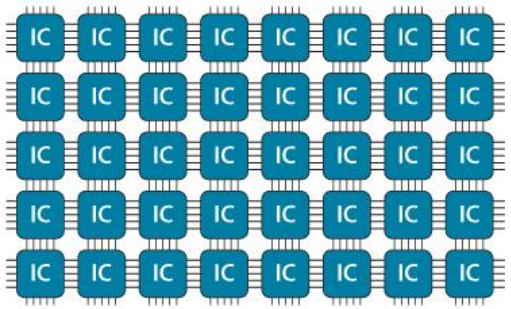
HETEROGENEOUS INTEGRATION ENABLES CONTINUATION OF MOORE'S LAW

Substrate Size driven by Artificial Intelligence



Acknowledgement: John Lau, IEEE EPS tutorial, Malaysia (partial)

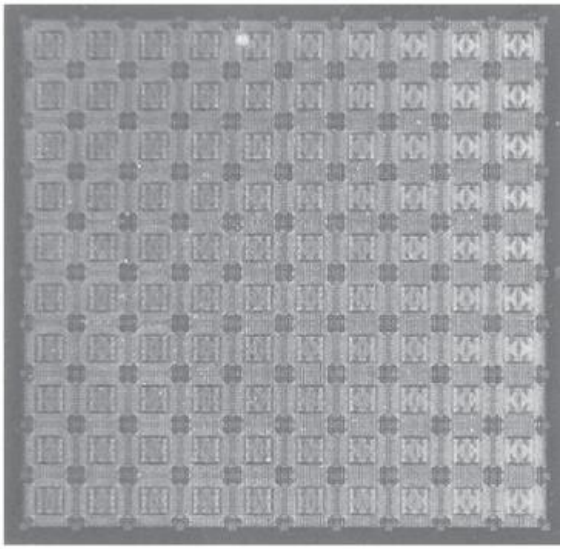
Technology for Digital/Wireless Convergence



Dense Connectivity between ICs

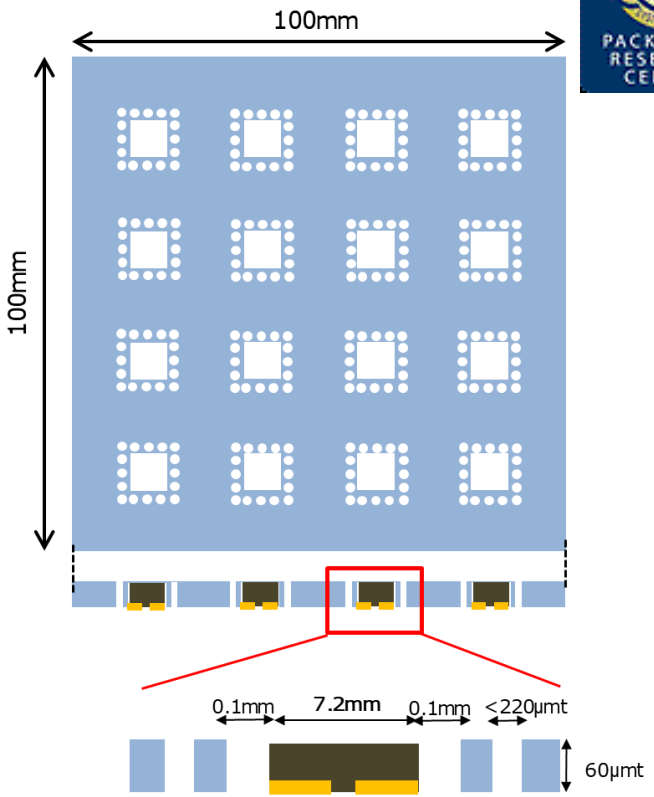
Rao. R. Tummala, McGraw Hill, 2019.

61-Layer LTCC/Cu-MCM (IBM,1992)



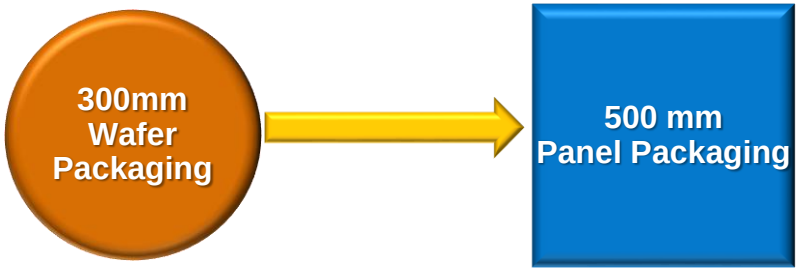
Multi-chip Module (MCM)
Single CPU

Glass Interposer



Silicon Interposer

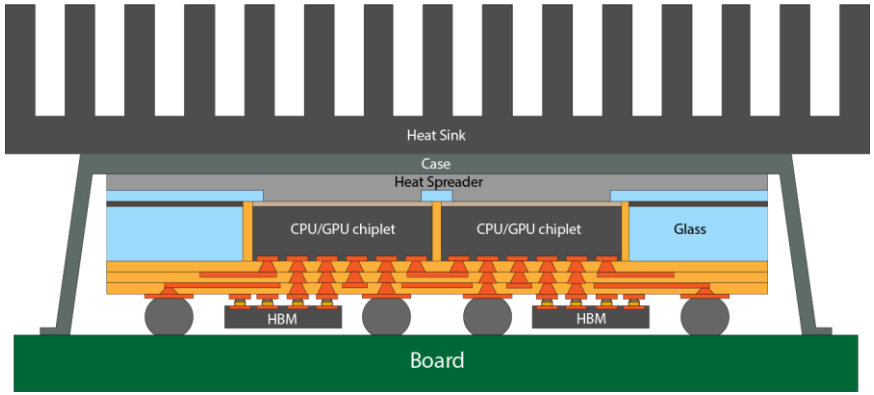
- 100mm size on a wafer too expensive



Glass Interposer

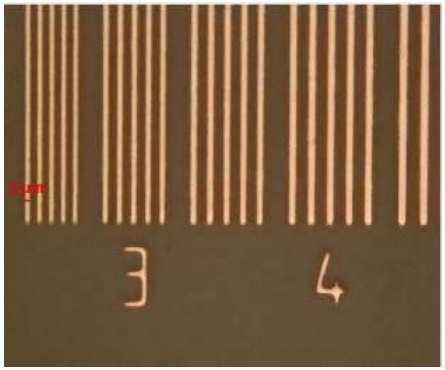
- 100mm size on a panel cost effective

High Density Connectivity between Chips



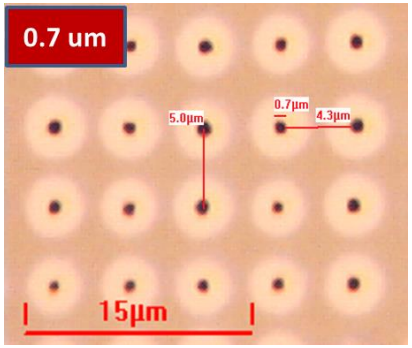
L/S/Via = 1/1/1 um

Semi-Additive Process



1um/1um 2um/2um 3um/3um

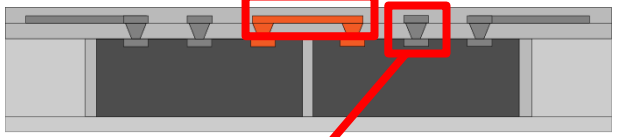
Microvia



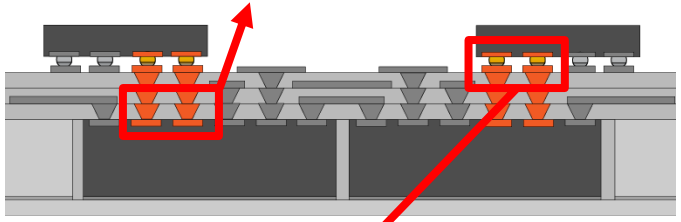
0.7um/5um pitch

Chip First

High-density RDL characterization
- 2-5 µm microstrip lines, 3 different dK
- 2-5 µm L/S coupled MS lines
- 0.25 – 5 mm long lines



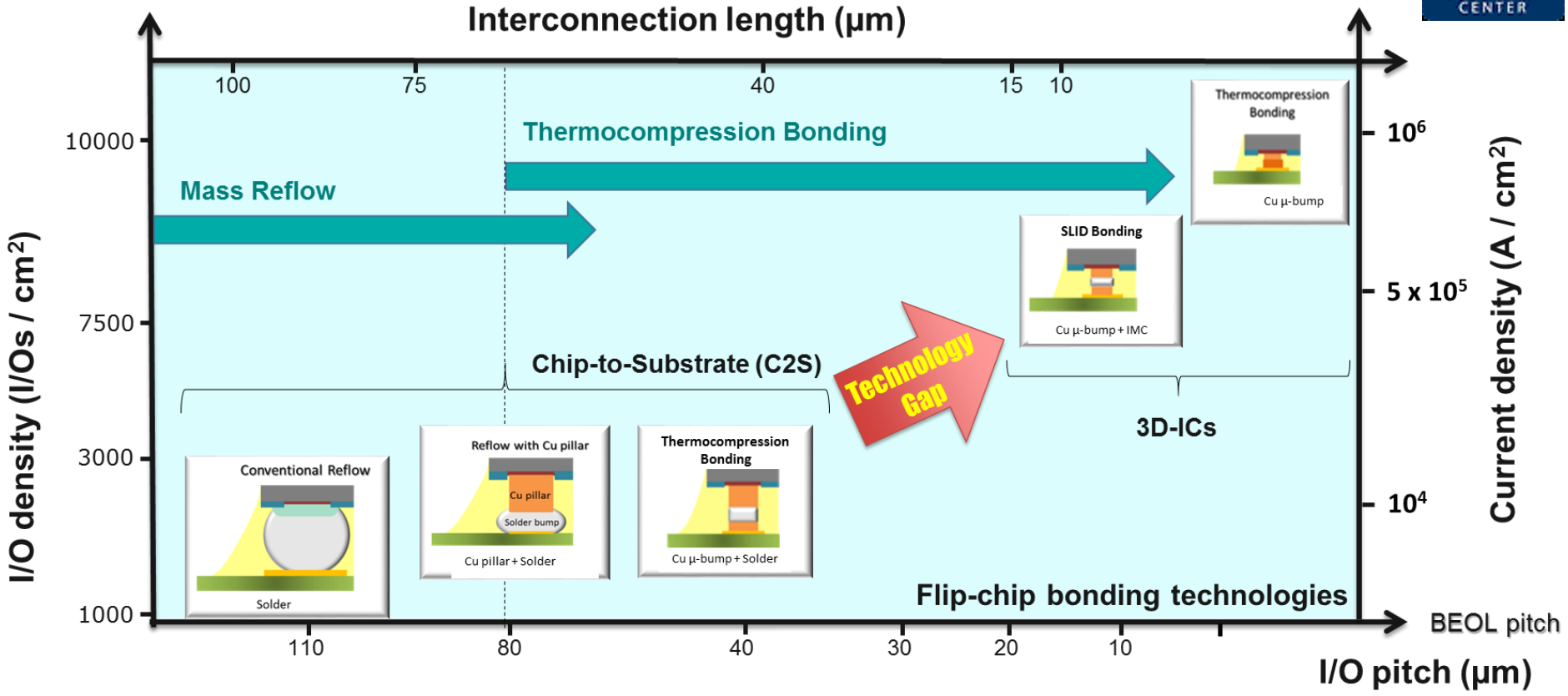
Chip-PKG Microvia characterization
- 3-10 µm via, 7-20 µm pad
- Impact of pad size, via diameter, via pitch



Assembly bump characterization
- 35 µm pitch, 20 µm dia Cu-SnAg bumps

Courtesy: Siddharth Ravichandran, PRC
Fuhan Liu, PRC

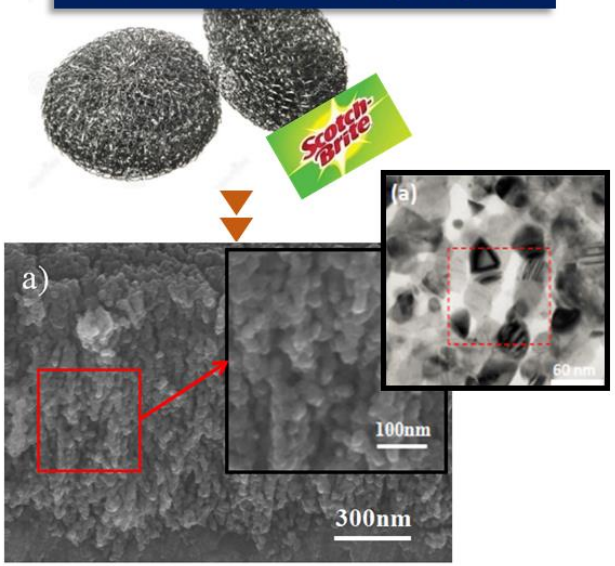
Assembly….Closing the Gap



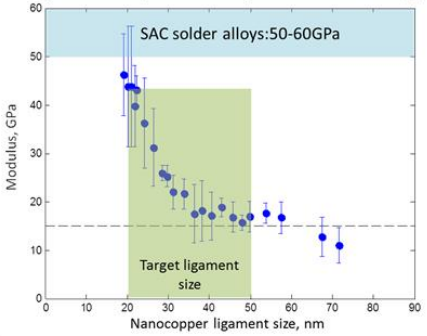
- Sn-based lead-free solders are reaching their limits in pitch scalability, power handling capability and creep resistance → **direct Cu-Cu bonding** as next interconnection node
- **Non-coplanarities** are a key bottleneck for development of a universal assembly solution

Nanoporous-Cu Film Sintering Assembly Pitch < 20μm

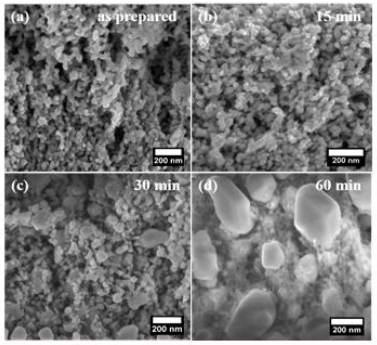
Nanoporous (NP) Cu: nanoscale metal sponges



High compliance pre-sintering

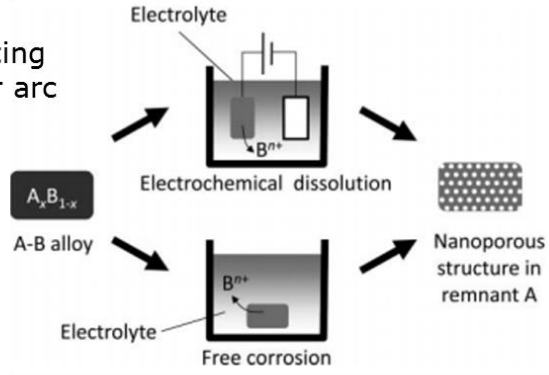


Controlled densification

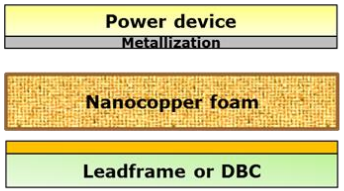


Low-cost synthesis by selective etching

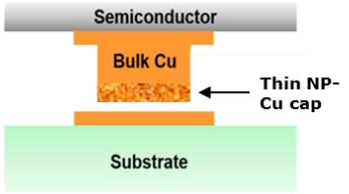
- Electroplating
- Furnace or arc melting

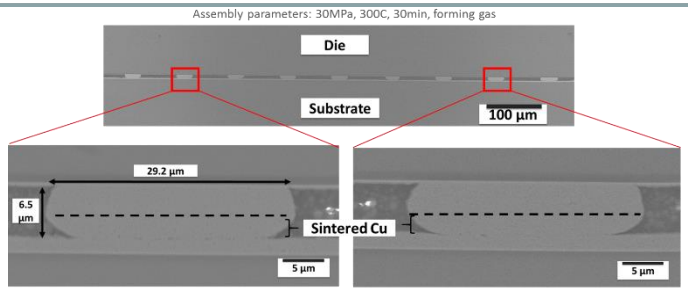


Die-attach films, inserts or preforms



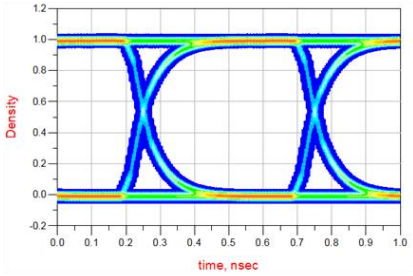
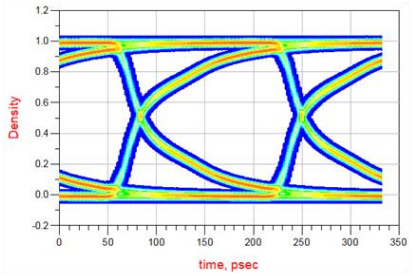
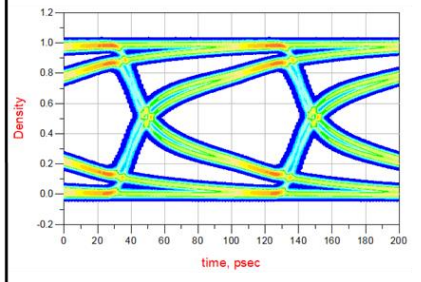
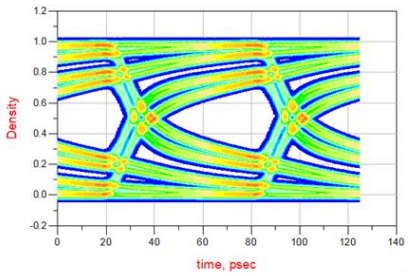
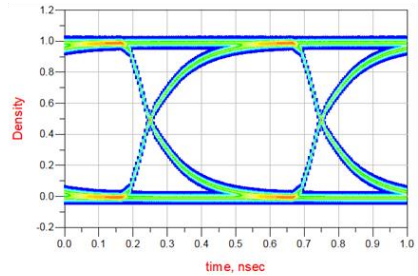
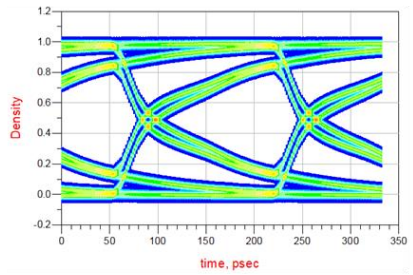
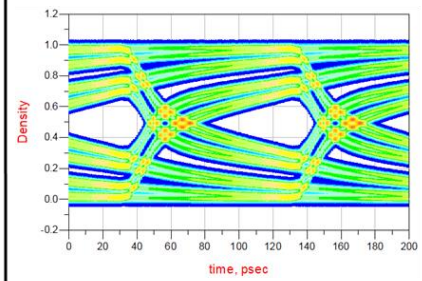
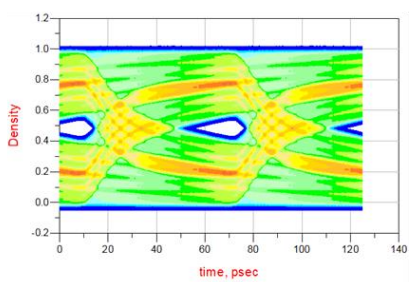
Cu pillar with NP-Cu caps (semi-additive processing)





Courtesy: Vanessa Smet, PRC

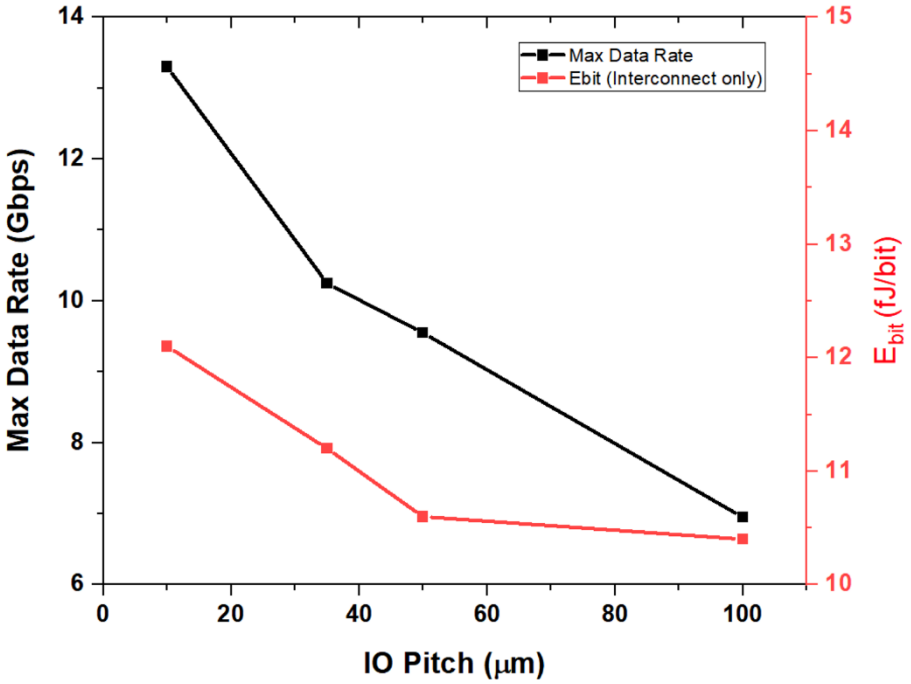
Comparison of Glass & Silicon Interposer

	2 Gbps	6 Gbps	10 Gbps	16 Gbps
Glass				
	Eye Width = 97 %UI Eye Height = 0.91 V	Eye Width = 93.5 %UI Eye Height = 0.78 V	Eye Width = 85.5 %UI Eye Height = 0.59 V	Eye Width = 73.5 %UI Eye Height = 0.38 V
Silicon				
	Eye Width = 95.5 %UI Eye Height = 0.89 V	Eye Width = 77.5 %UI Eye Height = 0.55 V	Eye Width = 55.5 %UI Eye Height = 0.25 V	Eye Width = 24.5 %UI Eye Height = 0.07 V

Simulation settings:

- Statistical simulation at BER = 1E-12
- Rise/Fall Time = 10 %UI
- TX Impedance = 50 Ω
- RX termination at μ-bumps
- Channel length = 6 mm
- Bump Pitch/Diameter = 55/20 um
- Line Width/Spacing/Thickness = 2 um

Energy Per Bit & Bandwidth Density



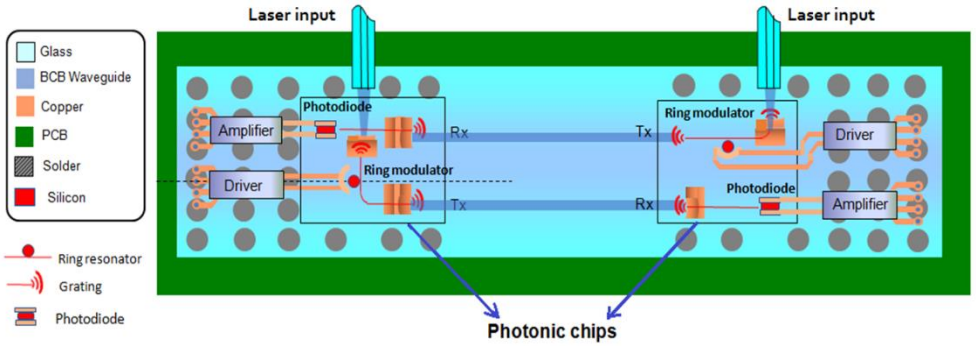
	3D IC w/ TSV [Zhang, et al. '18]	Monolithic 3D [Zhang, et al. '18]	3D GPE (35 μm Pitch)
Bandwidth density	1.76 Tbps/mm^2	12.625 Tbps/mm*	4.65 Tbps/mm^2
ESD capacitor	50fF	50fF	0.5 pF
E_{bit} (no ESD)	76.2 fJ/bit	3.7 fJ/bit	11.2 fJ/bit
E_{bit} (with ESD)	176.2 fJ/bit	135.1 fJ/bit	1.01 pJ/bit

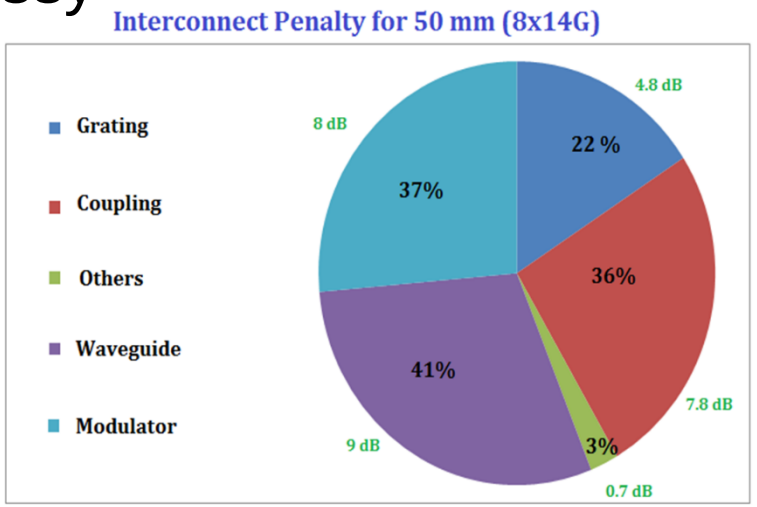
GPE: Glass Panel Embedded

- E_{bit} only includes interconnect. The ESD capacitances based on model assumptions add 1 pJ/bit
- E_{bit} increases with decreasing pitch due to increased mutual capacitance between IOs

Computing – Photonics Interconnects

- Fine Pitch Cu Interconnects too lossy
- Photonics in the Module
- Emerging Technology

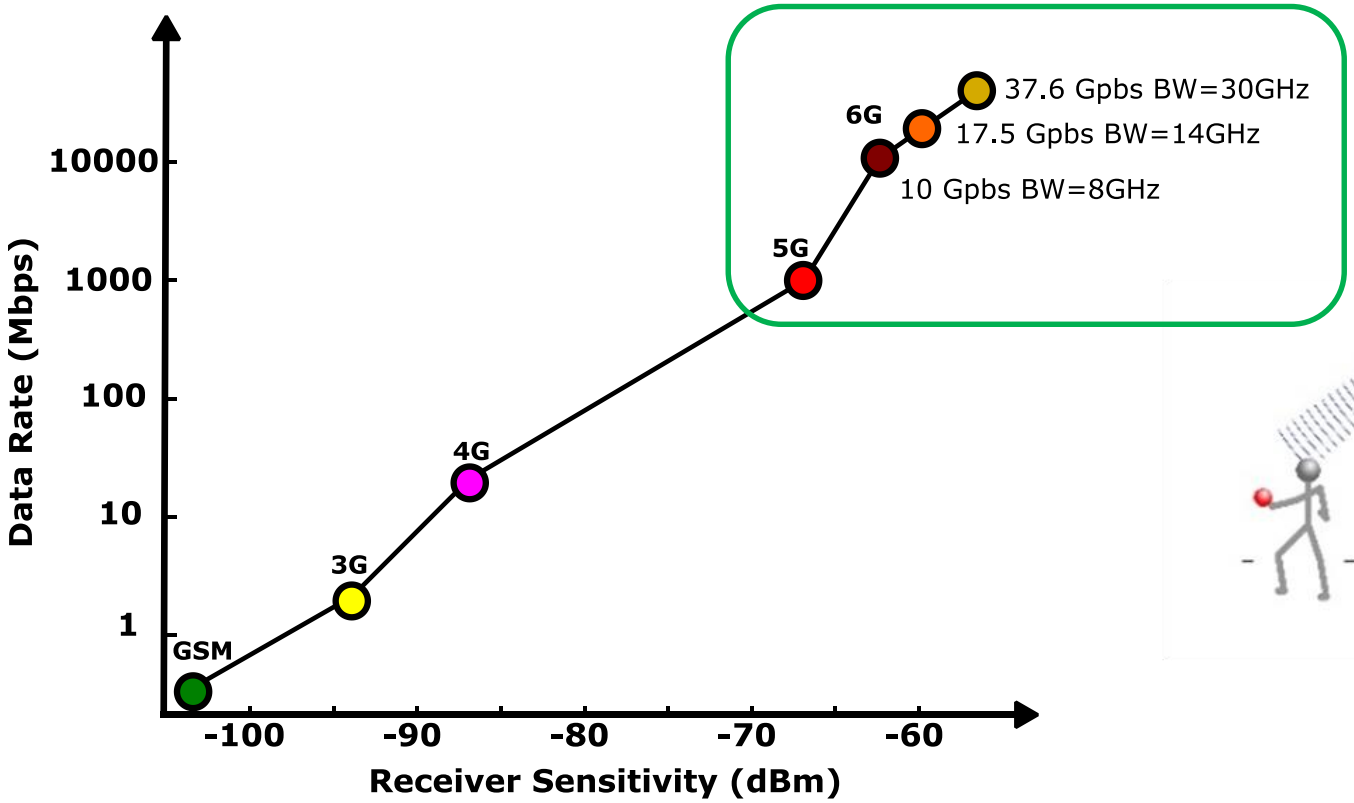


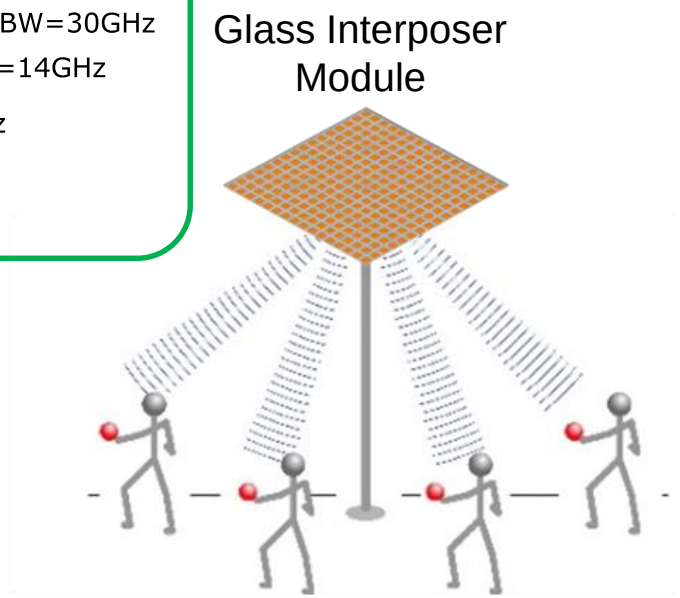


Our (PRC) Focus

Metric	SERDES[5]	IBM Terabus[6]	Proposed work(estimated)
Type of bus	Electrical (Cu on FR4)	Optical (Silicone)	Optical (BCB)
Energy consumption	23.2 pJ/bit	4.65 pJ/bit	≤ 1.2 pJ/bit
BER	10^{-9}	10^{-12}	10^{-12}
distance	1 cm	36 cm	5 cm
Data rate/lane	40 Gb/s	160 Gb/s	896 Gb/s

High Data Rate Wireless

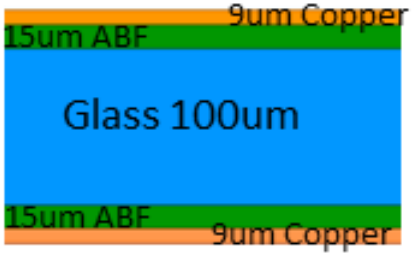




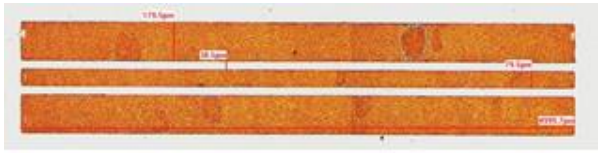
- Higher data rate requires larger bandwidth (1Gbps Vs 10Gbps)
- 5G and sub-THz (6G)
- Antenna in Package is essential

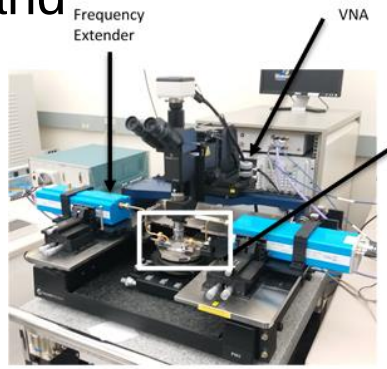
Low Loss Interconnects

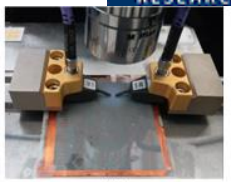
- Coplanar Waveguide (CPW) & Microstrip
- **0.2dB/mm@100GHz and 0.25dB/mm@140GHz**
- Comparable to LCP[2-3], Astra[4], Rogers [5] and Teflon[4]
- Microstrip: 0.076dB/mm (26-30GHz)

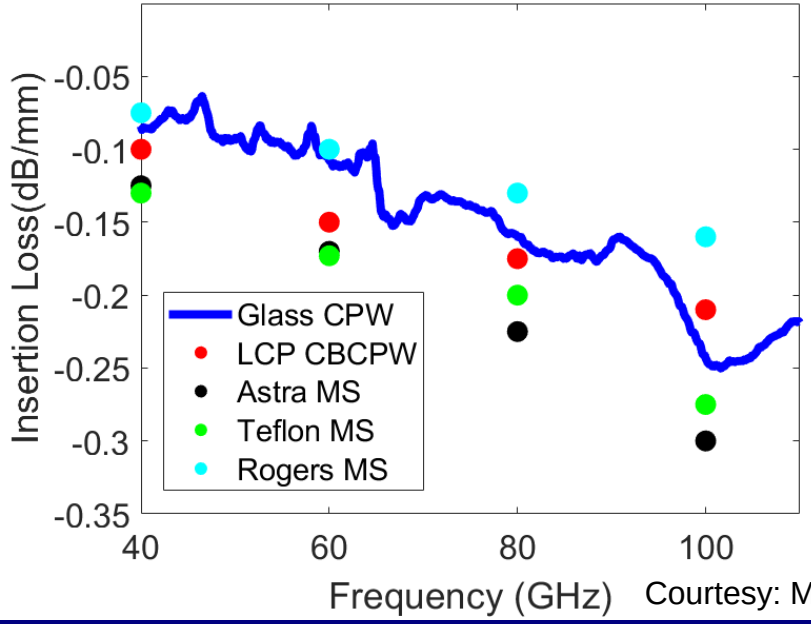


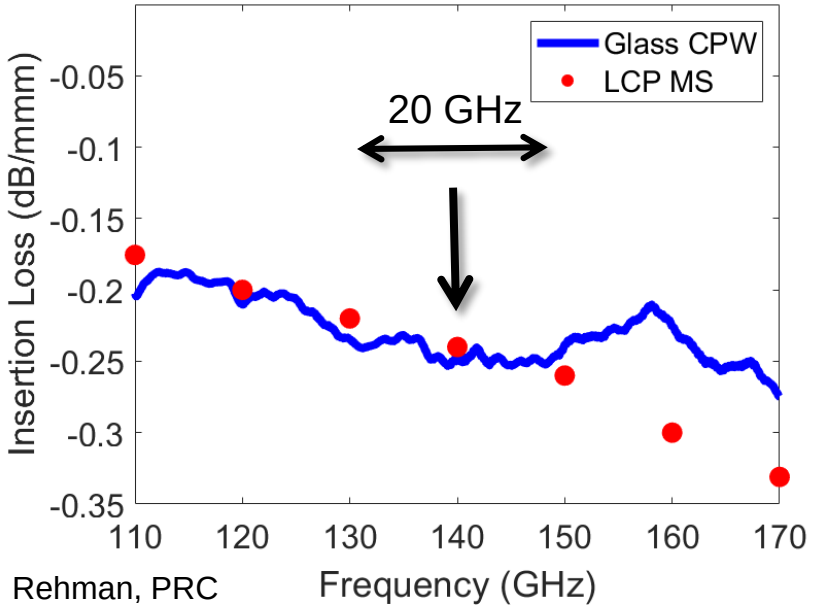
CPW Lines









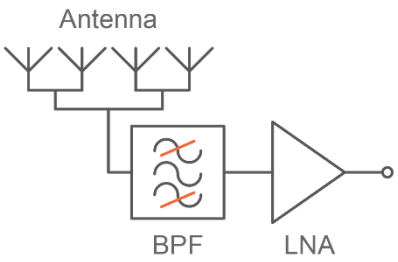


Courtesy: Mutee ur Rehman, PRC

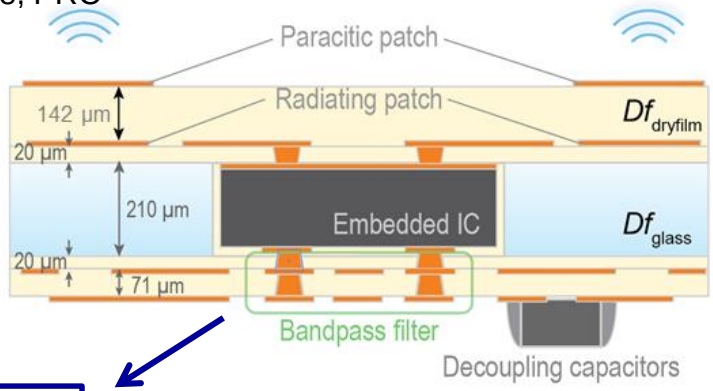
Antenna in Package (AiP) – 5G

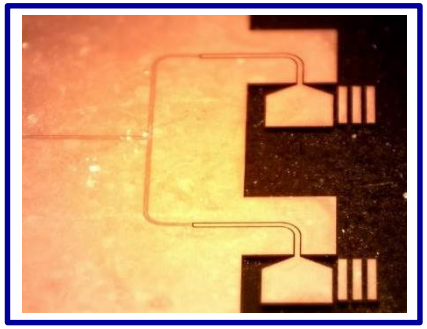
Module architecture

Courtesy: Atom O. Watanabe, PRC



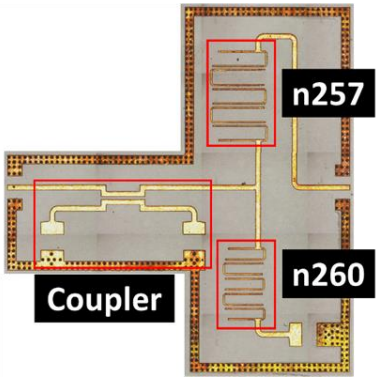
Module stack-up





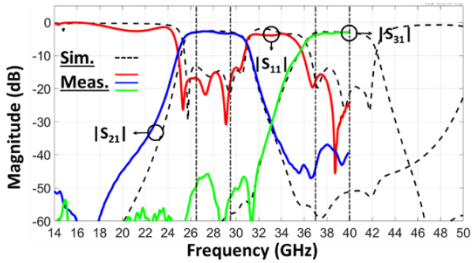
- S11 < -9 dB: 18.87 – 40 GHz
- Gain > 6.2 dBi: 24.25 – 40 GHz
- 5G bands: 24.25 – 40 GHz
- Good performance within the entire 5G bands

Integrated
Hairpin Diplexer n257 and n260 &
Coupled-line Coupler

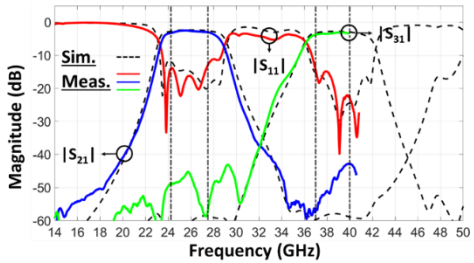


Courtesy: Muhammad Ali, PRC

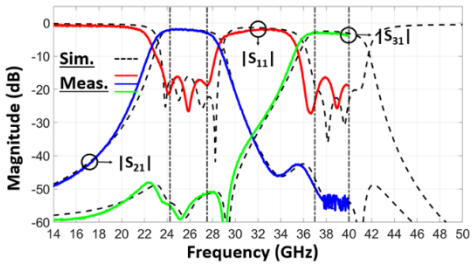
Diplexer - Hairpin n257 and n260



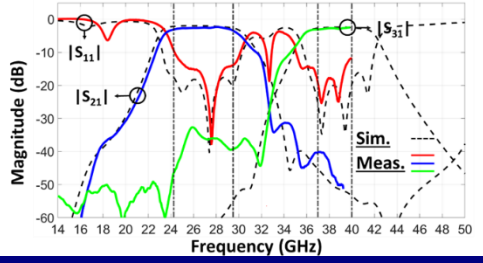
Diplexer - Hairpin n258 and n260



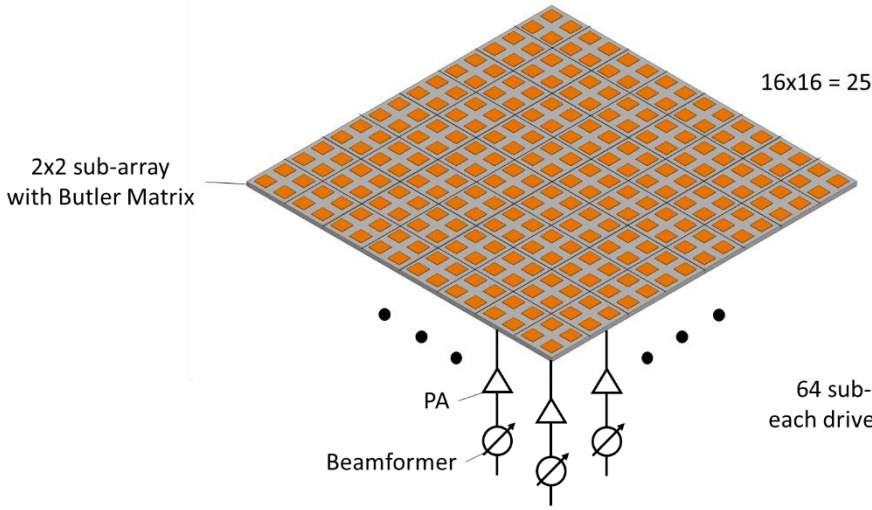
Diplexer - Interdigital n258 and n260

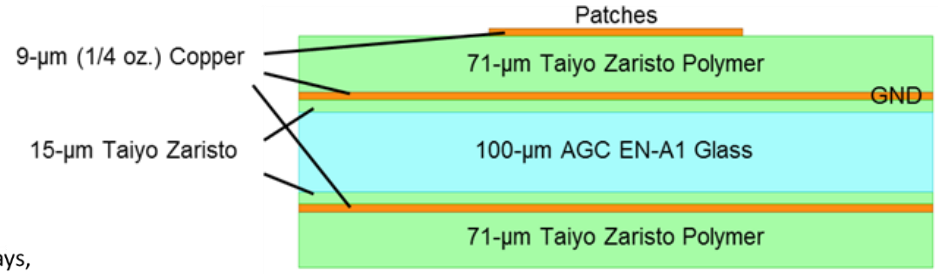


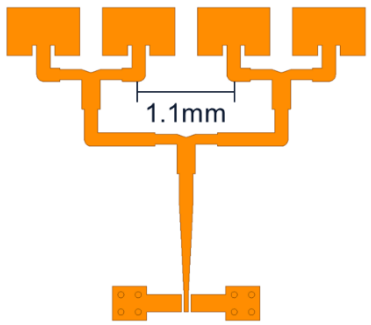
Diplexer – Edge-coupled n257, n258 and n260

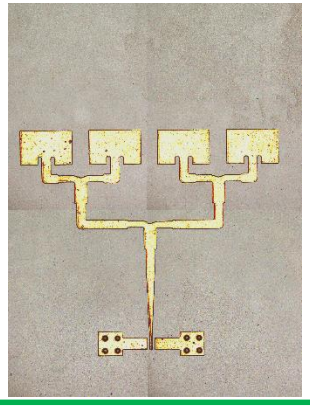


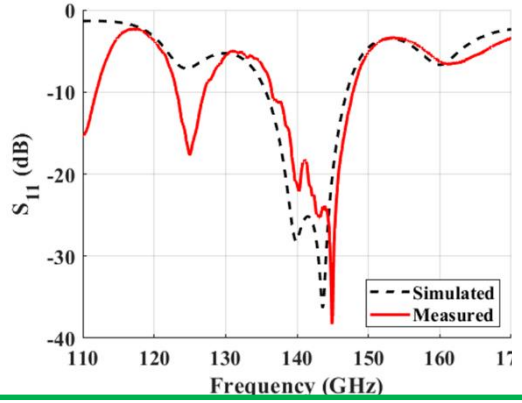
Antenna in Package (AiP) – 6G

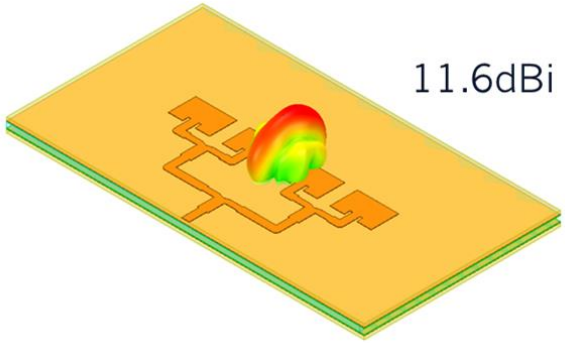










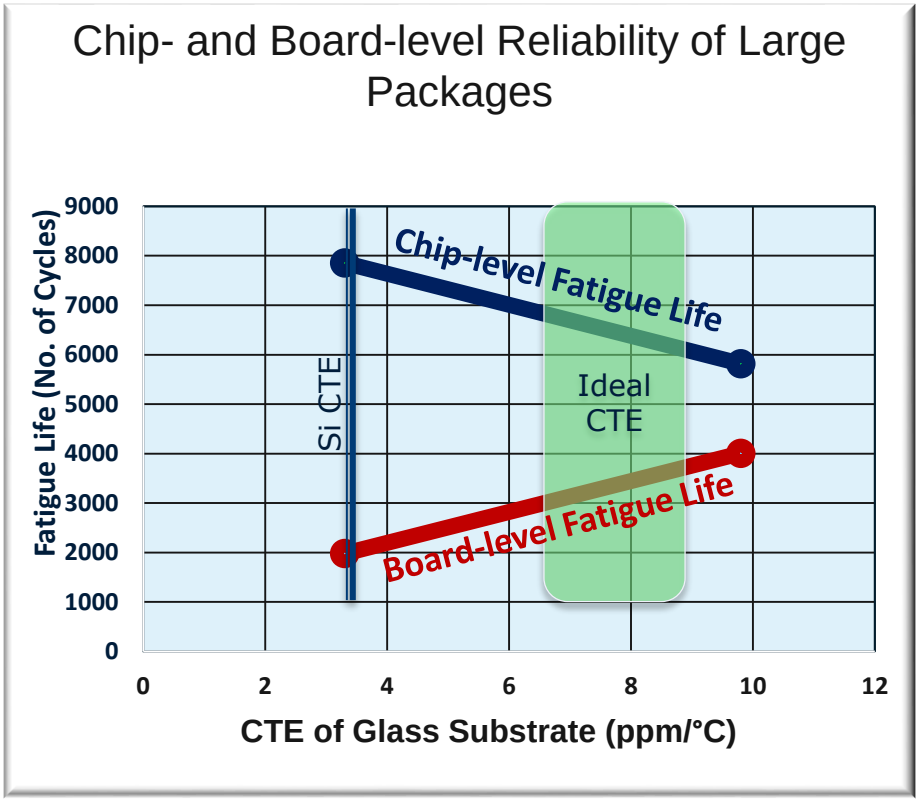


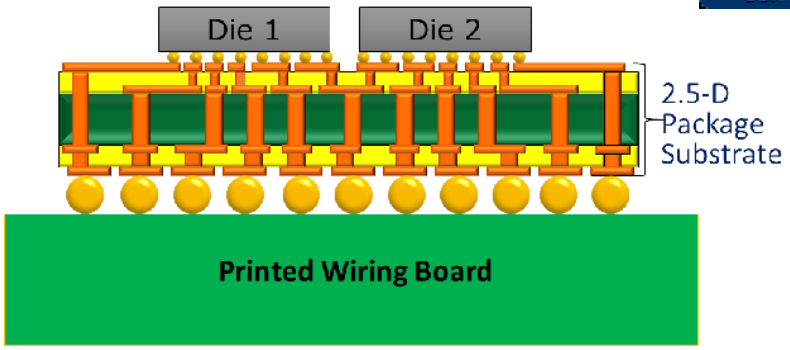
- 2x2 patch antenna elements - top layer
- 2-D Butler matrix - bottom layer
- Feed using vias
- Gain of each element: ~6dBi

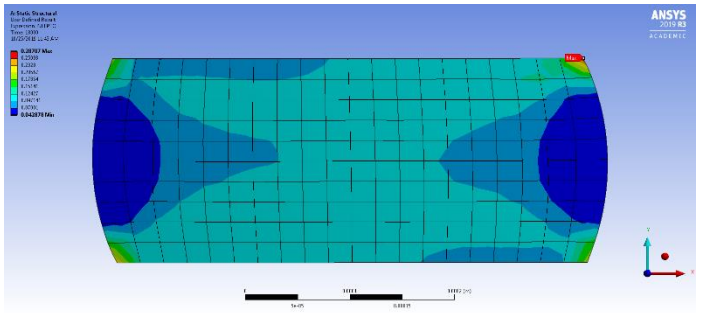
- Element spacing: 1.1mm (λ/2 @140GHz)
- 20% Bandwidth (goal)
- Total area: 3mm x 3mm

Kai-Qi Huang, GT-PRC.

Reliability & Integration



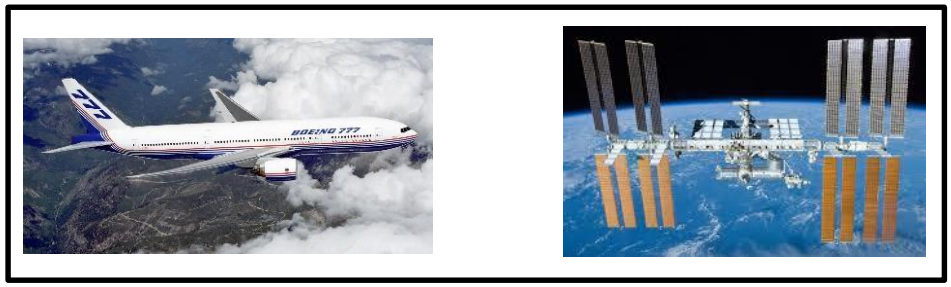




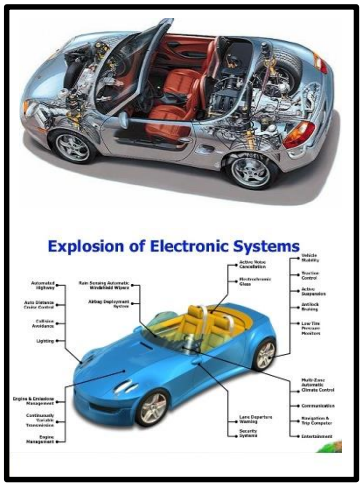
Distribution of accumulated plastic strain in the second last solder ball for high CTE (9 ppm/K) glass substrate

- Direct interposer assembly on to Printed Wiring Board
  - Tuned CTE for Glass Interposer maximizes Chip & Board reliability
- Eliminates ONE level of packaging

Usage vs. Accelerated Testing Various Applications



AEROSPACE



AUTOMOTIVE

3D Systems Packaging Research Center

MILITARY

MEDICAL

COMPUTERS

COMMUNICATIONS

Field Conditions—Aircraft Z

Operating Temperatures:

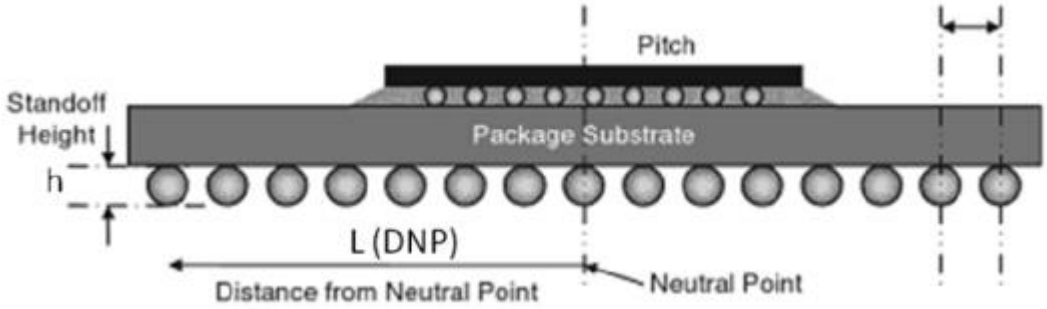
Diurnal Temperatures:

Case #	No. of Occurrences	$T_{initial}=T_{min}$, °C	T_{max}, °C	T_{ave}, °C	ΔT, °C
1	30	-55.0	85	15.0	140.0
2	60	-42.5	85	21.3	127.5
3	150	-32.5	85	26.3	117.5
4	155	-22.5	85	31.3	107.5
5	180	-12.5	85	36.3	97.50
6	950	-2.5	85	41.3	87.50
7	1700	7.5	85	46.3	77.50
8	1800	17.5	85	51.3	67.50
9	950	27.5	85	56.3	57.50
10	20	37.5	85	61.3	47.50
11	20	49.0	85	67.0	36.00

Case #	No. of Occurrences	$T_{initial}=T_{min}$, °C	T_{max}, °C	T_{ave}, °C	ΔT, °C
1	10	-55.0	-50.00	-52.25	5.00
2	20	-42.5	-31.0	-36.75	11.50
3	20	-32.5	-19.0	-25.75	13.50
4	20	-22.5	-7.00	-14.75	15.50
5	70	-12.5	5.00	-3.75	17.50
6	520	-2.5	15.5	6.50	18.00
7	950	7.5	25.5	16.50	18.00
8	1050	17.5	38.0	27.75	20.50
9	500	27.5	57.0	42.25	29.50
10	20	37.5	71.0	54.25	33.50
11	20	49.0	71.0	60.00	22.00

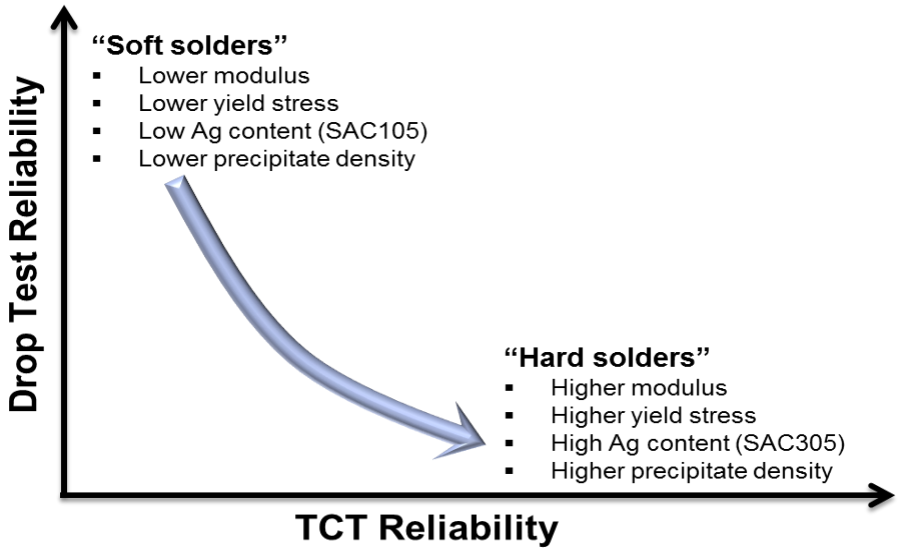
Technical Challenges

- Aggravated solder strains
  - Large CTE mismatch
  - Large package sizes
  - Pitch reduction
  - Aggravated warpage



- Balanced fatigue & drop performance

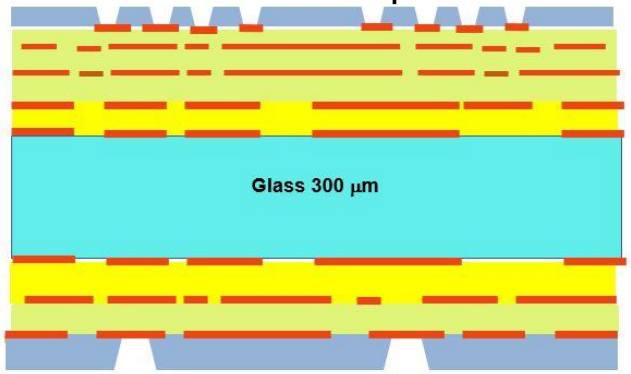
- Additional constraints
  - SMT-compatibility
  - Reworkability
  - System-level reliability



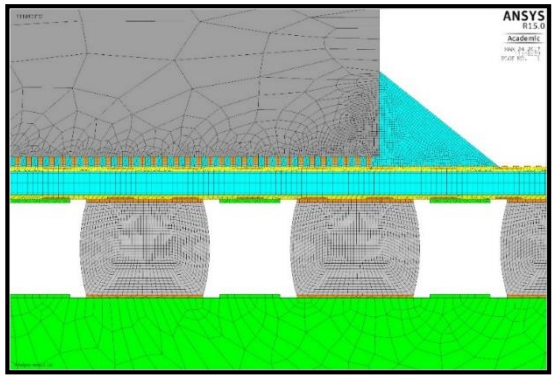
Glass Interposer Reliability for Space Collaboration with JPL

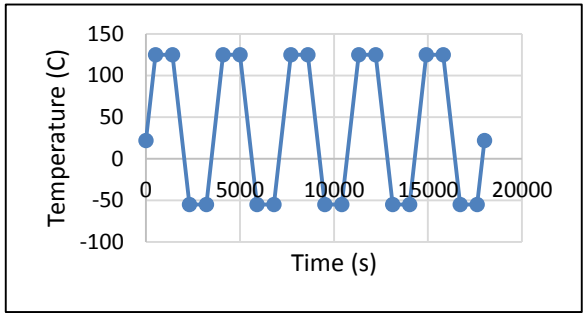
Prof. S. Sitaraman

Glass Interposer

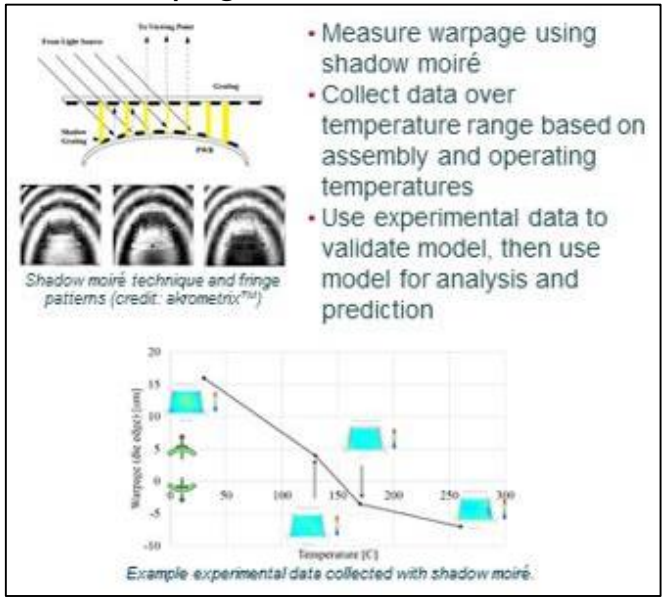


Process Modeling & Prediction from First Principles

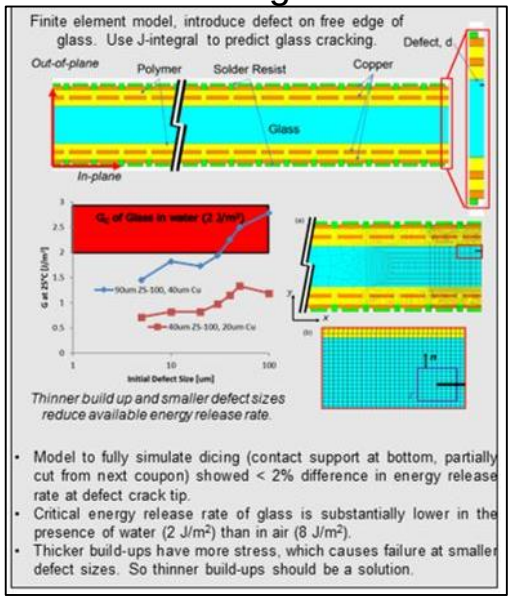




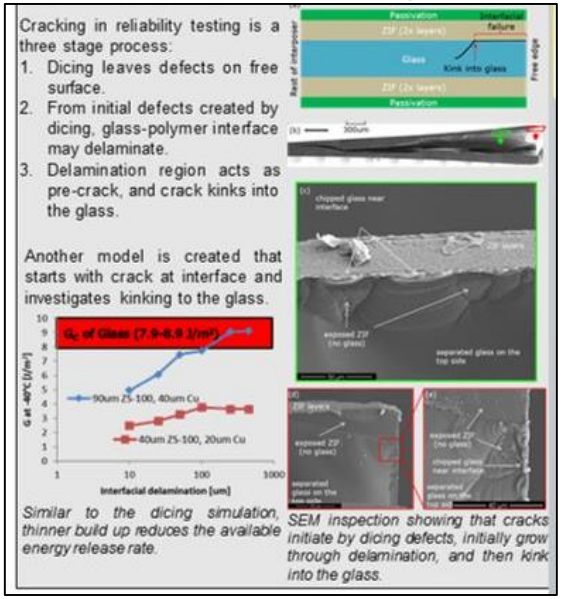
Warpage Measurements



Dicing



TCT Reliability



Thank You

NAMASTÉ

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