

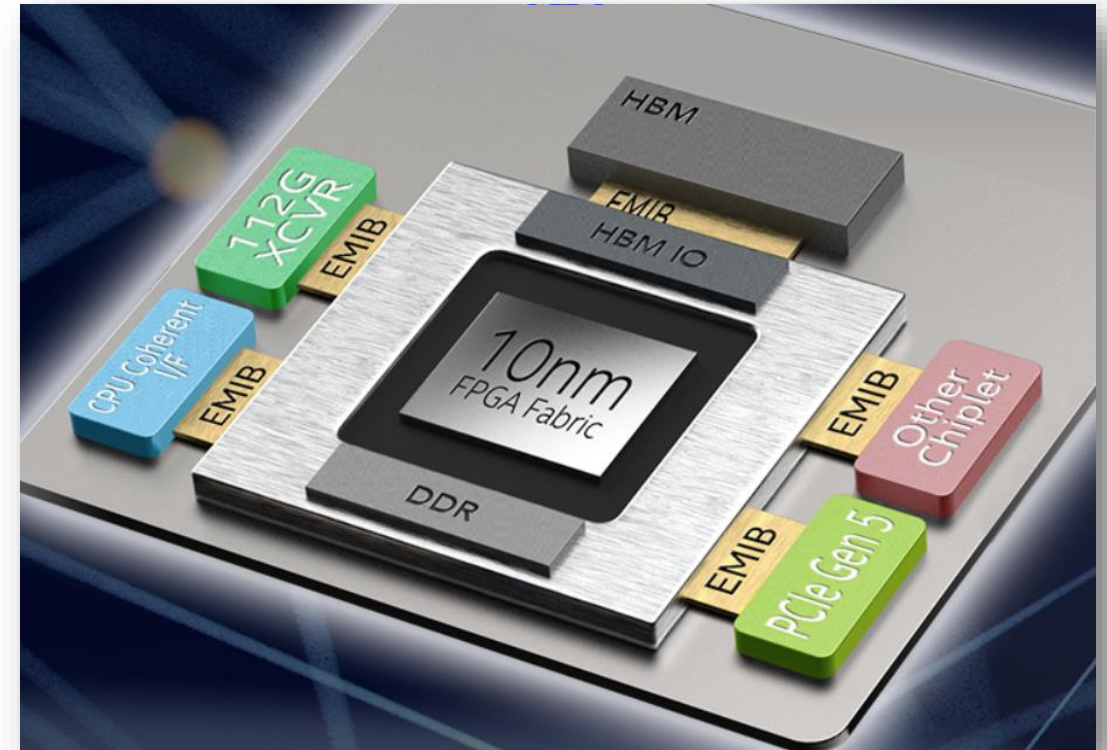
2.5D/3D Heterogeneous Packaging: Design Methodology Overview

Kevin Rinebold

Account Technology Manager – Advanced Packaging Solutions

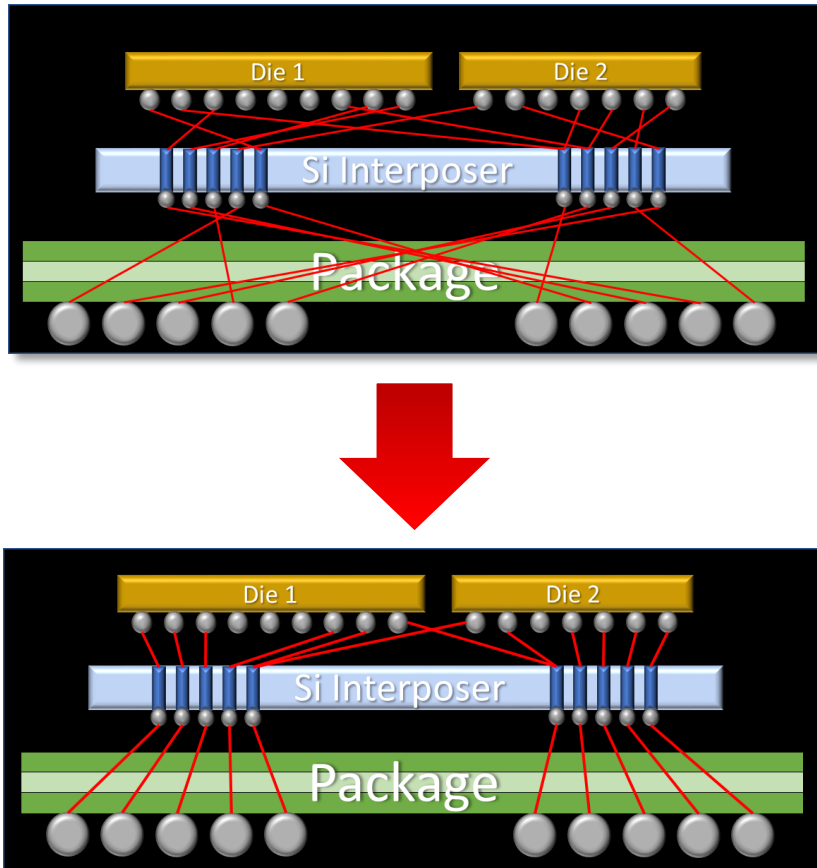
The scale and complexity of 2.5D/3D heterogeneous packages exposes challenges in existing tools and processes

- System planning and prototyping
 - Design abstraction, net list definition, and system level IO optimization
- Substrate implementation
 - Capacity/performance, manufacturing quality
- Verification (DRC/LVS)
 - Individual substrate level, full 3D assembly, and in-process verification
- Multi-domain integration and modeling
 - Mechanical, electrical, thermal, stress



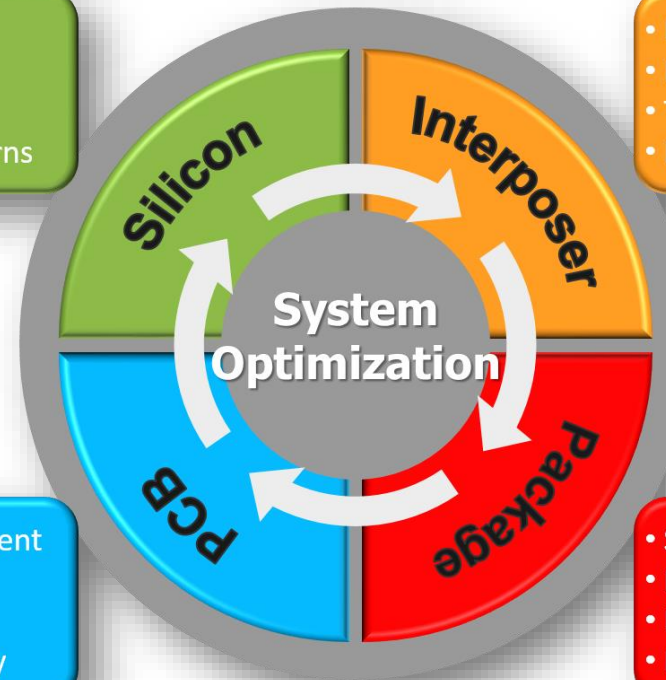
2.5D/3D Heterogeneous planning and prototyping

Interdependences and impact



- Bump placement
- Signal – PG ratio
- Bump connectivity
- RDL tech and patterns

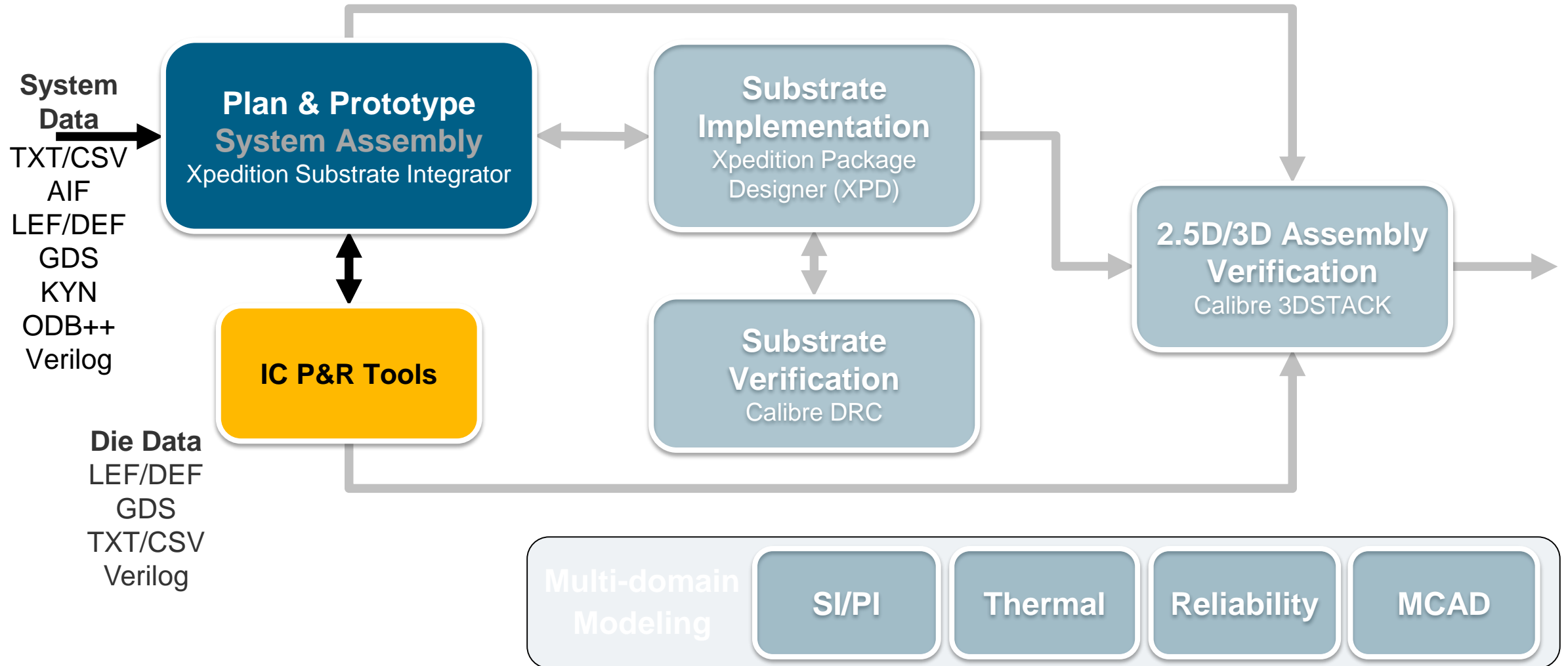
- Critical part placement
- BGA matrix & nets
- Escape routing
- Socket compatibility



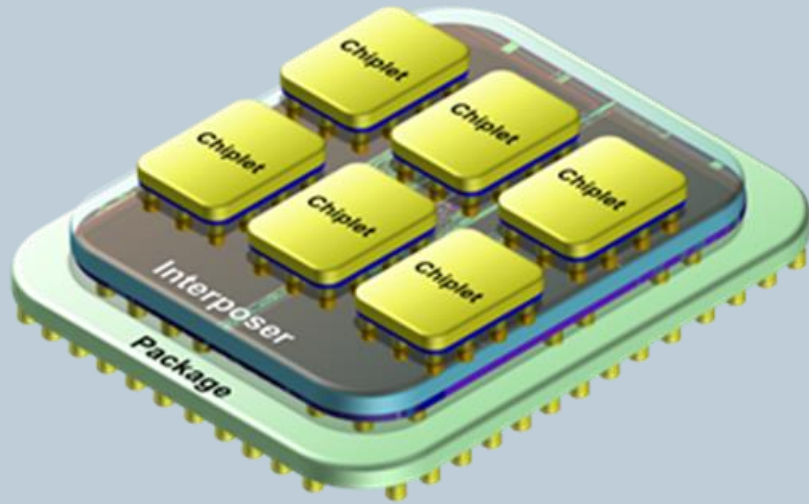
- Micro bump patterns
- Die to die connectivity
- TSV placement
- Bump pattern & nets

- Substrate technology
- Ball matrix & net list
- PG supply strategy
- Die place & config

2.5D/3D Heterogeneous planning and prototyping



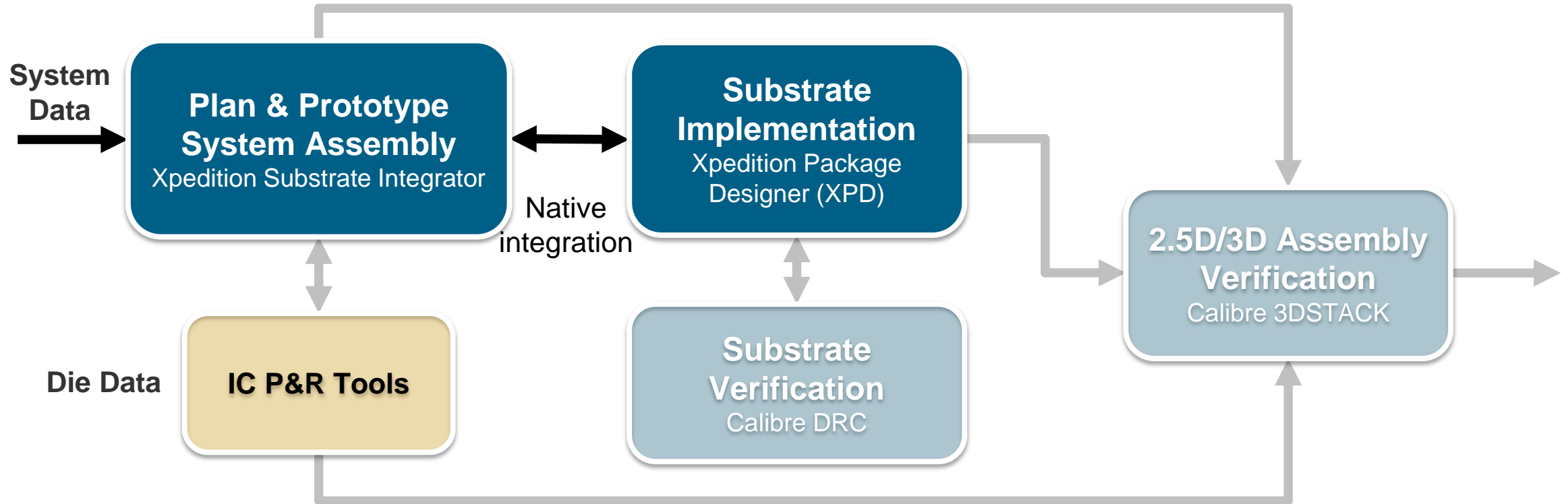
2.5D/3D Heterogeneous planning and prototyping



- ✓ Define and optimize connectivity in context of full-system – die, interposer, package, & pcb
- ✓ Generate and manage the full system net list
- ✓ Minimize dependency on error-prone spreadsheets
- ✓ Drives rapid prototyping to evaluate electrical and thermal feasibility
- ✓ Requires capacity, performance, and scalability for 500K – 2M pin interposer/package designs

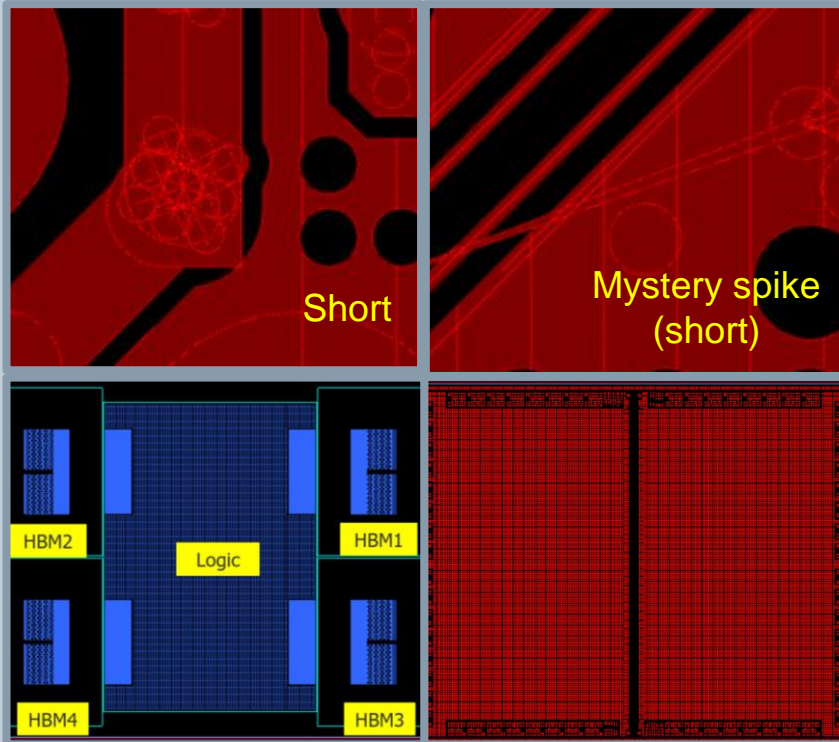
Image courtesy CEA-Leti

2.5D/3D Substrate implementation



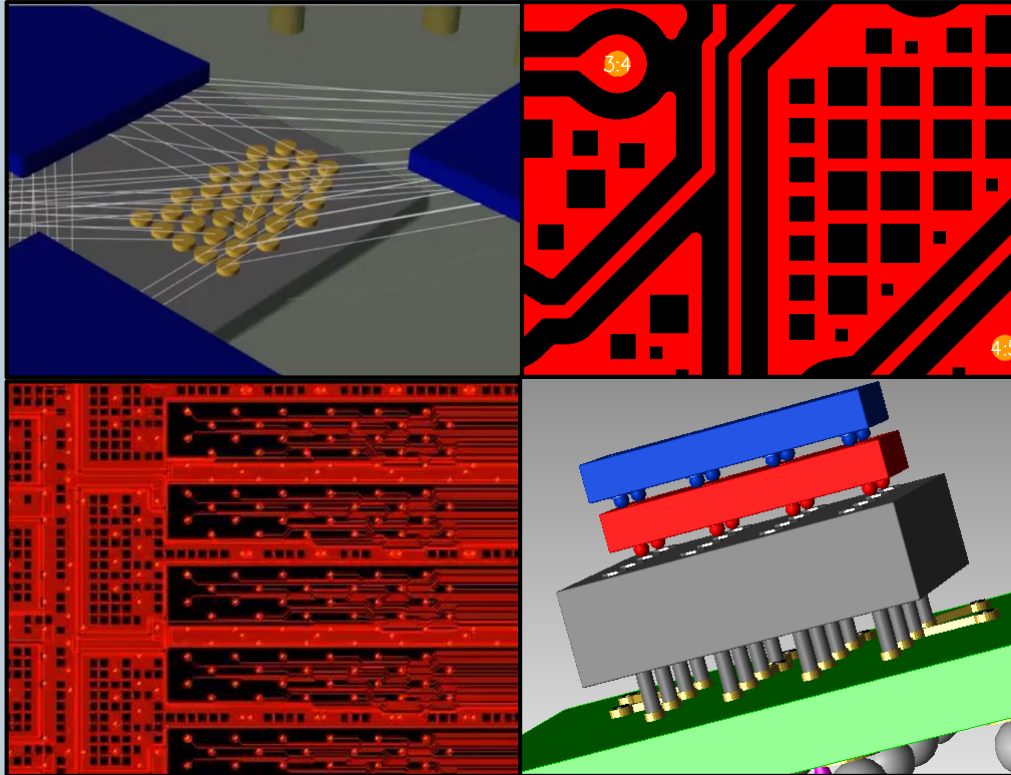
2.5D/3D Substrate implementation

Challenging the legacy solutions



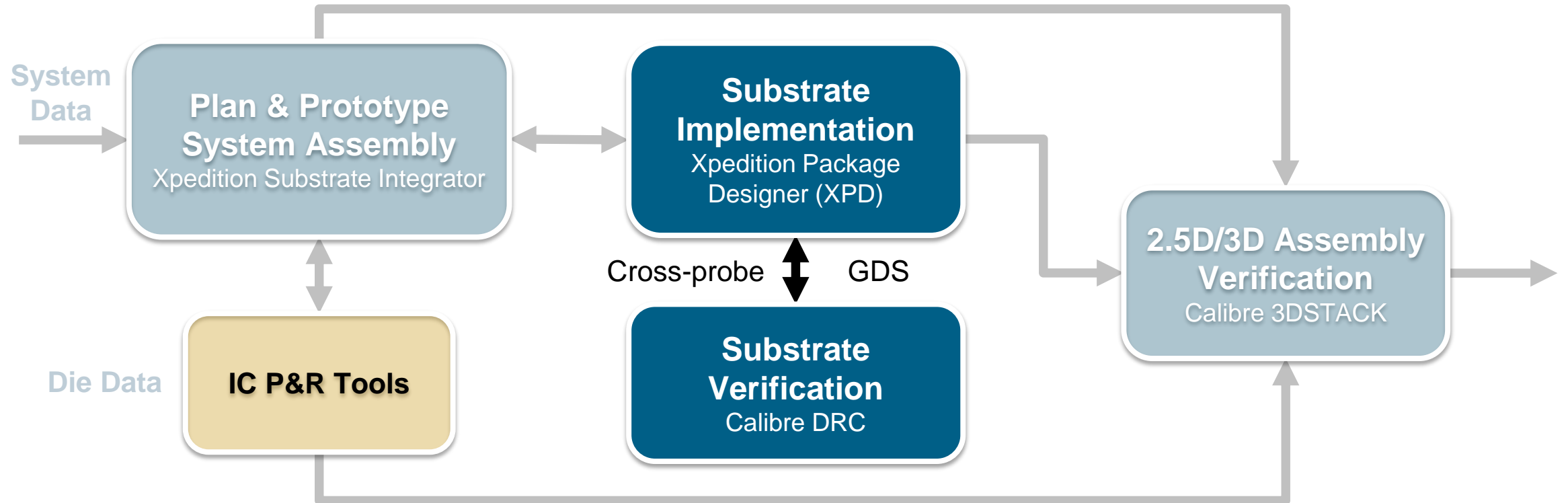
Consistent high-quality manufacturing outputs and tool capacity/performance are problematic areas for legacy tools

2.5D/3D Substrate implementation



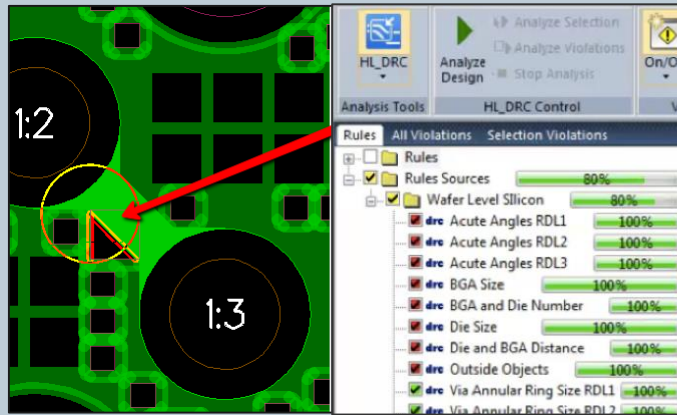
- ✓ Design and verify heterogeneous interposers and packages in a fully integrated 3D environment
- ✓ Capacity and performance for high pin count designs – 500K to 2M range
- ✓ Flexible and efficient areafill with accurate representation of smallest geometries
- ✓ Quality GDSII of non-Manhattan shapes minimizes false verification errors
- ✓ Correct-by-construction methodology

Comprehensive substrate sign-off and verification



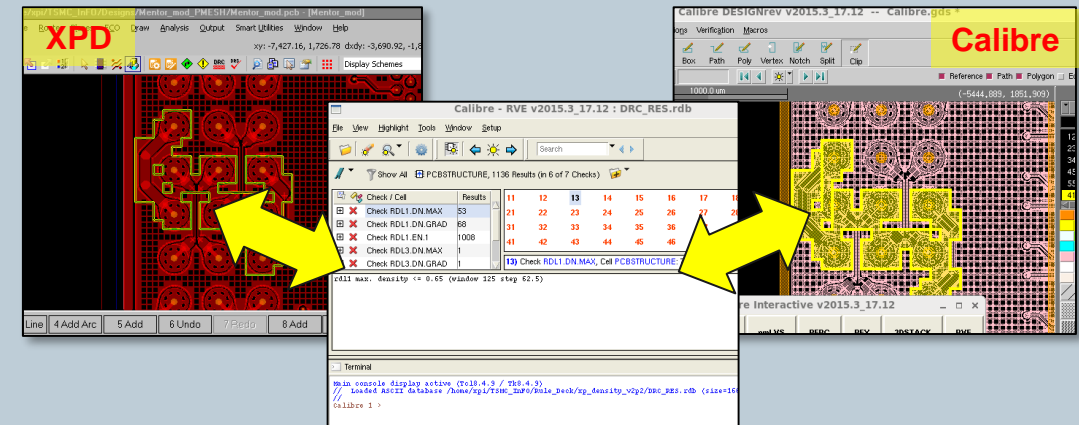
Comprehensive substrate sign-off and verification

In-Design Verification



- Unique in-design verification
 - Automates checking of non-standard rules
 - User-definable custom rules
- Addresses the rapidly changing complex rules of HDAP and interposer technologies
- Identify and resolve most problems before final sign-off

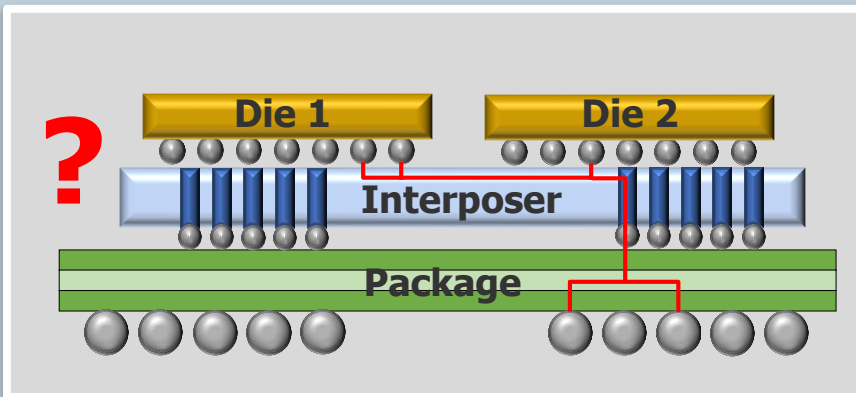
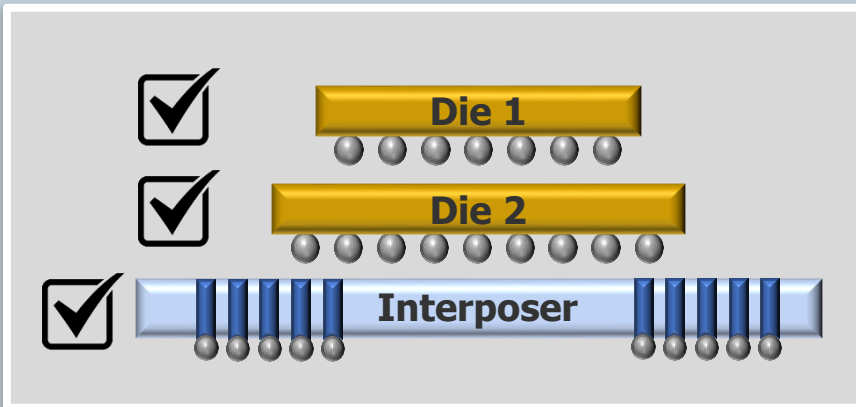
Final sign-off & Verification



- Independently verify the manufacturing outputs not just the design database
- Dynamic cross-probing to quickly identify and resolve issues
- Increasing number of foundries/OSATs requiring independent sign-off with Calibre

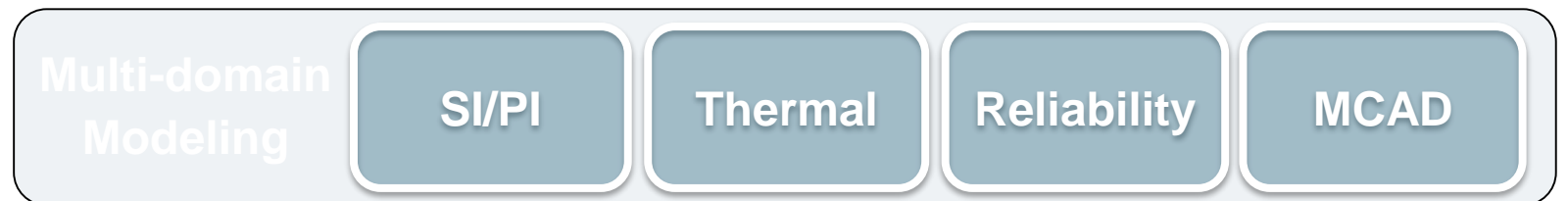
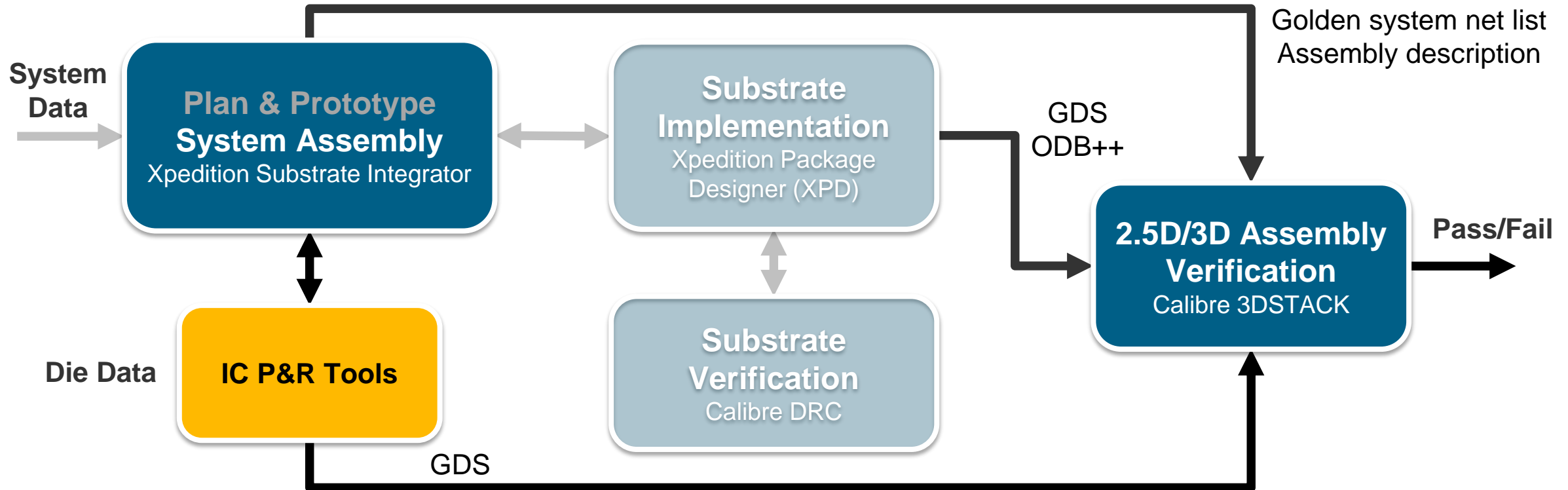
2.5D/3D Heterogeneous assembly verification

Individual device verification isn't enough



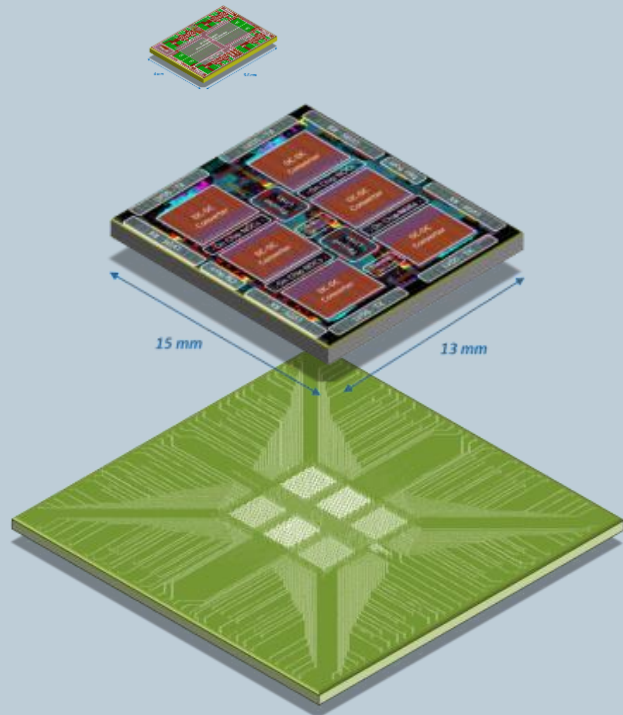
Independently verifying discrete die and substrates per their process rules does not ensure the overall 2.5D/3D package assembly is correct or will perform as expected

2.5D/3D Heterogeneous package assembly verification



2.5D/3D Heterogeneous package assembly verification

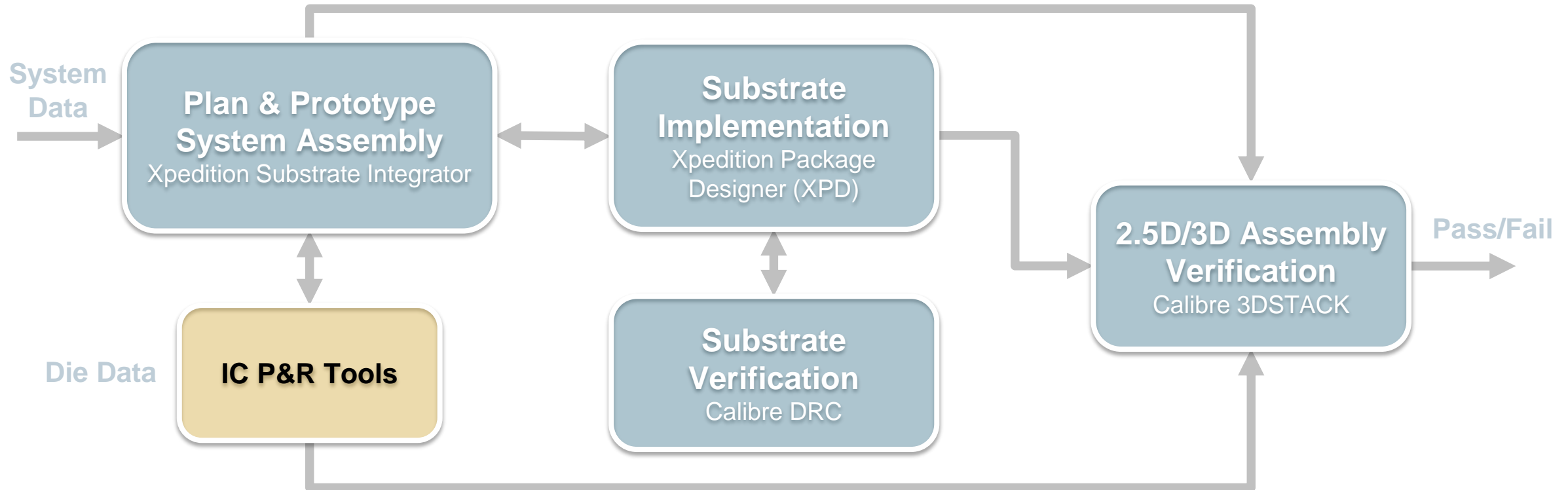
Layout independent assembly verification



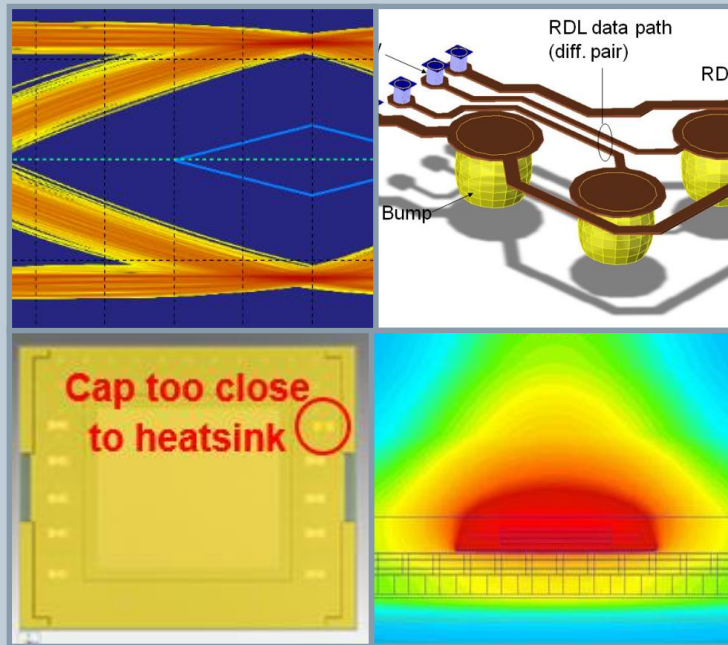
- ✓ Aggregates post-layout design data to build model of the full heterogeneous assembly
- ✓ Verifies golden source model to manufacturing files
- ✓ Performs 3D physical checks across the devices/substrate interfaces (DRC/LVL)
- ✓ Performs connectivity verification between all devices/substrates (LVS)
- ✓ Scalability for increasing design complexity

Image courtesy CEA-Leti

2.5D/3D Heterogeneous packaging Multi-domain modeling



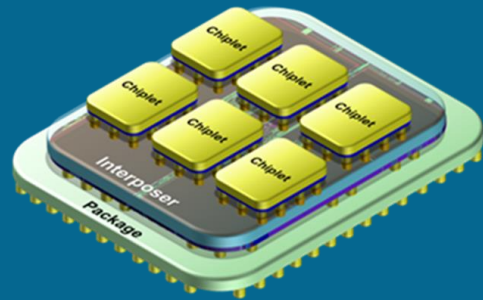
2.5D/3D Heterogeneous packaging Multi-domain modeling



- ✓ Comprehensive solver technology for die and package level extraction
- ✓ Detailed thermal modeling from gate to system level
- ✓ ECAD/MCAD collaborative design
- ✓ Stress analysis to identify unexpected CPI stressors impacting device performance

Comprehensive solution for complex 2.5D/3D Heterogeneous packaging

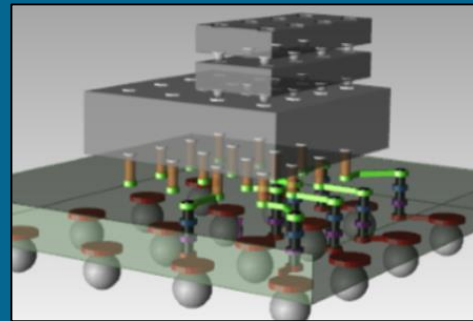
Plan and Prototype



- Define and optimize connectivity in context of the full-system
- Generate and manage the full system net list
- Eliminates dependency on error-prone spreadsheets

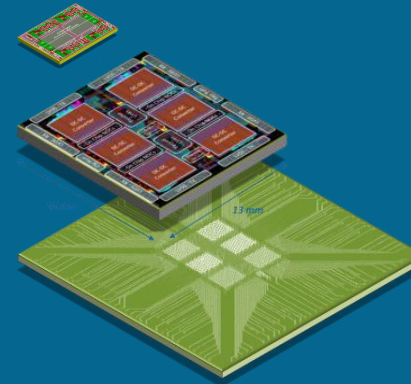
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Implement



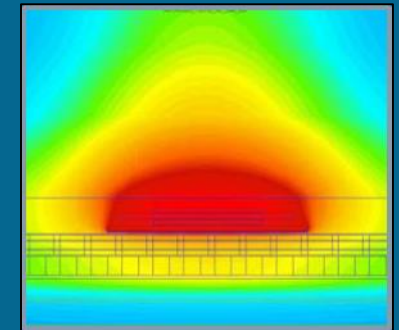
- Fastest path to implement large complex packages
- Minimize substrate re-spins and material scrap cost
- Capacity and performance for the highest pin count designs

Verify



- In-design verification to minimize iterations
- Substrate sign-off with the gold standard – Calibre
- Layout independent full assembly level verification

Model and Simulate



- Comprehensive die and package level extraction
- Detailed thermal modeling from gate to system level
- Stress analysis to identify unexpected stressors impacting performance

For more information please contact:

Brett Attaway

Brett.Attaway@siemensgovt.com

Kevin Rinebold

Kevin.Rinebold@siemens.com