Innovative 20nm Space FPGA Ceramic & Ruggedized Package Trends

2020 NEPP Electronics Technology Workshop

Suresh R.
Fellow, Advanced Packaging

Gamal Refai Ahmed
Fellow,
Chief Thermo-Mechanical Architect

June 16, 2020

RT Kintex UltraScale Platform Announced in May 2020

High Bandwidth Compute Capability

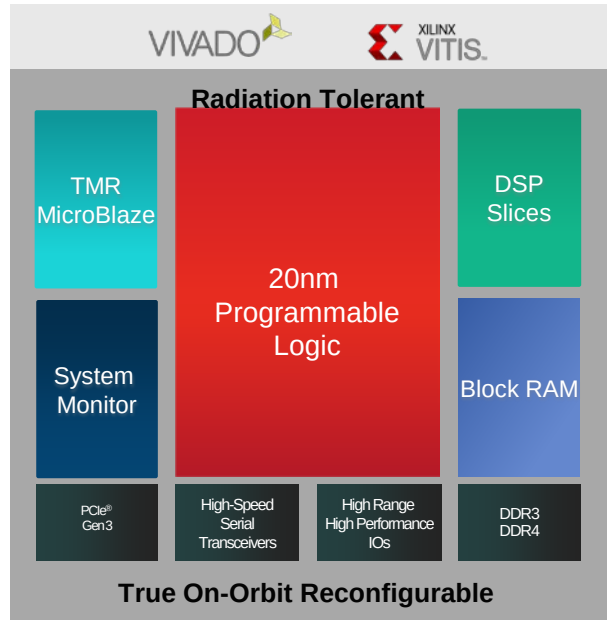
Features

- 2760 DSP Slices: Multi-precision fixed and floating point modes
- 32 High Speed SERDES (12.5Gbps): 400Gbps aggregate BW
- Radiation Tolerance across all orbits TID >100Krad/si, SEL >80MeV-cm^2/mg
- Robust 40x40 mm Ceramic Column Grid Array Packaging
- Machine Learning Ecosystem enables High Performance Edge Inference in Space

Meets Next Generation on Orbit Processing Needs

- Protos, Mechanical Samples: **NOW**
- Vivado SW, XPE*, Datasheet: **NOW**
- Production (Class B, Class Y): **Sept 2020**

MIL-PRF-38535



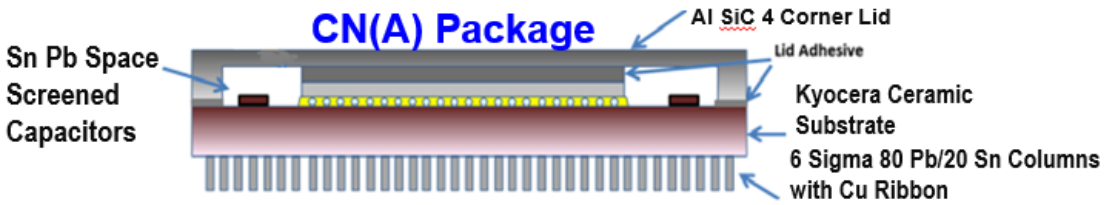
Process, Analyze & Reconfigure

*XPE Xilinx Power Estimator Tool, TID = Total Ionizing Dose, SEL = Single Event Latchup

XILINX

Introducing 20nm Technology: XQRKU060-CNA1509 Package

- Package Details: 40x40 mm ceramic flip chip package with Pb/Sn Cu ribbon solder columns
  - Same package construction/columns as current XQR5VFX130-CN1752 45x45 mm package
  - Qualification on track
- Enhancing the Thermo-Mechanical Integrity for High G /Vibration Environment
  - Introducing edge bonding to the package (Zymet UA2605-B)
  - To eliminate any Mechanical crack between the package the PCB interconnect
  - Enabling back bracket to stiffen the package in the System
  - Introducing Dynamic mounting to apply constant pressure on the package during the life time
  - Ensuring stable thermal contact between the package and the thermal solution



Bill Of Material & Suppliers	XQRKU060-CNA1509	XQR5VFX130-CN1752
C4 Bump	Eutectic Sn Pb	Same
Lid	4 corner AlSiC	Same
Substrate	Ceramic (Alumina)	Same
Chip Capacitors	Sn Pb with cap level space qual testing per MIL-PRF-32535	Same
Column	80 Pb/20 Sn with Cu ribbon	Same
Assembly Supplier	Kyocera San Diego	Same
Column Attach Supplier	6 Sigma	Same

Edge bonding passing 2500 cycles (see Zymet UA-2605-B Edge Bond Adhesive)

XILINX.

What are the options beyond 20 nm for Space?

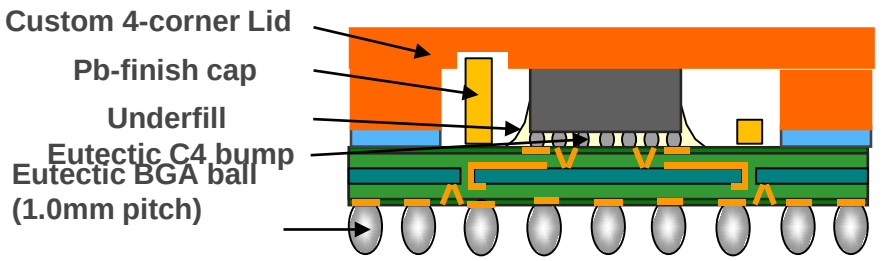
Ceramic running into design and technology bottlenecks

Feature	HTCC (SIRF POR)	LTCC (870T)	Organic	Comment
Process Temp	> 2000C	< 1000C	< 250C	
Dielectric Material	Alumina	Special Ceramic	Epoxy Silica filled (>80%)	
Metallization	Fused W or Mo	Fused Cu	Cu	Resistivity: Fused W >> Fused Cu >> Cu
Substrate CTE ppm/C	7 ppm/C	11-12 ppm/C	13-15 ppm/C	PCB CTE 17-21 ppm/C
PKG Type	Pin / CCGA	BGA / LGA	BGA / LGA	BGA assembly much easier
Lamination process	One-time	One-time	Sequential	
Via formation	Universal Punch tooling	Universal Punch Tooling	Laser drill	Organic via density >> Ceramic
Min. C4 pitch	180um	150um - 180um	110um	7nm is 130um min.
Min. Dielectric thickness	100um	75um*	25um	*50um maybe available 4 layers
Line/Space um	75um/75um min.	40um / 40um	10um / 10um	
Via/pad um	100um / 150um	50um / 100um	50um / 85um	
Advanced node designs	Not feasible	May be feasible with pitch fan-out and derating	Exists 14L – 18L	Technology/design not feasible PDN, X-talk metrics challenging to meet with Ceramic
Applying Mech Pressure	~10-15PSI	~10-15PSI	~30-50 PSI	Next Gen need to stand for high Thermo-mech solution
Thermal solution, RJA	~ 3 C/W	~3 C/W	~/>1.5 C/W	Next Gen need more thermal performance
Power W(Flux W/cm2)	</= 12 (5W/Cm2)	</= 12 (5W/Cm2)	>+25W (7W/Cm2)	Next Gen need to have more Performance/W by Adding more hard IP

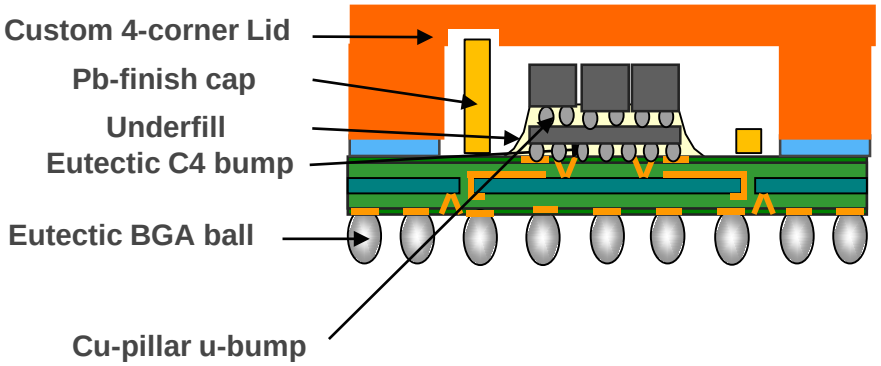
Ruggedized Organic Packaging for Non Space Applications

Current (In Production)

Monolithic 20nm/16nm



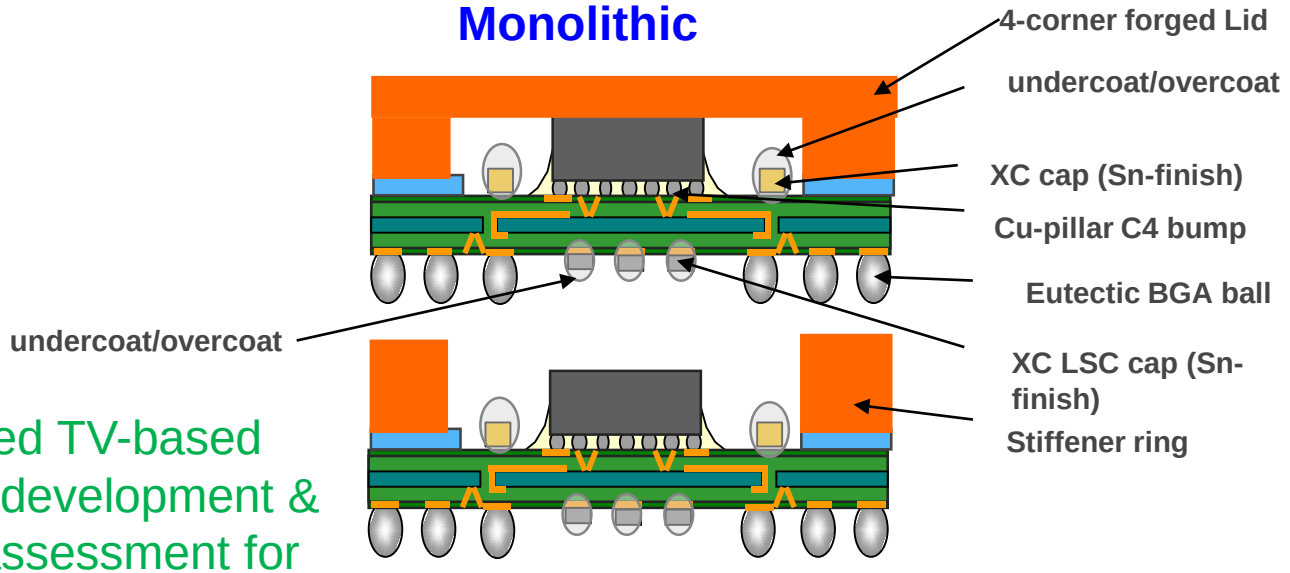
SSIT 20nm/16nm (non-HBM)



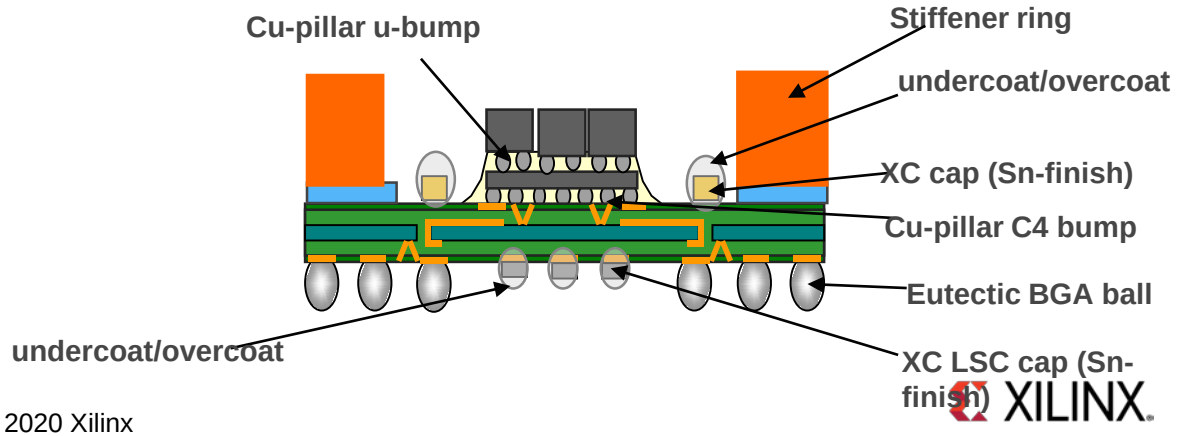
Completed TV-based technology development & reliability assessment for next generation solutions

Future

Monolithic

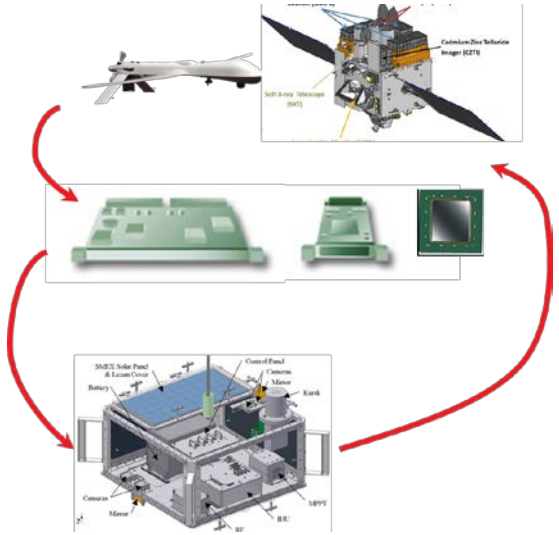


SSIT (non-HBM)



XILINX

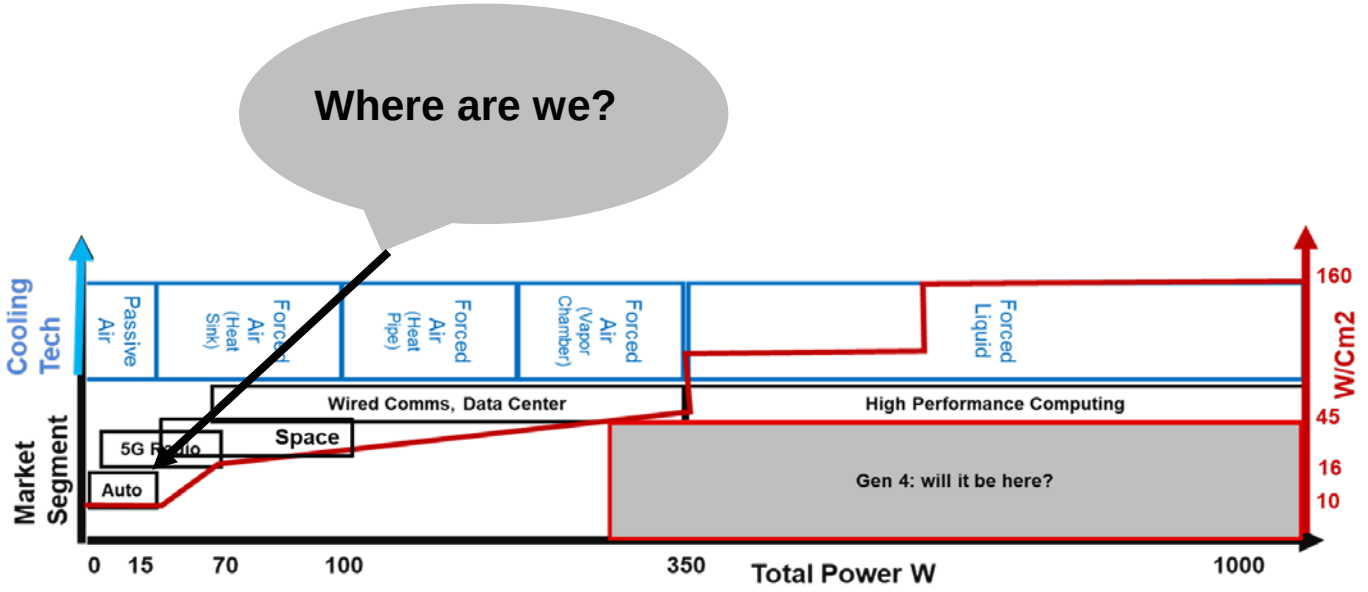
Today Challenges were addressed in 20nm Technology



- Determine application requirements
  - Size, weight and power
    - →XLNX
- Select overall system parameters
  - →XLNX
- Assemble development vehicle
  - →COTS
- Design deployment system

Space PKG solution need to be architected based on:

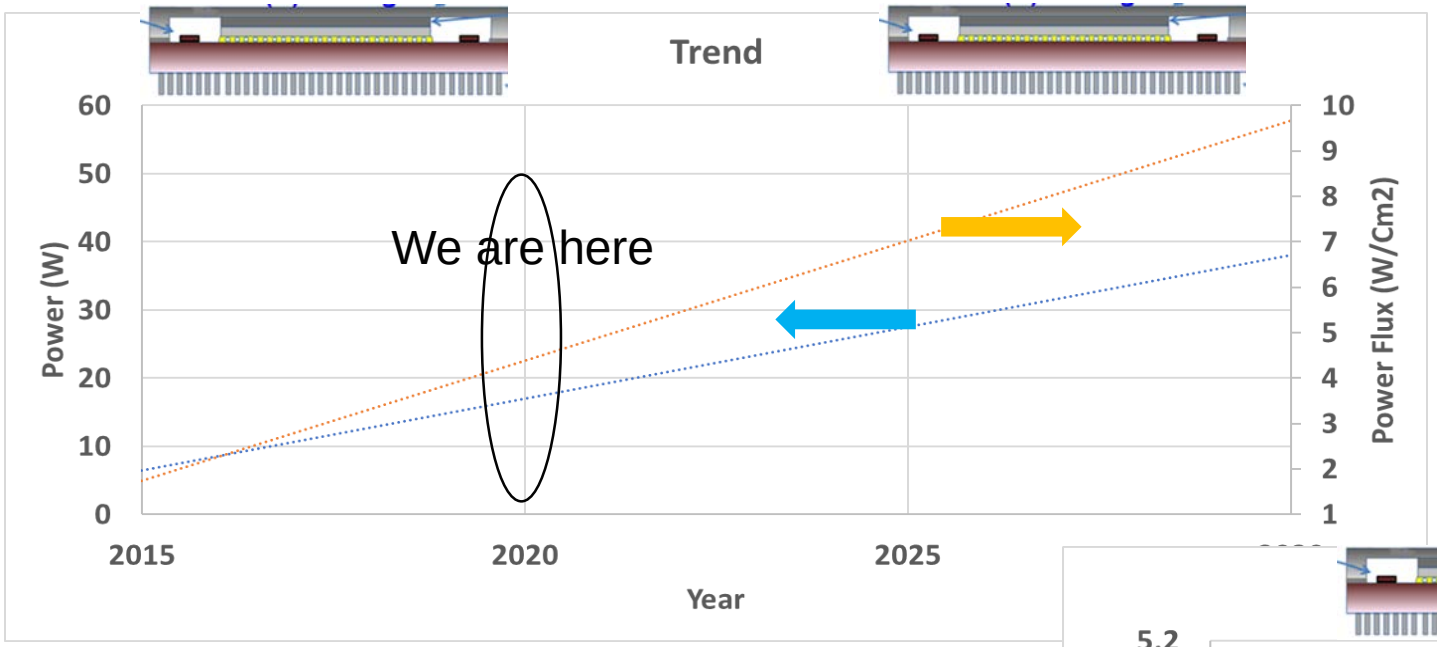
- Package Features
  - Interconnectivity
  - Line/spacing/Pad
  - Dielectric thickness
- Mechanical
  - Package structure
  - Assembly and Manufacture
- Thermal Management
  - Power Map;
  - Current Density
- Reliability



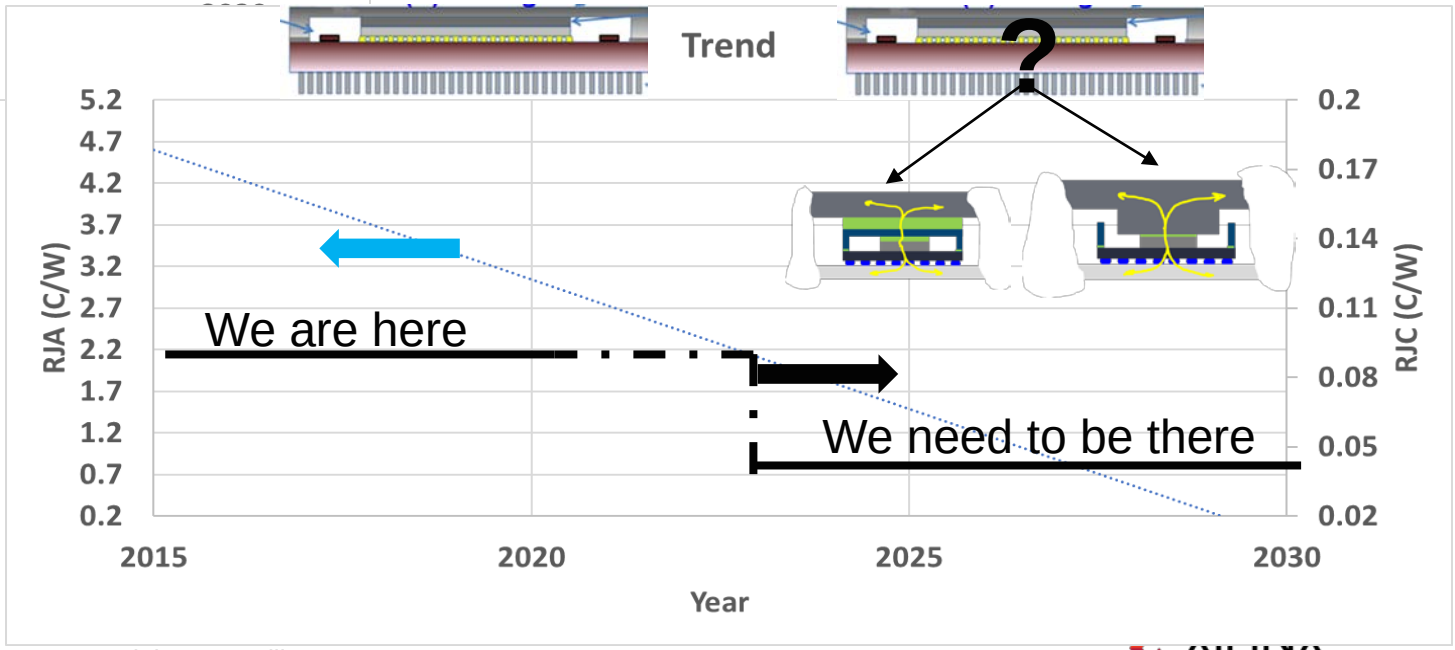
- Given all of the above
  - Can we extended thermal limit of FPGA in aerospace applications?

XILINX.

Past, Present, Future



We are ready for 20 nm and beyond



Adaptable.
Intelligent.

XILINX