ARM Radiation Testing & Collaborations

Steven M. Guertin

Jet Propulsion Laboratory / California Institute of Technology

Pasadena, CA

Outline

- SOCs/Program Perspective

- Goals

- Background on ARM/Collaborations

- Radiation Effects Evaluation Methods

- Results – SAMA5D3 - & final Snapdragon 835/845 – ReCap of FY19 results

- Future/Planned Work

- Conclusion

Processor Efforts/Enclave

- In the last 10-15 years there has been a big push to put more COTS hardware in space
  - Achieving normal Space Qual ~$10M-$100M
  - On lower-end architectures (Raspberry Pi), this is cheaper, but not really necessary
  - Low criticality (including ISS!), but also non-NASA
- You simply can't get 10000+ MIPS/W in RHBD
  - Can you make your application live in the RHBD range?
  - Do you sacrifice reliability and minimize qual cost?
  - Do you spend a lot of money on a qual that may fail?

- This trade off is not viable for most space users
  - Only options is minimal qual – which Ed talked about
  - Processor Enclave is seeking to help find reduced qual approaches to achieve some level of reliability
- The good news – 10x-1000x more processing…
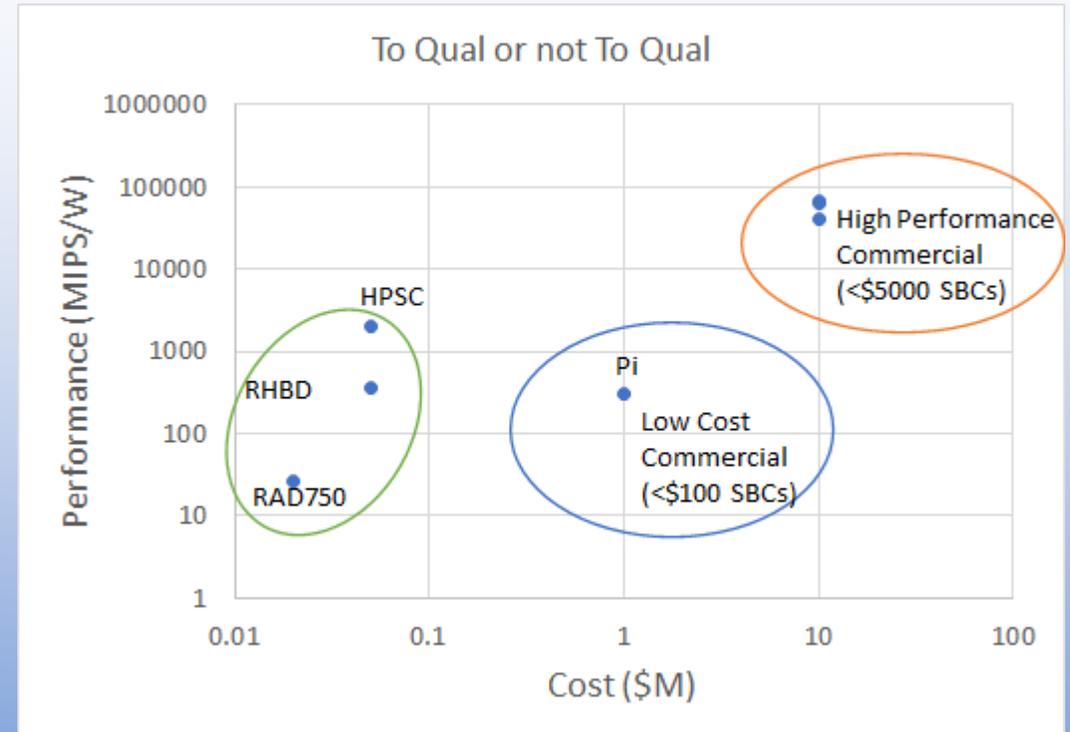
Assumes a "good qual", not just a "quick & dirty" exposure of a few flight lot boards. (this is literally a night & day difference)

Devices of Interest - ARM

- Drone processors
    – like Snapdragon 801
        on Mars Helicopter
- Cell phone processors – like
    Snapdragon 820-855, 865 (5nm!)
- Microchip/Atmel SAMA5D3
    – (ARM A5 devices – collaboration…)
- Xilinx Ultrascale+ MPSoC, similar
- TI TMS570 or similar – for fault tolerant ARM architecture
- (Broadcom, Huawei, Rockchips – esp. RK1808 with neural CPUs…)
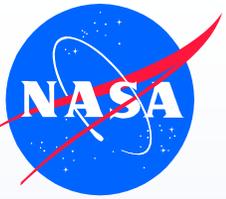
ARM Processor Testing Overview

- Understanding processor testing for space
  - What's it going to do with radiation
    - Calculation errors – possible incorrect operation
    - In fact, falling on its face is more likely, requiring reset
    - May permanently fail
  - Test approaches
    - Low-level structures – the old approach, and still used for RHBD devices
    - Application based
- Build collaborations
  - Maximize budget impact by covering more of the space
  - Identify key mission needs – reliability, cost, performance, relevant data
  - Develop better metrics to enable comparison of devices
    - For example, the entire SWAP required to implement a system
    - Dissimilar processor architectures should not always be compared
- Key issues
  - Limited documentation, expensive evaluation equipment, complex system design and complex error modes, potential severely limited hardware options (partner chips, etc.)

ARM

- Modern space processors are dependent on commercial IP.
- IP-only – puts ARM in a unique position...
  - They don't make hardware.
  - They need to develop and verify fault tolerance works correctly.
  - They need to help licensees properly implement hardware and software.
- Increasing understanding that 10+ heterogenous processor SOCs will stop much more often than they give a wrong answer.
- We can engage ARM to understand:
  - Fault modes; correction methods
  - Fault handling
  - Hardware configuration and handling
    - TMR, DMR, on-chip clusters, proper enabling
  - Software impact

Fault Correction

Fault Handling

Multi-node Redundancy

ARM IP

Space RHBD SOCs

Cutting edge commercial

Low power, high rel commercial

FPGAs

ASICs
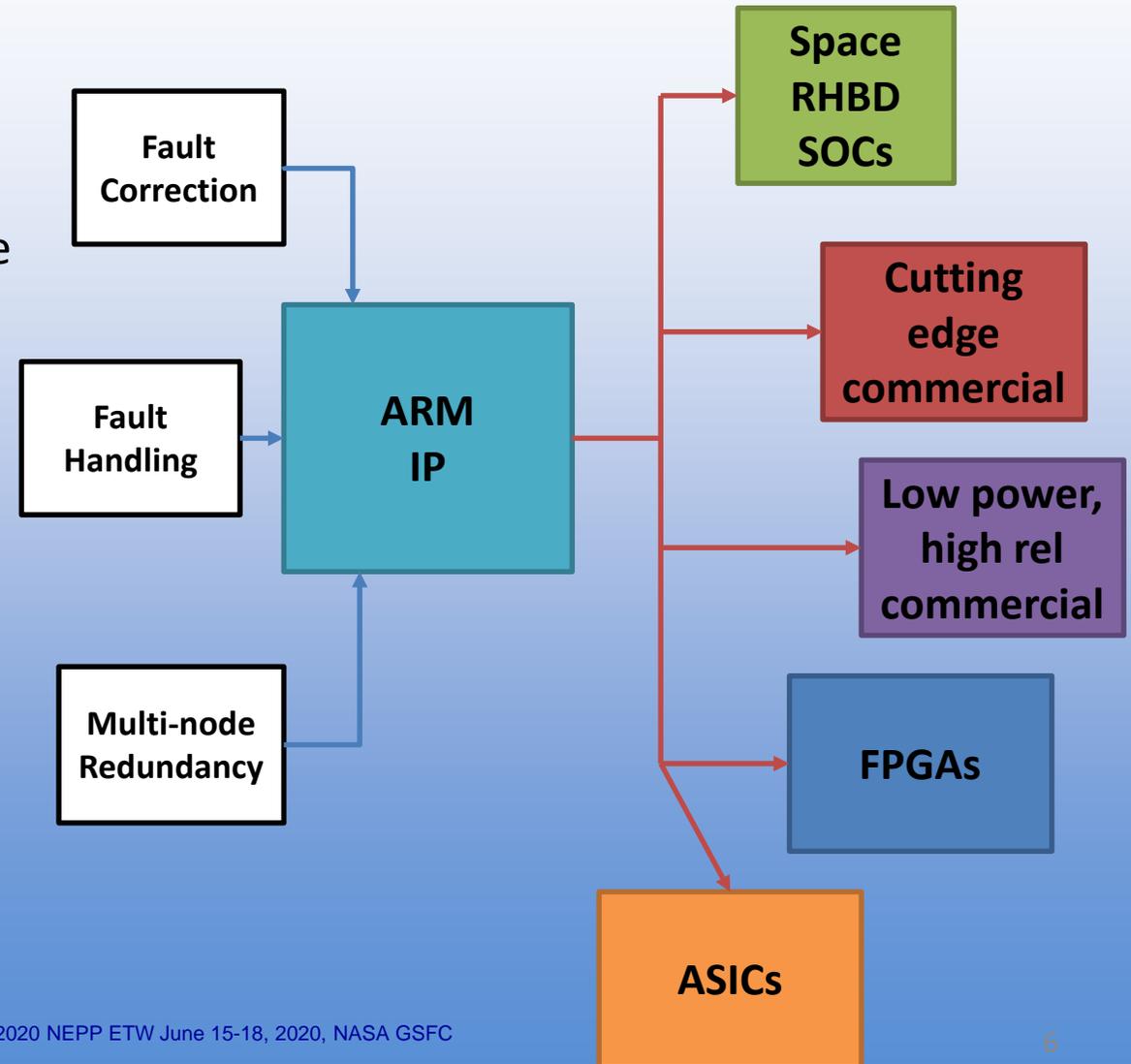
What is an SOC

- Anything that combines multiple functions to create a system
  - Does not need to be a single device that is a system by itself – SOCs may need support devices
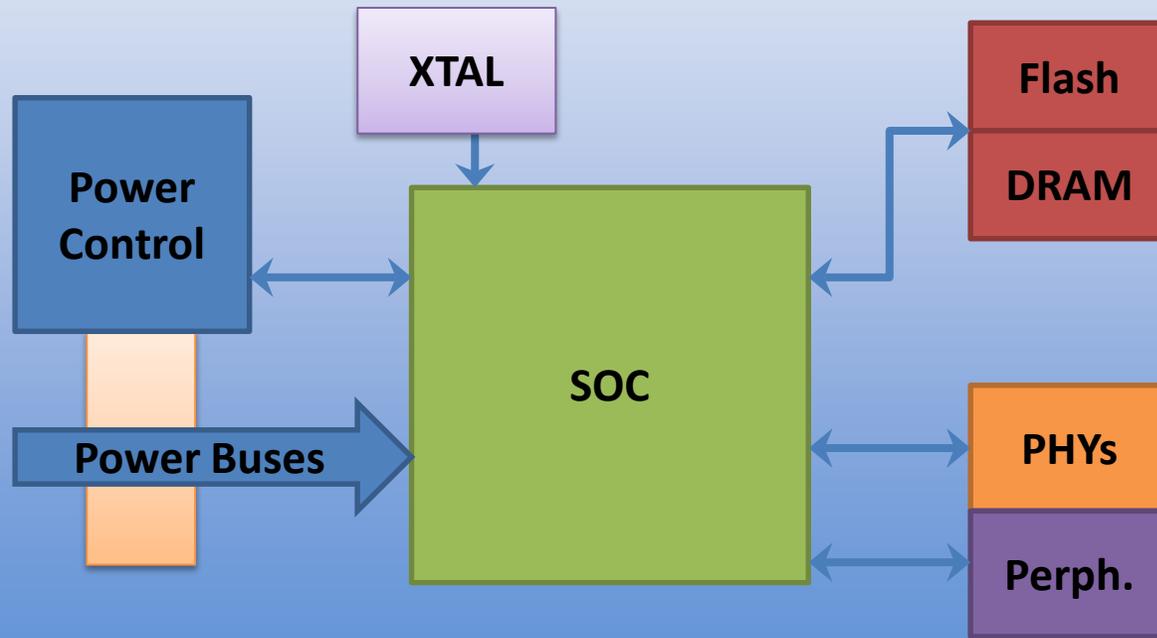
- most microcontrollers
- cell phone processors
- modern commercial processors
- BAE RAD5545
- HPSC Chiplet
- GR712, UT699/700
- nVidia Tegra series
- drone processors
- FPGAs (different topic)

Advanced Processors – ARM & Flight/RHBD - collaborative with BAE Systems, HSPC, others

Compare soft- vs. hard-ip ARM devices
- A5 Microcontroller SAMA5D3
- A5 FPGA/other hard-IP
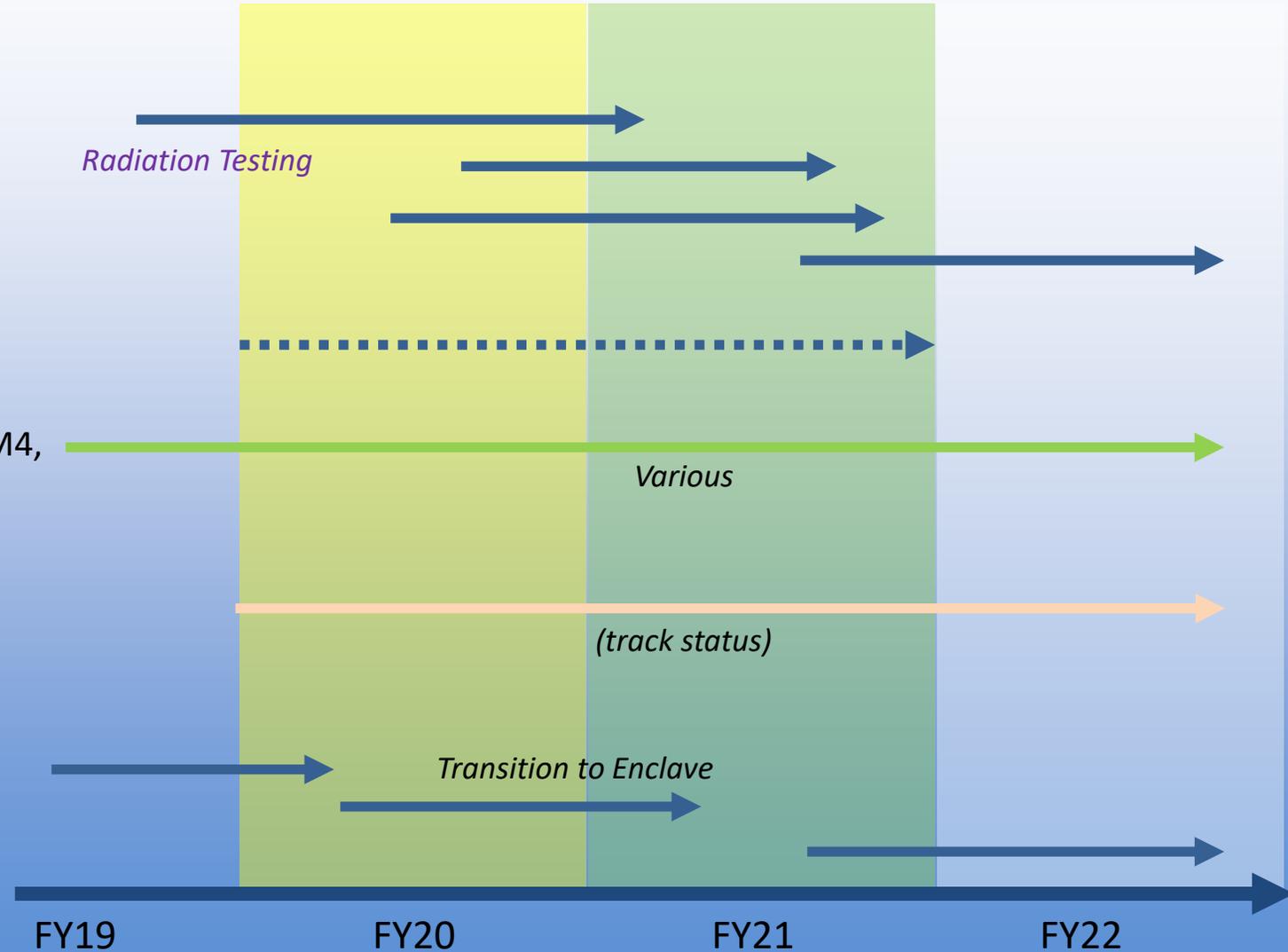- A5 soft IP
- A5x, 7x or 9x

ARM Fault Tolerance
- Dual R4 or R5

Additional Vorago/Cobham M0, M4, R5, etc....

High Performance Spaceflight Processor (HPSC)

Snapdragon General
- 835/845
- 855
- 865

Radiation Testing

Various

(track status)

Transition to Enclave

FY19   FY20   FY21   FY22

ARM Processors FY20 Plan (Pre C19)

Describe Proposal

 ARM processors and associated system-on-a-chip (SOC) devices represent a large portion of the commercial and aerospace markets. They provide a unique opportunity to determine architecture-specific and process-specific radiation effects sensitivity due to the availability of the processors across multiple manufacturers and architecture options (including FPGA soft-core processors).
 Previous efforts have collected data on SAMA5D3, Snapdragon 835, and 845. Efforts are currently establishing FPGA code for A5 implementation in soft-core, and for testing of Snapdragon 855 devices.
 ARM has expressed interest in exploring effectiveness of their fault tolerant architectures, and FY19 efforts have established a path forward on evaluating this, and collaborating with ARM.

Describe FY2020 Plans (including procurements >$10K)

Utilizing collaborator recommendations, A5 architecture soft-core and hard-core devices will be tested and compared.

Testing of fault tolerant dual-lockstep Hercules processors will be tested and results discussed with ARM collaborators.

Snapdragon 855 devices will be tested and compared to performance of 835 and 845 devices previously tested.

Procurements include: beam time, 15k; test boards, 10k

Enumerate Deliverables

1. Test report for hard/soft-core A5, Q1FY21
2. Test report for Snapdragon 855, Q4FY20
3. Test report for fault-tolerant ARM architectures (A5 focus), Q4FY20
4. Summary report for task, Q1FY21 (completed after activities finished using carry-over).

List Partners

Principal Investigator: Steve Guertin
NASA Co-Investigator(s): Andrew Daniel
Partners (NASA & Non-NASA Organizations): Ed Wyrwas (GSFC), UFRGS (Paolo Rech), ARM

Budget Request Summary (from Excel sheet)

NASA Labor	JPL Labor	NASA WYE	NASA CS Travel ($K)	Procurement ($K)
0.0	0.25	0.0	10k	15k

National Aeronautics and Space Administration

Year: FY2021
Lead Center: JPL
Type: RA
Category: Primary/Proposed Continuation]

**ARM SEE Testing
ARM Architecture SEE Fault Handling Across Implementations**

Describe Proposal

ARM devices are currently being used in many active missions as well as being an architecture favored for future processor designs. NASA and ARM lack understanding of implementation and effectiveness of ARM fault handling. ARM is fab-less, with various design-time configured parameters, each instantiation of ARM IP can have different SEE behavior.

In FY18/19 it was observed that fault-tolerant ARM devices have significant SEFI problems. ARM has indicated this may be due to the hardware manufacturers not implementing fault handling correctly, users not configuring it correctly, or potential flaws in the actual IP. FY20 activities are currently focused on implementing and testing A5 cores in nominal operation (FPGA&. In FY21 this will be expanded to target configuration and operation of ARM features to improve fault handling.

Arrangements with ARM and UFRGS will be finalized in FY20 to support these activities in FY21. Collaboration improves overall test capability, and understanding of test results. Because the A5 is relatively old, there is minimal anticipated risk to making results public.

Describe FY2021 Plans (including procurements >$10K)

1) Increase coverage of test capabilities targeting fault handling of A5 core and ARM-supported features (procuring DUTs, etc).
2) Fault handling/SEE injection testing of SAMA5D3 – focused on A5 core (beam charges anticipated ~10k)
3) SEE testing of FPGA implementation of A5 RTL (w/ARM support for FT configuration) (beam charges anticipated ~10k)
4) Final report bringing together performance across different A5 implementations, including recommendations for ASIC implementation of A5 at JPL. Report includes overview of FT configuration implicaitons.

To be presented by Steven M. Guertin at the

Enumerate Deliverables

1. Completion of test set up and test plans (Q2 FY21)
2. SEE test report for hard silicon devices SAMA5D3 & SAMA5D2C (latter comes from UFRGS collaboration)
3. SEE test report for FPGA A5 fault tolerant instantiations/options
4. ETW presentation of preliminary findings (Q3FY21)
5. Final report of findings (Q1 FY22)

List Partners

Principal Investigator: Steve Guertin/JPL

NASA Co-Investigator(s): Andrew Daniel/JPL

Partners (NASA & Non-NASA Organizations): E.Wyrwas/GSFC, P.Rech/UFRGS, R.Jeyapaul/ARM

Task	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
			Month - FY21										FY22		
Test Plans for Hard & Soft Core A5 IP			■	■	■	■									
SEE Tests for Hard & Soft Core A5							■	■	■	■					
Hard Core A5 Test Report								■							
Soft Core A5 Test Report											■				
ARM Collaboration	■	■	■	■	■	■	■	■	■	■	■	■			
ETW Presentation							■	■							
End of year Report														■	■

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Task Partnering

- Engaging in collaborative efforts:
  - NSWC Crane
  - Carl Szabo, Ed Wyrwas, Ted Wilcox, and Ken LaBel, GSFC
  - Jeff George, Aerospace Corporation
  - Larry Clark, ASU
  - Heather Quinn, LANL, and other members of the Microprocessor and FPGA Mitigation Working Group
  - Sergeh Vartanian, Andrew Daniel, and Greg Allen, JPL
  - Vorago Technologies – collaborating on hardware/plans
  - Paolo Rech – GPU/Applications, UFRGS, ARM Collaboration
  - Intel – informally
  - BAE Systems
  - AFRL
  - ARM collaboration – in formulation

- Looking for additional collaborators
  - Tester side – are you testing processors?
  - Manufacturer side – knowledge or hardware support
  - Application side – specific applications...

Device/Test-Specific Approach

- More specific NEPP Processor Enclave example
  - Focused on collaborative understanding of faults
  - Intention to obtain better operational and configuration information
  - Feed-back key information on effectiveness of fault handling
- ARM task FY20 is focused on Snapdragon 855 and ARM A5 processors implemented as hard-vs.-soft
- Also supporting processor telecon/collaboration within NASA and other government groups
- Positioning this work within efforts in the NASA, government, academic, and commercial priorities via collaborations and planning
- FY20/21 plans (with JPL's ability to carry-over FY20 funds, we expect to reach most of the FY20 plans)

Primary Goals

- We are working to get a handle on the architectural implications of SEE on the ARM platform
- ARM devices (even newer high performance cores) are implemented in many different silicon environments
  - Cell phone processors at 5nm, microcontroller devices at 100s of nm,
  - Provides opportunities to directly compare process nodes, and to get data on the newest process nodes
  - Not all implementations easily explored (e.g. "custom" ARM cores in phones)
- We would like to develop an approach that intelligently identifies what issues are inherent to the architecture, and what issues are primarily due to the fabrication
- Further, ARM cores (not just processors) have a significant number of configuration parameters that can affect SEE
  - Includes FT settings
  - In some cases devices are very well documented
  - Indication that ARM is interested in knowing how well their devices work in order to improve reliability options

Processor Enclave Justification

- We fully expect that just about anything under the Sun will be "tried" under the expanding commercial space sector.
  - Do we really understand the radiation implications, or knowledge limitations
  - Can there be guidance on how to determine appropriate risk vs. performance tradeoffs?
- Paradigm 1: How do we solve a set of problems/space applications
  - Take an application and determine what hardware is needed, can it be rad hard?
- Paradigm 2: What are the break points, in terms of performance and price, for various levels of system design and resilience
  - We think the enclave works best here
  - The obvious level – is to be knowledgeable about the current SOTA (see trap below)
  - But a spectrum, where 3-6 year old commercial "sweet spots", can be identified
  - At lower performance, fully rad-hard space processors are clearly the best solution
- Rick Alena pointed out on a recent telecon that we need to beware of the performance trap where we're looking at the highest performance stuff because it's the highest performance stuff.
- Periodic analytics report? – what's the current state... how do we have the data/results feed into a growing body of knowledge
  - What is the right way (or a way) to compare different architectures? Have we considered system SWAP?

The Raspberry Pi Example

- The Raspberry Pi is interesting to explore
  - Lots of users – it's a Linux computer with GPIO!
  - It's so cheap and simple, it draws in hobby hardware solutions
  - But it is also used to run certain processing tasks
- ~~What if~~ When someone wants to fly it?
  - Astro Pi: ESA has an ISS box that is a space-hardened Raspberry Pi; NASA also has its own Pis as well
  - Flying these is not much different than the lower-end microcontrollers in some of the cubesat kits

Obligatory photo of Raspberry Pis floating in space!

https://www.raspberrypi.org

Migrate to this?
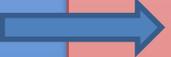
Why Using Pi?	Toggle IOs	Running Software	Semi-RT Application and Hardware Optimized for Pi
Alternate Solution	Rad Hard Microcontroller	Lots of other space computers	Limited – Pi might be best solution
Cost to achieve high reliability:	Low (even though devices are $5k+)	Depends on processing requirements $5-500k	High/not possible; rel. limited – recommendations can be made.

ARM Collaboration

- Currently in process to finalize a research agreement with ARM
- Initial goals are to try to understand the expected performance of an A5 processor during beam exposure
  - Space environment can double for natural environment for faults
  - Inject faults into ARM processors running in various configurations
- ARM has a set of fault handling approaches
  - Cache protection (including L1 ECC)
  - Dual-core lockstep; multi-core multiple execution
  - Parity protection on bus control, ECC on data
- Multiple hard core devices, and access to soft-core generator is planned
  - At architecture build time there may be options that impact fault handling
  - Comparison across multiple technologies/processes of essentially similar hardware

Snapdragon Test Development/Methods

- Video playback test

- 3DMark benchmarking software

- Also porting some specific benchmark codes
  - Don't expect standard benchmarks to be of significant benefit
    - This is an SOC, not a processor – need SOC benchmarks...
    - SOC benchmarks are inherently not well defined...
  - But exploring altering the benchmarks for modern devices – e.g. Mean Work To Failure (MWTF) based on which resources are used – DSP, multiple cores, etc

Snapdragon 835

- Samsung 10 nm
  - 8 Kyro 280 CPUs
  - Adreno 540 GPU
  - Hexagon DSP

- Using Intrinsyc's
  835 Mobile Hardware
  Development Kit – Android only,
  which is not desired...

- This board uses package-on-package (they essentially all do)

- No avenue to put Linux on the board.
  - Linux gives us more ability to understand how the it actually runs...

Snapdragon 845

- Samsung 10 nm
  - 8 Kyro 385 CPUs
  - Adreno 630 GPU
  - Hexagon DSP

- Using Intrinsyc's 845 Mobile Hardware Development Kit – Android only from factory, which is not desired…

- Supports yocto Linux.

Snapdragon 835/845 Update

- Extended Snapdragon 835 and obtained Snapdragon 845 data (same 10 nm process)
- 835: SEFI behavior: 1×10^{-4} cm^2 for LETs under 2 MeV-cm^2/mg, increasing to 3×10^{-4} cm^2 for LET ~6.9 MeV-cm^2/mg
- 835: Up to an LET of about 2 MeV-cm^2/mg the cross section for L2 bit errors was on the order of 1×10^{-11} cm^2/bit. This cross section did not significantly change up to LET 6.9
- 845: (only tested at 6.9 MeV-cm^2/mg): SEFI behavior: 2×10^{-4} cm^2
- 845: About 4 L1/L2/L3 bit errors per SEFI – gives device-level bit error cross section of about 8×10^{-4} cm^2 at LET 6.9 MeV-cm^2/mg
  - We lack understanding of the cache bits used in the testing to compare this to the 835. The per-bit sensitivity is expected to be about the same.
- Both 835 and 845 SEFI cross sections are much higher than the DDR2 SEFI cross section
  - Test ions had to travers both the DDR4 device and the processor
- Results independent of the test program used (video playback or graphics benchmark program)
  - All tests operated under the Android OS
  - Maybe slightly different mix of L2 correctable bit errors (statistics)

Snapdragon 855 – FY20/early 21

- TSMC 7nm
  - 8 Kyro 465 CPUs
  - Adreno 640 GPU
  - Hexagon 690 DSP/tensor accelerator

- Using Intrinsyc's
  855 Mobile Hardware
  Development Kit
- Initial plan same as 835/845 –
  - Android apps, crashes, error reports
  - Allows comparison to other Snapdragon but limited comparison to other devices
- Also, doing this effort within
 the Enclave approach

ARM A5 General Approach

- A5 is one of the lower end ARM processors, but we have some access to how it works via collaborators
  - Evaluate effectiveness of fault approach
  - Understand SOC-integration impact on fault approach in SAMA5D3 and SAMA5D2 (latter via collaborator)
  - Identify operational mode, OS, and other configuration details that impact fault handling
- First stage is basic error performance of the A5 in SAMA5D3 <- FY19
- Second stage is errors in SAMA5D3 with various FT config <- FY20
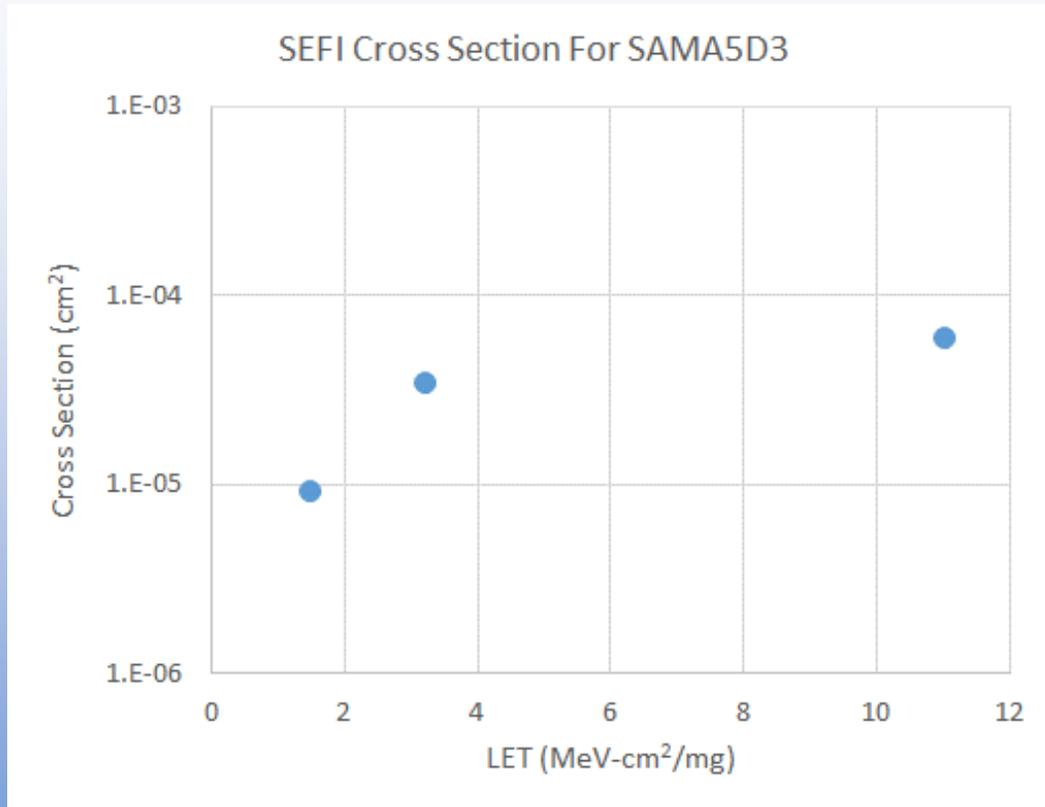- Third stage is A5 performance when implemented on an FPGA <- FY21

SAMA5D3 - Example

- A5-Based Microcontroller

- Xilinx UltraScale+ MPSoC has dual-core A5s for comparison
  - (And comparison to on-chip quad-core A53)

- Also working on getting A5-IP via collaboration

Basic Sensitivity
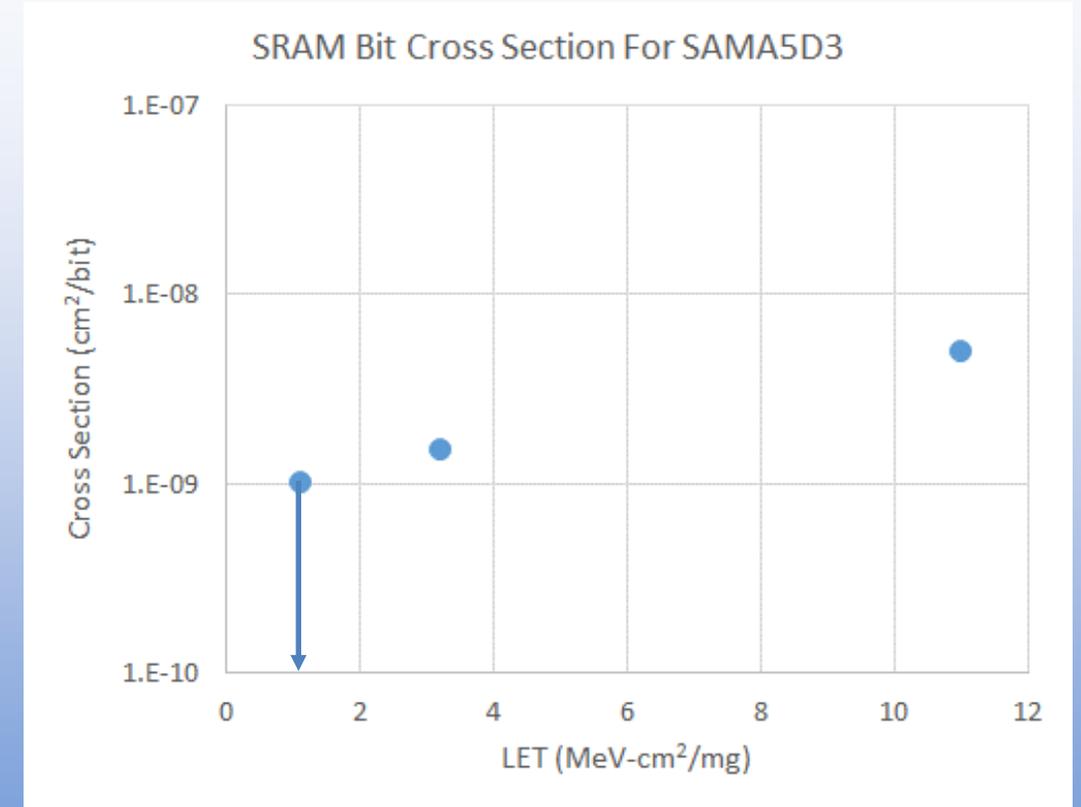

SEFI Cross Section For SAMA5D3

SRAM Bit Cross Section For SAMA5D3
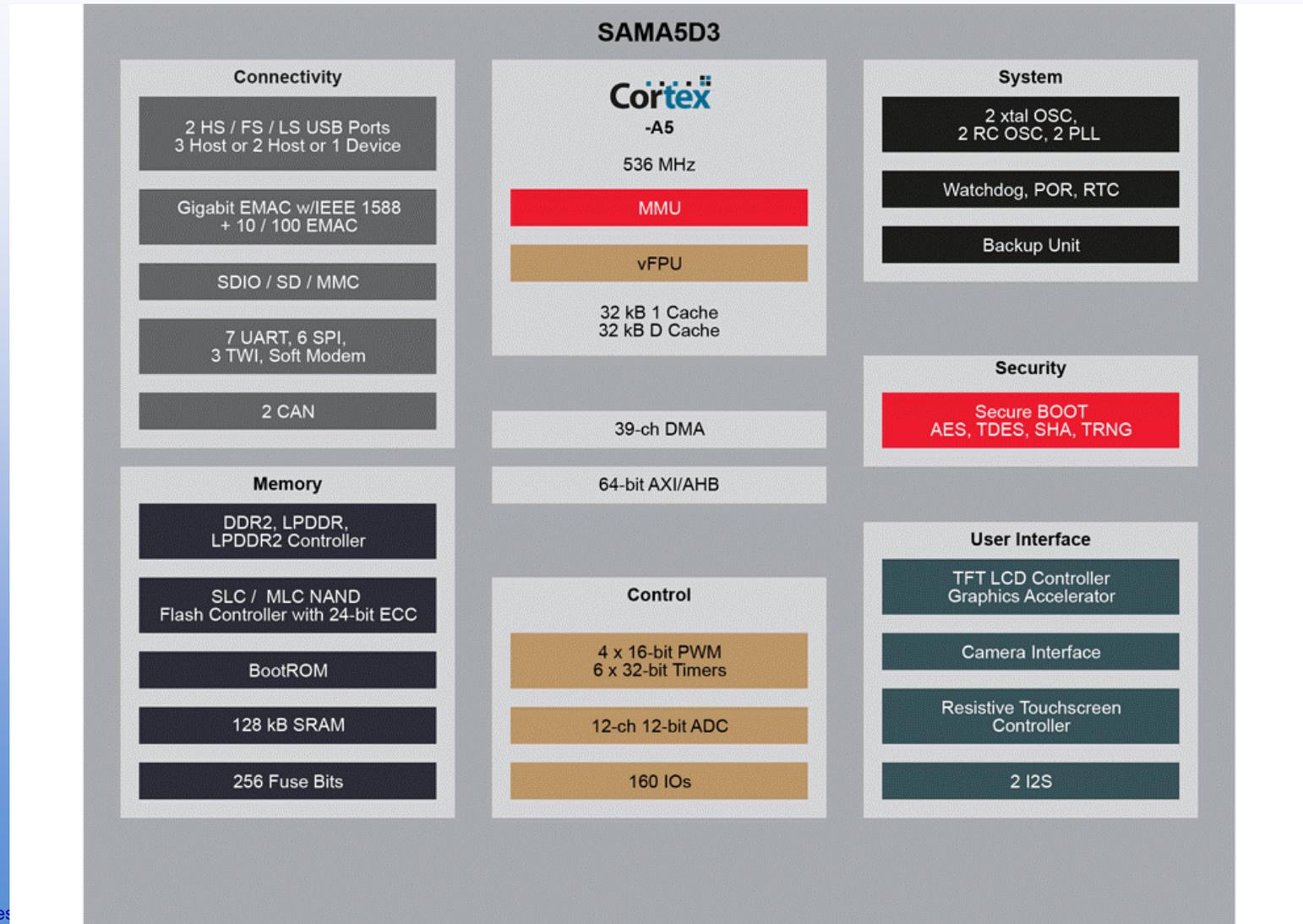
- Crashes were more likely to occur than execution errors

- Memory bit errors were easiest to extract with debug tools
- Software crashes limited in-situ data extraction (i.e. memory test programs).

A5 Plans this FY, when labs online

- ARM has expressed interest in helping run simulations.
- Use simulation, software configuration, and detailed hardware options to highlight shortfalls of core-level simulation.
  - There have been some community papers (recently) that explore the order-of-magnitude higher crash rates in SOCs, compared to detectable errors. (TBD: can I get some references here).
  - Target simulations to the appropriate level.
- Heavy ion irradiations of various system configurations
  - Observable errors vs. system-wide crash/hang/SEFI
  - Based on recommendations from collaborators
  - A5, and SAMA5D3 represent a corner of the ARM space, but they can be good vehicles for adding value to this effort. More advanced processing cores?
- Get basic A5 soft-core implementation online, begin migrating SAMA5D3 code
- Extract general information for use with all processor types.

Future

- Tests planned (heavy ion):
  - Snapdragon 855 with current approach, late FY20, early 21
  - Snapdragon 855 with Enclave approach – early 21 (pushing)
  - ARM Cortex A5 (SAMA5D3) with multiple fault configurations – late FY20, early 21
  - Collaborative/alternate A5 device with hard-core A5 – late FY20, early 21
  - ARM Cortex A5 soft/hard core IP comparison test with FPGA implementation – mid to late FY21 (plan currently under review)
- Extract critical info on what fault tolerance works and what doesn't, in order to help specify fault tolerance settings in ARM devices.

Conclusions

- ARM collaboration (ARM and UFRGS) and Processor Enclave helping to define this task
  - Fault-Tolerant, Mitigated ARM device data gives good feedback on effectiveness of mitigation options offered, possibly influencing future mitigation offerings from ARM.
  - Expecting support for fault tolerance hardware operation
- Reported FY19 updates on Snapdragon 835 and 845 testing – no surprises
- Reported FY19 initial SEE sensitivity of SAMA5D3
- FY20/21 plans call for: (FY20 test efforts are somewhat delayed)
  - fault tolerance configuration comparison for A5 processors
  - Snapdragon 855 testing using current approach and Enclave approach
- Positioning ARM-specific understanding/research in the context of the broader community, NASA needs, and in collaboration to understand proper configuration and improve fault handling.
  - Collaborations, ongoing biweekly meetings in support of this effort.
- Multi-angle approach allows isolation of architecture-specific and fabrication-specific behavior.
  - Additional manufacturing platforms allow us to better handle some limited documentation issues.

Processor Enclave Biweekly Call

- Please let us know if you are interested in participating
  - Looking for other doing testing of commercial devices and next-generation RHBD devices
  - Primary goal of the call is to try to minimize overlap and maximize testing and effectiveness of testing within NASA and participating government programs

  - Assistance is helpful from: testers, manufacturers (including ARM, RISC V, etc.), and applications designers (what do you guys really need?)
  - Or if you have a program and are looking for data or are interested in helping shape upcoming testing
- Next call is 6/19/2020
  - Planning to review ETW presentations with anyone who wants to call in (contact Ed Wyrwas, Steve Guertin, Jonny Pellish, or your favorite NEPP person)
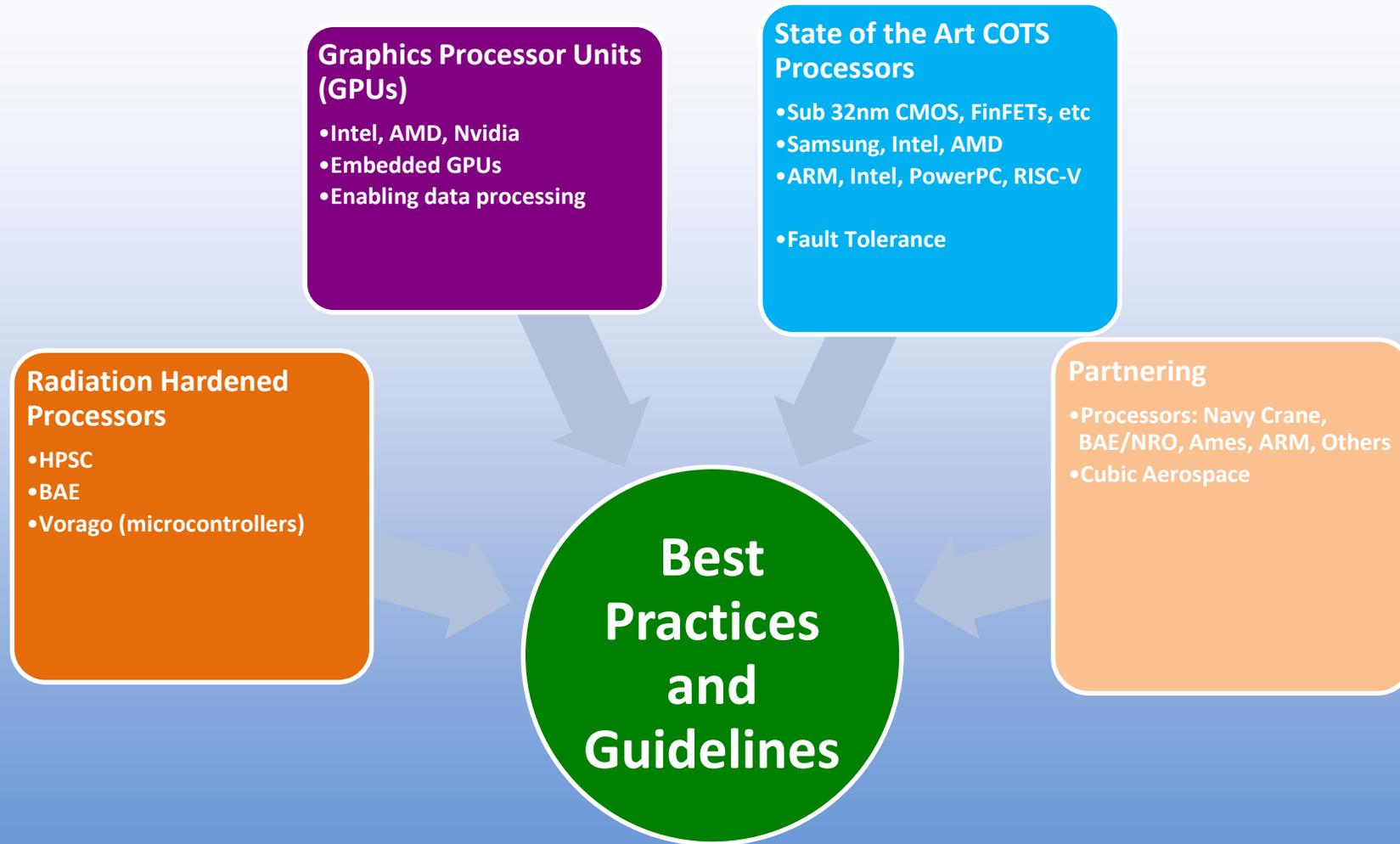
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Overview

- This task is part of the Processor Enclave.
  - Focused on ARM-architecture and devices
  - For FY20/21 – Snapdragon general testing; ARM collaboration and testing
    - Snapdragon is for general commercial approaches for specific devices
    - "ARM" effort is focused on architecture and fault tolerance and handling methods
- Focused on ARM processors, and the modern architectural push to SOCs with many (sometimes new) on-chip functions.
- An architecture-specific target and has picked up collaborators that help position it a little differently.
  - Keeps efforts focused, somewhat.
  - The hope is to keep the approach and findings more generalized.
- It also sits in a position in the overall approach to be an example of how the Processor Enclave is dealing with certain questions that cross over between commercial and rad-hard space.

NEPP – ARM Processors and Context

Graphics Processor Units (GPUs)

- Intel, AMD, Nvidia
- Embedded GPUs
- Enabling data processing

State of the Art COTS Processors

- Sub 32nm CMOS, FinFETs, etc
- Samsung, Intel, AMD
- ARM, Intel, PowerPC, RISC-V

- Fault Tolerance

Radiation Hardened Processors

- HPSC
- BAE
- Vorago (microcontrollers)

Partnering

- Processors: Navy Crane, BAE/NRO, Ames, ARM, Others
- Cubic Aerospace

Best Practices and Guidelines

Focus Categories

- **Architecture – to support evaluation and use of processor architectures throughout NASA, including processor types and FPGA/Soft processors**
  - **ARM-specific effort – Can we identify appropriate methods for ARM devices – identify architecture-specific and implementation-specific issues?**
- Implementations – to support evaluation and use of primary form-factors
- **Fabrication Facilities/Technology – to obtain information on fabrication facilities and related technology (e.g. Samsung 7nm, 3D, Automotive, etc.)**
- Application/Use Case – to support ways of using devices for different NASA needs
- Develop data on specific devices/Methods for evaluation – support actual flight use, and understand that in many cases the project will have to evaluate their own part (but we can provide guidance)
- Manufacturers – to have an up-to-date tool set for understanding devices from various manufacturers.
- Collaborations – to engage manufacturers when they are available or can work with us, we want to harness this
- **Test Reports, Test Methods, Guidelines, BOKs**

Why ARM?

- Modern SOCs can't be considered stand-alone processors
  - Support devices must be considered, especially buses

- ARM or ARM support devices are used in many modern SOCs
  - Allows compare & contrast test approaches across similar-but-different devices

- In many cases, the architecture is well-documented
  - Especially in FPGAs how to properly use resources

Next Gen Space Computing

- Most research into processor faults is being done on simpler devices.
- Aside from cubesats and very low budget missions, almost anything simple can have its radiation risk mitigated by using $5k microcontrollers – which actually save a lot of money.
- There is a growing interest in figuring out how to use low power, high performance architectures off the shelf, or with minimal radiation improvements.
- The market is not in simple devices – it is in neural processors, 8/16+ core heterogenous processors.
  - Complex control architectures with a lot of hidden daemon-like resources
    - System monitors in the fabric – for use with debug tool (cannot be disabled)
    - If you could tap into these, it might help… but you probably can't
  - But they also have so much additional stuff on-board that redundancy is baked in