Status of NEPP Radiation Testing
3D NAND Flash

Ted Wilcox

ted.wilcox@nasa.gov
NASA Goddard Space Flight Center
# Acronyms

- **BER**: Bit Error Rate
- **CBRAM**: Conductive Bridge RAM
- **CMOS**: Complementary Metal-Oxide Semiconductor
- **COTS**: Commercial Off The Shelf
- **CP**: Charge Pump
- **DRAM**: Dynamic Random Access Memory
- **ECC**: Error-Correcting Code
- **EDAC**: Error Detection and Correction
- **EEPROM**: Electrically-Erasable Programmable Read-Only Memory
- **FRAM**: Ferroelectric RAM
- **GEO**: Geostationary Earth Orbit
- **LET**: Linear Energy Transfer
- **MBU**: Multiple Bit Upset
- **MCU**: Multiple Cell Upset
- **MLC**: Multi-level Cell
- **MRAM**: Magnetoresistive RAM
- **NAND**: Not AND (Flash Technology)
- **NEPP**: NASA Electronics and Packaging Program
- **NOR**: Not OR
- **NVM**: Non-Volatile Memory
- **PCM**: Phase Change Memory
- **QLC**: Quad-level Cell
- **RBER**: Raw Bit Error Rate
- **SBU**: Single Bit Upset
- **SEE**: Single Event Effects
- **SEFI**: Single Event Functional Interruption
- **SEU**: Single Event Upset
- **SLC**: Single-level Cell
- **SSD**: Solid State Drive
- **SSR**: Solid State Recorder
- **STT-MRAM**: Spin-torque Transfer MRAM
- **TID**: Total Ionizing Dose
- **TLC**: Triple-level Cell
- **UBER**: Uncorrected Bit Error Rate

To be presented by Ted Wilcox at the 2020 NEPP Electronics Technology Workshop (ETW), NASA GSFC, Greenbelt, MD, June 17, 2020.
Outline

• NEPP Focus
• State of 3D NAND Flash
• Typical Memory Test Setups
• Summary of Past TID & SEE Results
• Hynix 72-layer Heavy Ion / Proton data
• Future Plans
NVM Technologies Of Interest to NEPP

NOR Flash
- Electrical charge
- Random Access
- Low Density
- Simple interface
- Limited endurance
- Varied rad tolerance
- Example Usage: FPGA configuration

NAND Flash
- Electrical charge
- Seq Access
- Highest Density
- Complex interfaces
- Very limited endurance
- Limited rad tolerance
- Example Application: bulk data storage

FRAM
- Ferroelectric orientation
- Random Access
- Low Density
- Simple interfaces
- High endurance
- Rad tolerant

ReRAM, 3DXPoint, PCM, CBRAM
- Resistive memory
- Random Access
- Lowest to Highest Density
- Varied interfaces
- Very high endurance
- Excellent rad tolerance
- Still developing…

STT-MRAM
- Electron spin
- Random Access
- Lowest* Density
- Simple interfaces
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All of interest to NEPP, but today’s focus is NAND Flash
Typical 3D Flash Overview

- Each plastic BGA package contains 1-16 dice stacked
- Each die contains 32-96 layers (~2020) of charge trap or floating gate transistors in a vertical string
- Each transistor stores 1-4 bits
- Total $\rightarrow$ 8+ Tb per component

42 Terabytes visible in this photograph
State of 3D NAND Flash

- Planar NAND flash scaled to its practical limits years ago
- Virtually all consumer NAND flash is 3D NAND
  - Micron and Intel 96L → 128L and 144L (11% + 10% market share)
  - Hynix 96L v5 → 128L v6 (11%)
  - Samsung 92L V-NAND 5 → 128L V-NAND 6 (33%)
  - WD and Kioxia 96L BiCS4 → 112L BiCS5 (15% + 19%)
  - YMTC 64L → 128L
- Not just 3D, but multiple bits per cell
  - MLC is standard for enterprise, TLC standard for consumer devices, QLC for “write once read many” applications
- Mil-Aero reliant on past generations of planar SLC
  - Reliable, but available? Scalable?
- Multiple vendors, multiple technologies, 128+ layers to consider!
Past NEPP 3D NAND Testing

- **2016/2017:** Samsung 32L V-NAND SSD, Hynix 36L NAND parts
- **2018/2019:** In-Depth Characterization: Micron 32L NAND → Flight
- **2019/2020:** Hynix 72L

**Focus:**
- Evaluate broad trends in TID and SEE response
- Characterize trade-offs in performance
  - SLC vs MLC or TLC? Voltage?
- Understand complex effects
  - SEFI Modes, MBUs vs Multi-Level Upsets, Destructive SEE, retention/endurance changes, irradiation bias effects, etc.
• Three-dimensional ion track structure can be determined experimentally, and results look exactly as you’d expect:
Refresher on Past Results -- 3D NAND Flash TID

- Well-established that erase circuitry is weakest link for TID (high-voltage CPs)
- Commonly fail 20-75 krad (Si) while program and read circuitry may last longer
- In continuous rewrite application, retention errors are minimal but eventually we can’t program clean data
- This is not an easy 100krad technology
Refresher on Past Results -- 3D NAND Flash TID

- Storage cells may outlast erase circuitry, as in Micron 3D NAND (SLC)
- Don’t assume uniform error distribution

~50 krad irradiated in opposite directions
Refresher on Past Results -- MLC vs SLC

- So far, applications seem to be using SLC devices or “SLC mode” if at all possible – for performance and endurance, not radiation
- MLC and beyond increase density but at what cost to rad tolerance?
Typical Test Setup

• Favor flexible, inexpensive testers to adapt to new part types
• Adjust test routines quickly / on-the-fly
• “Throw away” hardware after TID/Proton testing
• Challenges include documentation, piece-part access, decapsulation
ON TO THE NEW DATA:
SK HYNIX 72 LAYER 3D NAND
Hynix v4 72L 3D NAND Flash

H25QFT8F4A9R-BDF
Eight-die stack, each 512 Gb TLC
55 nm vertical pitch
3x nm bit line half pitch

82 layers fabricated
72 active layers of charge trap NAND
Logical NAND strings are 144 cells long, wrapping around a “U” at the base

Images used with permission, courtesy of TechInsights
Heavy Ion Testing

Memory Cell SEU
- Powered off state to isolate from control circuitry
- Powered on and dynamic tests to evaluate differences
- Consider number of bits relative to fluence
- SBU vs. MBU, angular effects, data pattern, etc

Peripheral Circuitry
SEFI
- Powered on and operating dynamically
- Depends on underlying tech, but can reveal error signatures typical for a memory type

Memory-Specific Hard Failures
- Stuck bits
- Broken program/erase circuits

TID Tolerance
- Evaluate all operational modes
- Irradiate in appropriate conditions (worse case? flight-like?)
- Failure distributions, lot-specific testing issues

Single-Event Latchup
- Powered on, static and dynamic
- High voltage and temperature
- Focus on power supply and recovery, less on SEFI that will inevitably occur
- Strongly dependent on fab process

Ideal
Helpful
Not Useful
Heavy Ion SEU Results

I wonder what happens here?

Heavy ion data helpful to verify decoding technique
Heavy Ion SEFIs

• As expected, Hynix v4 72L devices show many complex SEFI modes that generally prevent I/O until power cycle
• Comparable to previous parts
  – SEFI LET\textsubscript{th} between 1.5 and 7.3 MeV·cm\textsuperscript{2}/mg
  – LET\textsubscript{SAT} ~ 5x10\textsuperscript{-5} cm\textsuperscript{2} (per die)
• Can be handled with intelligent system design and fault tolerance
What about destructive failures?

• Recent tests, most notably Micron 32L parts intended for flight, did not show any destructive failures under any testing
  – Even at 80°C, absolute maximum supply voltage, LET > 75 MeV·cm²/mg
• However, two Hynix 72L samples were completely dead after irradiating with LET of 58.8 MeV·cm²/mg.
• More study is likely, but these test campaigns were primarily focused on the memory array and not specific component’s usability.
Why Low Energy Protons?

• Several test runs showed $\text{LET}_\text{th}$ for SEU less than lowest easily available LET at our test facilities
  – These are the highest fluxes in space
  – How do highly-scaled devices behave?

• We wanted to use the ultra short range – and tunability – of low energy protons to explore the three dimensional structure of NAND
Low Energy Protons – What Might Happen?

• By adjusting accelerator energy, we can vary placement of peak LET in increments of ~1 um. Memory stack is ~4.5 um thick.
• If device upsets, we should be able to move the Bragg Peak around the vertical depth of the memory array.
Direct Ionization by Low Energy Protons

- Direct ionization by low energy protons should have a distinct peak where LET is maximized
- We can see that quite clearly at ~700 keV
Low Energy Proton Upsets by Layer

To be presented by Ted Wilcox at the 2020 NEPP Electronics Technology Workshop (ETW), NASA GSFC, Greenbelt, MD, June 17, 2020.
Movement of Bragg Peak within Memory Array

Errors sorted by logical page and byte addresses

Errors sorted by physical layer and byte addresses

Histogram by physical layer

Proton Energy

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Are Protons Just Piling Up?

- Multiple protons with LETs insufficient to directly flip a cell could strike the same cell during test.
- But, analysis shows at these fluences, multiple strikes should be virtually nil – and slope of error vs. fluence would be different.
Takeaways

• 3D NAND Flash
  – Continues to scale vertically and in bits per cell, but rate is slowing
  – Piece-part testing is absolutely critical to understanding effects at the memory level
  – Remains sensitive to SEU, but given other factors that cause routine error corruption, SLC operation appears quite reasonable for spaceflight
  – However, unpredictable SEFI risks exist and are compounded by complex structures, and
  – Some parts continue to exhibit unusual destructive effects

• Future Plans
  – Hynix 72L electron testing and \textit{TID testing} in 2020
  – Micron 96L or 128L and Hynix 96L SEE testing in 2021
  – Re-visit Hynix 72L destructive SEE mode