Xilinx Zynq SoC Upscreening for EMIT Project

Jason Heidecker, Digital Part Specialist
Parts Engineering & Reliability Group (5141)

Jet Propulsion Laboratory
California Institute of Technology

Table of Contents

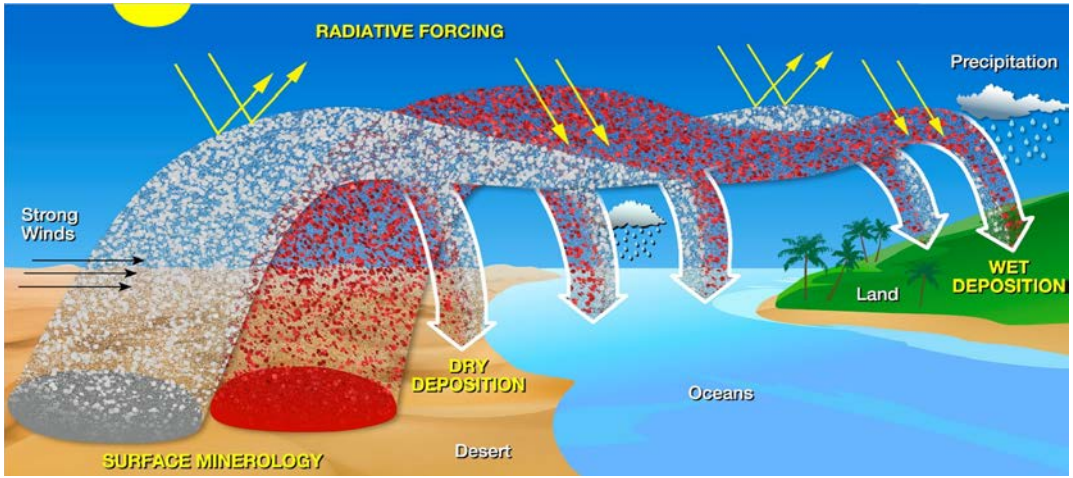
EMIT - Earth surface Mineral dust source InvesTigation

- Mission to map the surface mineralogy of deserts via imaging spectroscopy in the visible and short-wave infrared. The maps of the source regions will be used to improve forecasts of the role of mineral dust in the radiative forcing (warming or cooling) of the atmosphere. i.e. *Predict the increase or decrease of available dust sources under future climate scenarios.*

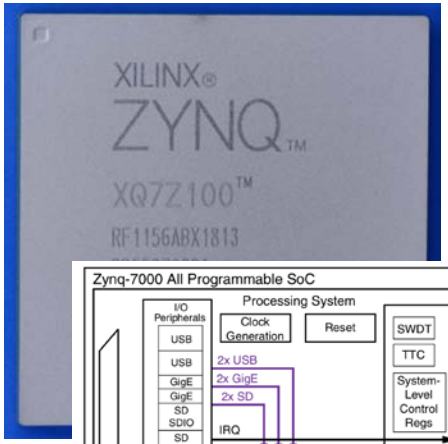
- NASA Class C (NPR 8705.4)

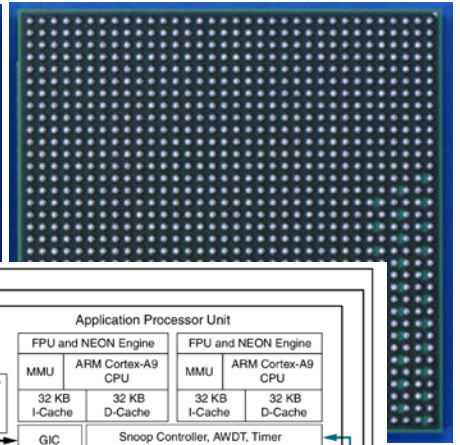
- 1 year mission on ISS

- Level 2 parts requirements – *100% screening and lot qualification required*



Xilinx Zynq SoC - XQ7Z100-2RF1156I





- *Defense-grade* Zynq-7000Q All Programmable SoC
- “UltraScale” 28 nm CMOS flip-chip
- On-package BME caps (25 total)
- Ball grid array (BGA) package (1156 balls; Eutectic / 63Sn-37Pb)
- Processing System (PS)-
  dual-core ARM® CortexTM-A9
- Programmable Logic (PL)-
  CLB, RAM, DSP, I/O, JTAG, PCI Express, Serial TxRx, ADC

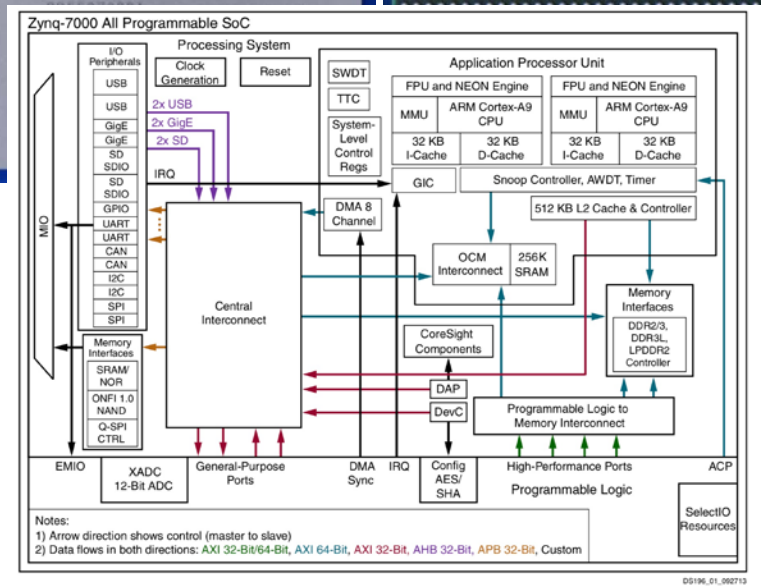


Figure 1: **Zynq-7000 All Programmable SoC Overview**

State-of-the-Art SoC on Small/Accelerated Mission...

- Zynq SoC is most complex microcircuit screened by 514.
- Ideally, much more NRE would be involved compared to other screening jobs.
- Unfortunately, EMIT schedule allowed *less* time than normal.
  - 12 weeks NRE phase for this task, compared to ~12 months* Xilinx spent on developing test program for Zynq-7000.

Theme of this presentation:

What is achievable by end-user when trying to screen advanced SoC to space requirements?

Constraints on this activity:

No involvement from Xilinx.
No application-specific circuit.

**Source: hallway conversation with Xilinx.*

Xilinx Defense Grade

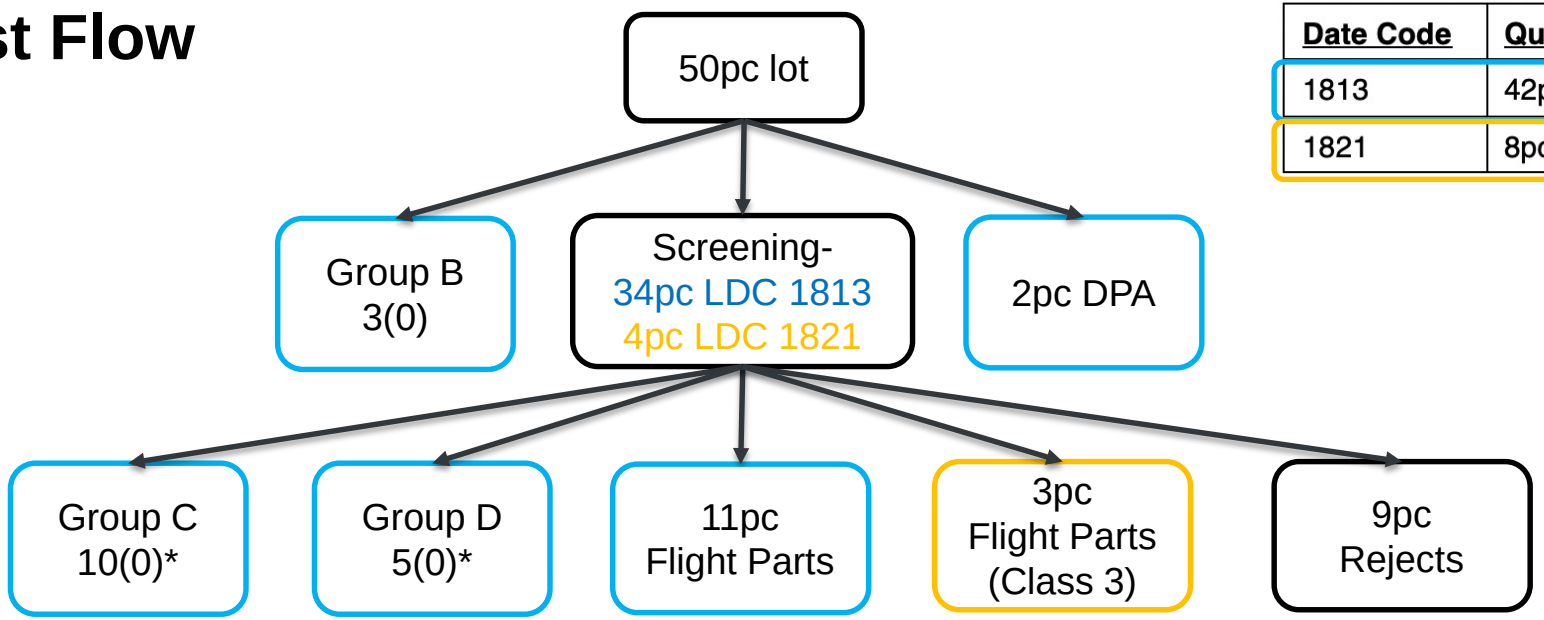
- *One-time* MIL-STD-883 Group D (does not meet Class Q/V periodicity requirements)
- Screening consists of only 40C/+25C/+100C electrical testing

EMIT Requirements (PETS Class 2, Based on 38535 Class Y)

- Screening with temp cycling, burn-in, CSAM
- Group B – *Die and Ball Attach Verification*
- Group C – *Life Test*
- Group D – *Package Qual*
- DPA

Screening and lot qualification requirements captured in JPL general specification 10437407 for non-hermetic flip-chip microcircuits.

Test Flow



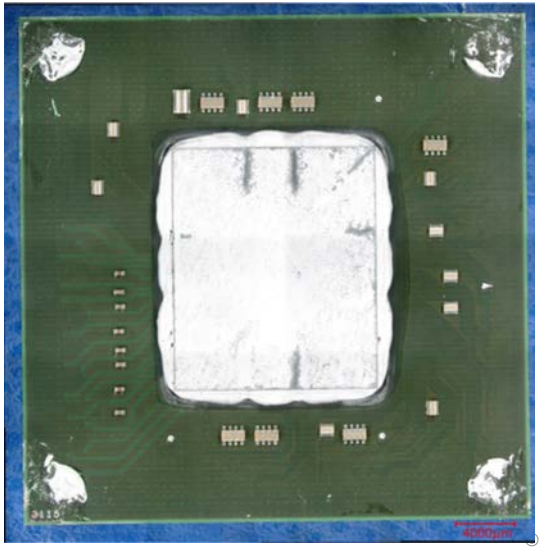
Date Code Breakdown

Date Code	Quantity
1813	42pc
1821	8pc

1. Group B is typically done on screened parts to reduce risk of failing qual, however for this lot Group B was done on unscreened parts to get more information faster for EMIT project.
2. DPA originally 2pc, later became 4pc as two electrical rejects were sent to complete DPA steps.
3. ”Rejects” include handling failures, delta failures, BGA socket failure during burn-in
4. 3pc passing screening from LDC 1821 can only be used for PETS Class 3 since LDC 1821 did not get DPA, Group B, etc. (only subjected to screening)
5. * Reduced sample sizes require waiver. Group C requirement: 22pc. Group D: 15pc.

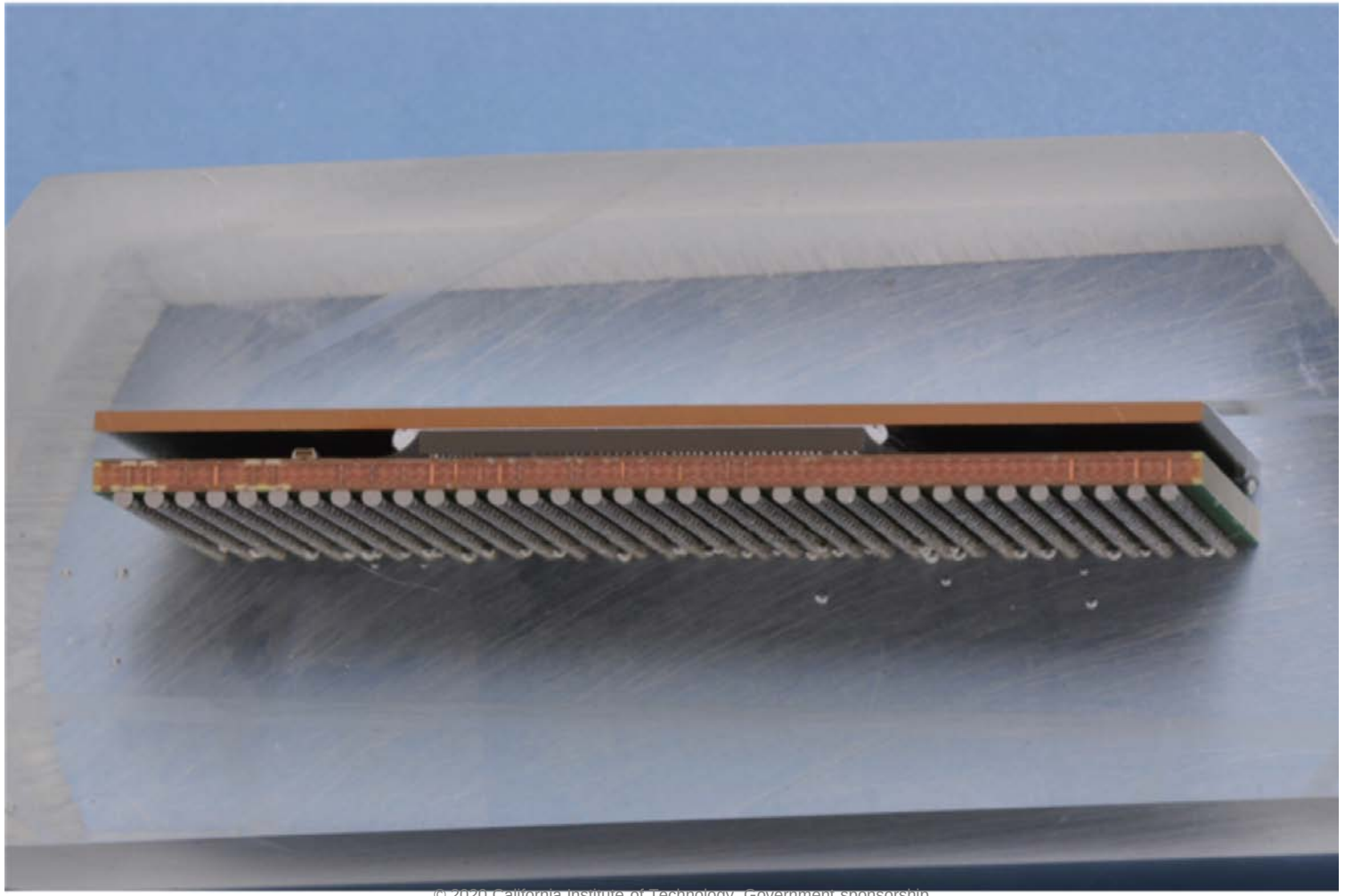
DPA - Pass

- Originally sent 2pc for DPA
- Unable to complete all test steps on first 2 samples
- Additional 2pc (electrical rejects) sent to complete the testing
- No anomalies or significant findings.



DPA Test Steps

Test	Test Method
External Visual	MIL-STD-883, TM 2009
Configuration	MIL-STD-883, TM 2016
Prohibited Material Inspection (External)	MIL-STD-1580, Req. 9
X-Radiography	MIL-STD-883, TM 2012
Acoustic Microscopy (CSAM)	MIL-STD-883, TM 2030
Ball Shear	JESD22-B117
Internal Visual Inspection (Post Lid Removal)	MIL-STD-883, TM 2010
Prohibited Materials Inspection (Internal)	MIL-STD-1580, Req. 9
Glassivation Integrity	MIL-STD-883, TM 2021
Cross-section Inspection Including Metal Thinning Inspection	MIL-STD-883, TM 2018



100% Screening Tests

TEST DESCRIPTION	MIL-STD-883 TEST METHOD	CONDITION
Serialization		
External Visual	2009	Cond. A
Temperature Cycling	1010	Cond. C (10 cycles)
Electrical testing		-40°C, +25°C, +100°C
Burn-In (dynamic)	1015	Cond. D. max 125C T_J 168 hours
Electrical testing		25C
Delta Calculations		
Electrical testing		-40°C, +25°C, +100°C
CSAM	2030	
External Visual	2009	

Electrical Tests

The electrical test program is 2911 measurements per part, per temperature:

- Continuity checks
- Leakage currents
- t_{CO}, t_{PD}
- V_{IL}, V_{IH}, V_{OL}, V_{OH}
- Two functional tests at min/max/nom supply voltage:
  - IO Test
  - MicroBlaze Test
- Supply currents for V_{CCINT}, V_{CCAUX}, V_{CCO}

Electrical test program is performed:

- Pre/post burn-in
- Pre/post interim life test
- Post Group D

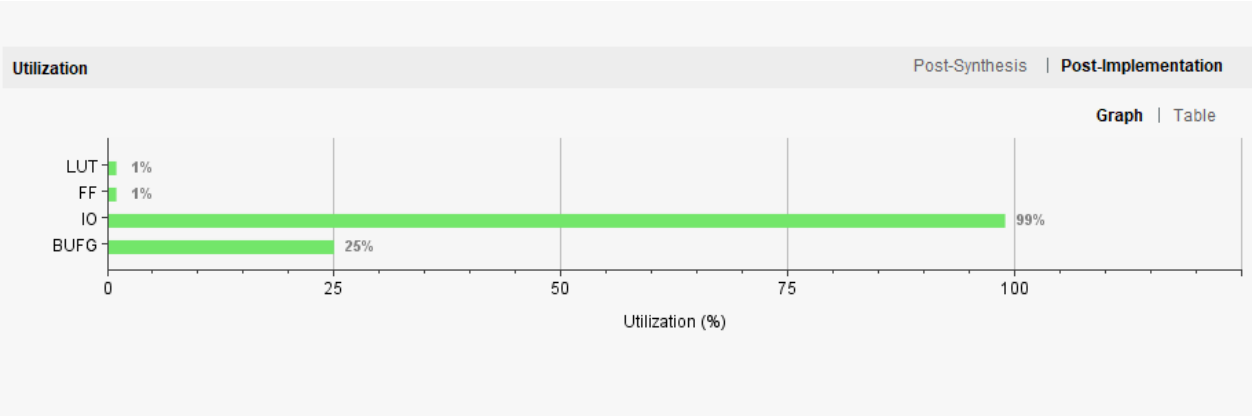
Electrical Test Challenges With Advanced SoC

- Expedited NRE schedule imposed by EMIT project led to unresolved issues with test setup. **Complex SoC requires much more time for NRE, not less!**
- Burn-in and electrical test relatively limited compared to what could be done by part manufacturer or with an application-specific circuit; therefore, **residual risk to projects using the lot as the parts are not 100% tested (see next slide).**
- Inconsistent results with “MicroBlaze” test. 18/38pc were failing under various temp/voltage combinations. **Not enough schedule allowed for debug. Test became “for informational purposes only”.**
- **Did not test Processing System.**

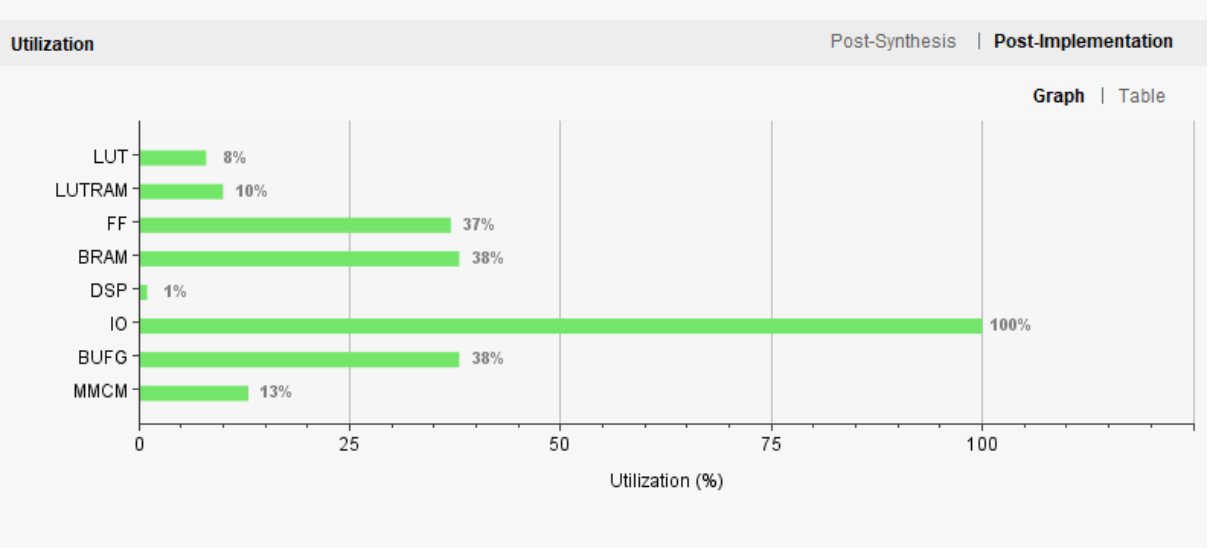
Strongly recommend screening with application-specific circuit, exact same design as mission if possible. Traditional ASIC requirements like “>95% fault coverage” for entire chip is not possible with advanced SoC.

Zynq SoC Resource Utilization During Functional Testing (Processing System not tested)

Before MicroBlaze (IO test only):



After adding MicroBlaze:



Limitations of Burn-in and Electrical Test

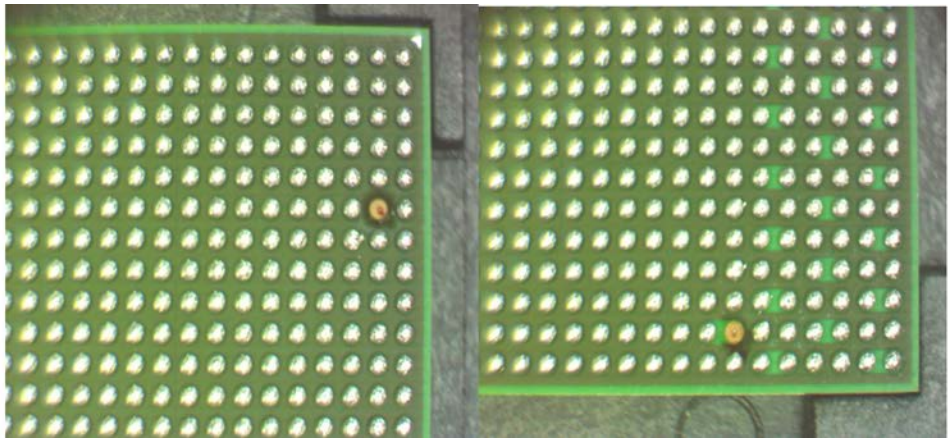
- What does an “acceptable” (per 38535/883) burn-in look like?
  - What is acceptable percentage of flip-flops, LUTs, BRAM, etc?
  - Does Processing System (ARM cores) have to be instantiated and dynamically exercised?

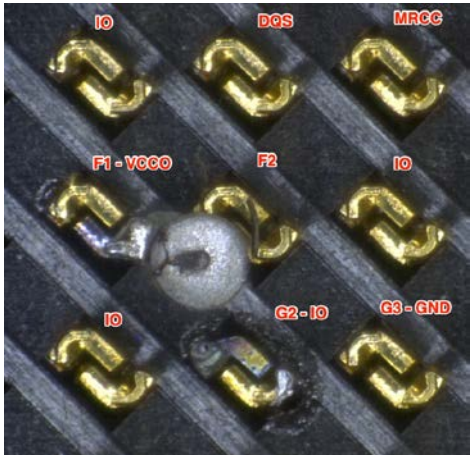
Additional guidance in 38535 and/or 883 for advanced SoC could be useful.

- How much of device needs to be tested pre/post burn-in?
  - Ideally everything used by the flight project
  - What if lot is to be used for multiple projects in the future? How do you ensure the lot is sufficiently screened for ANY project?
  - What if you only have 3-4 months for NRE?
  - Very difficult for end-sure and 3rd party test house to develop test comprehensive program for these devices.

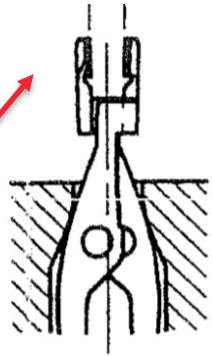
Involvement of part manufacturer is needed to develop comprehensive electrical tests for complex SoC. **Application-specific circuit recommended.**

Burn-in Socket Issue – Dislocated BGA Ball

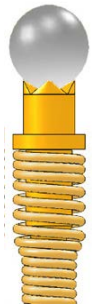




Clamp-Style (Burn-In)



Pogo-Pin (ATE)
Preferred



nt sponsorship
acknowledged.

Lot Qualification Tests – All Pass

Group B

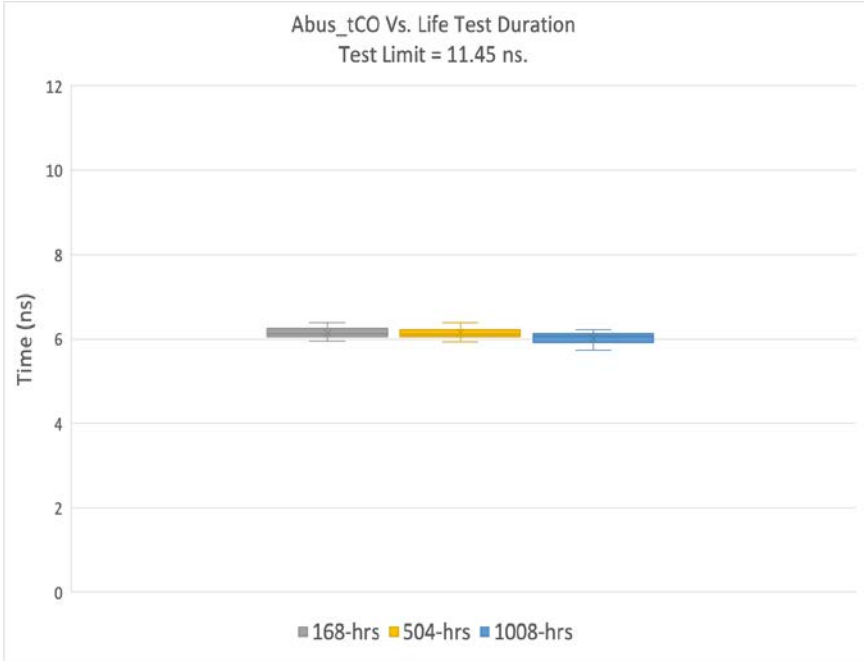
TESTS	MIL-STD-883 TEST METHOD	CONDITION
Resistance to Solvents	2015	
Die shear strength test on flip-chip and passive components, if applicable	2019 or 2027	
Solderability	2003	Soldering temperature 245C +/- 5C
For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package - TM 2038 (45 columns from 2 devices minimum)	JESD22-B117 (BGA) or 883 TM 2038 (CGA)	Ball Shear – JESD22-B117 Condition B

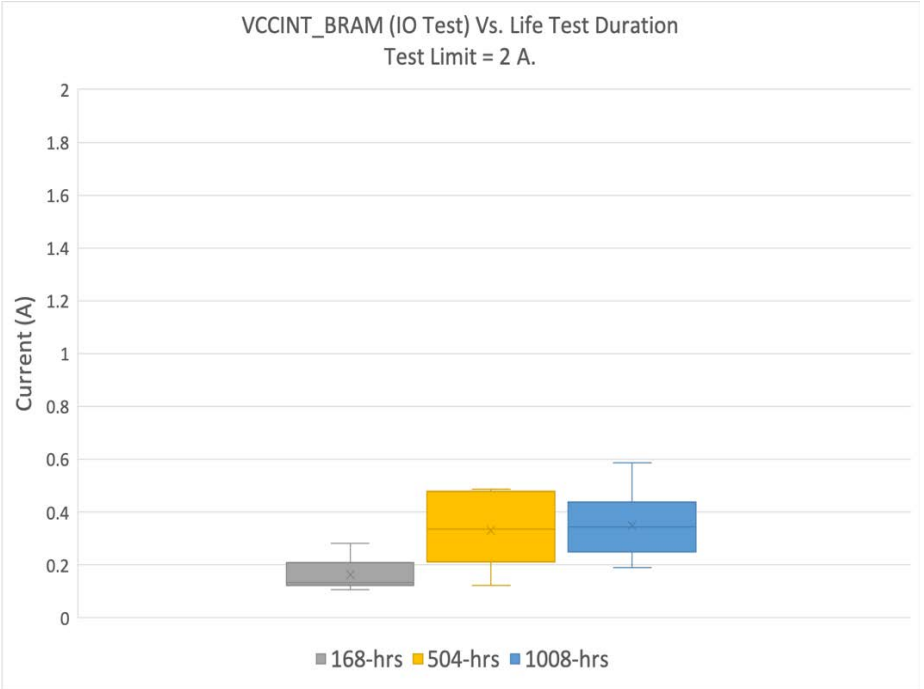
Group C

TESTS	MIL-STD-883 TEST METHOD	CONDITION
Operation Life Test End-point electricals	1005	A, C, or D. 1008 hrs at 125C or equivalent.

Group D

TESTS	MIL-STD-883 TEST METHOD	CONDITION
Physical Dimensions	2016	
a. Thermal Shock b. Temperature Cycling c. Moisture Resistance d. End-point electricals e. External Visual	1011 1010 HAST in accordance with JESD22-A118 2009	B, 15 cycles C, 100 cycles B
a. Mechanical Shock b. Vibration c. End-point electricals d. External Visual	2002 2007 2009	B A





Summary

Requirement	Result	Comments
DPA	✓✓✓	No anomalies.
Group B	✓✓✓	No anomalies. Ball share data within family of similar BGAs.
Screening – Electrical Test	✓	Not enough time for NRE. MicroBlaze test not fully debugged. Electrical test circuit limited compared to what EMIT will use (e.g. processing system not included in test)
Screening - Overall	✓✓	Despite inconsistent results with MicroBlaze test and limited coverage of the SoC features, the electrical test program did identify out of family parts thus allowing binning of the best parts for flight. MicroBlaze test ran fine during burn-in on all parts. No failures due to packaging (visual inspection, temp cycling, CSAM).
Group C	✓✓	10/10 passed with limited drift. Limited sample size due to part cost ($4k per part). 10pc tested instead of 22pc requirement.
Group D	✓✓	5/5 pass. Limited sample size due to part cost ($4k per part). 5pc tested instead of 15pc requirement.

Conclusion/Recommendations to Future Users of Commercial SoC

Additional Schedule and Application-Specific Circuits are Needed

- Complexity of advanced SoC and proprietary IP within its design is beyond end-user's ability to fully test. Traditional requirements such as ">90% fault coverage" for ASICs is not feasible. **Application-specific circuits** are needed for burn-in and electrical test to properly test and screen SoC.

- Budget at least >50% additional time to NRE phase compared to other microcircuit upscreening. Think in terms of months, not weeks. Even with application-specific circuit from flight project, **allow at least 6 months NRE** for developing electrical test program and burn-in hardware/software.

Jet Propulsion Laboratory
California Institute of Technology