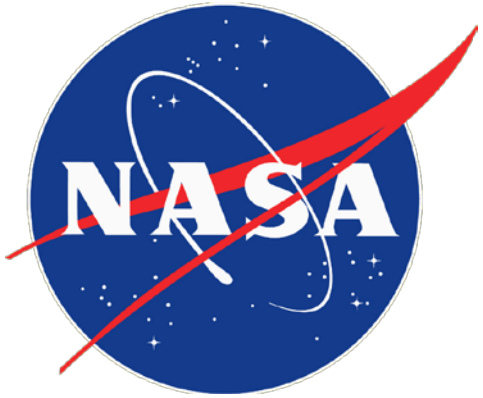

Architectural Models of Analog-to-Digital Converters for TID Radiation System Modeling

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Motivation for Architectural Modeling ADC Approach

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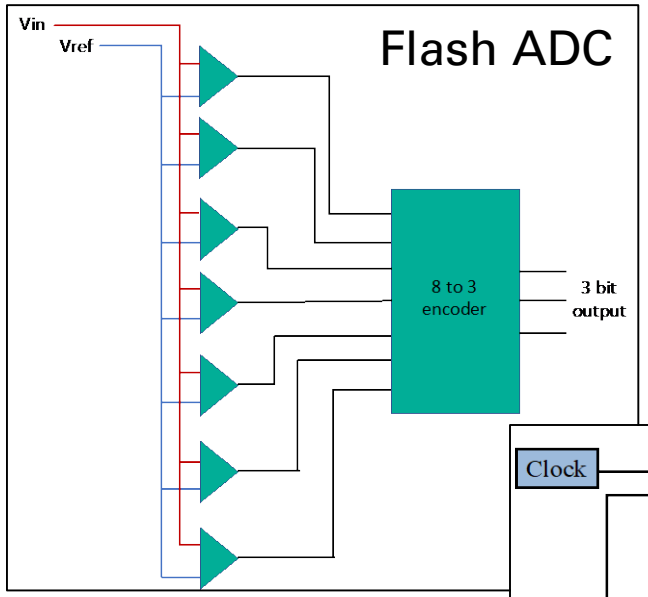
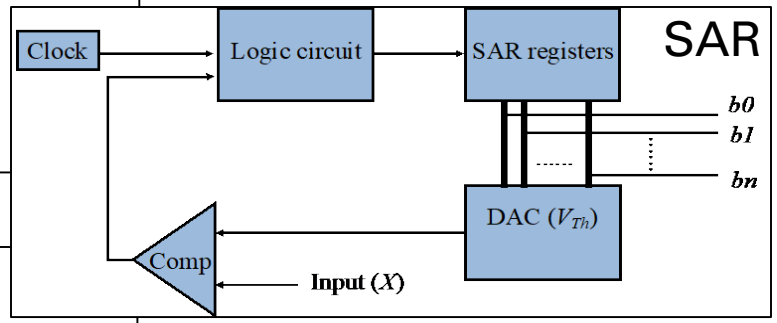
- Analog-to-Digital Converters (ADCs) are essential part of space systems
- Wide range of performance in terms of resolution, frequency, voltage range, and peripheral circuits
- Need flexible modeling method that covers many commercial ADCs
- Behavioral level, not transistor level, for system (board-level) simulation of TID impact
- Develop “architectural” approach for ADC simulation
- Need to explore validation methodologies for models of commercial ADCs
- Incorporate enhanced portability by calibration for same class of parts
- Build repository of re-usable, parameterized sub-blocks of ADC
- Develop a wide range of radiation-enabled models for specific part-number ADCs of interest to JPL

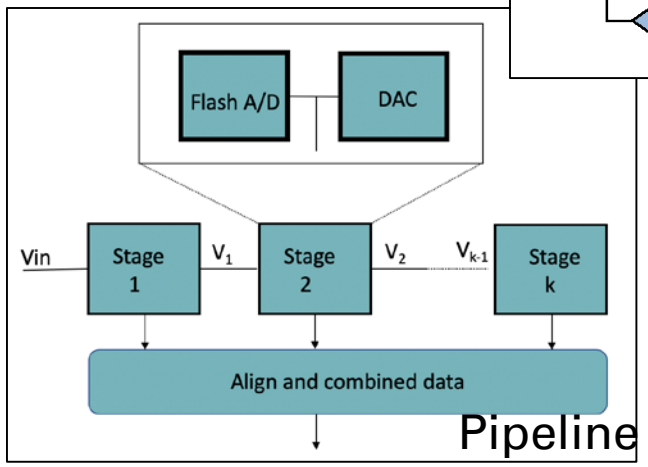
Common ADC Architectures



- Reference is fed to all comparators
- Multiple floating comparators
- Output of comparators are encoded



- Input is fed to he comparator
- Output pre-set/re-set based on the ref.
- Successive comparison brings accuracy



- Data is transferred in a pipeline fashion
- Individual stages perform concurrently
- Latency delay equal to the number of stages

Performance Overview of Common ADC Architectures

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ADC architectures are modeled based on accuracy, speed and power consumption, always a tradeoff

Architecture	Latency	Speed	Accuracy	Area
Flash	No	High	Low	High
SAR	No	Low-Medium	Medium-High	Low
Pipeline	Yes	Medium-High	Medium-High	Medium

Features of Architectural Modeling Paradigm

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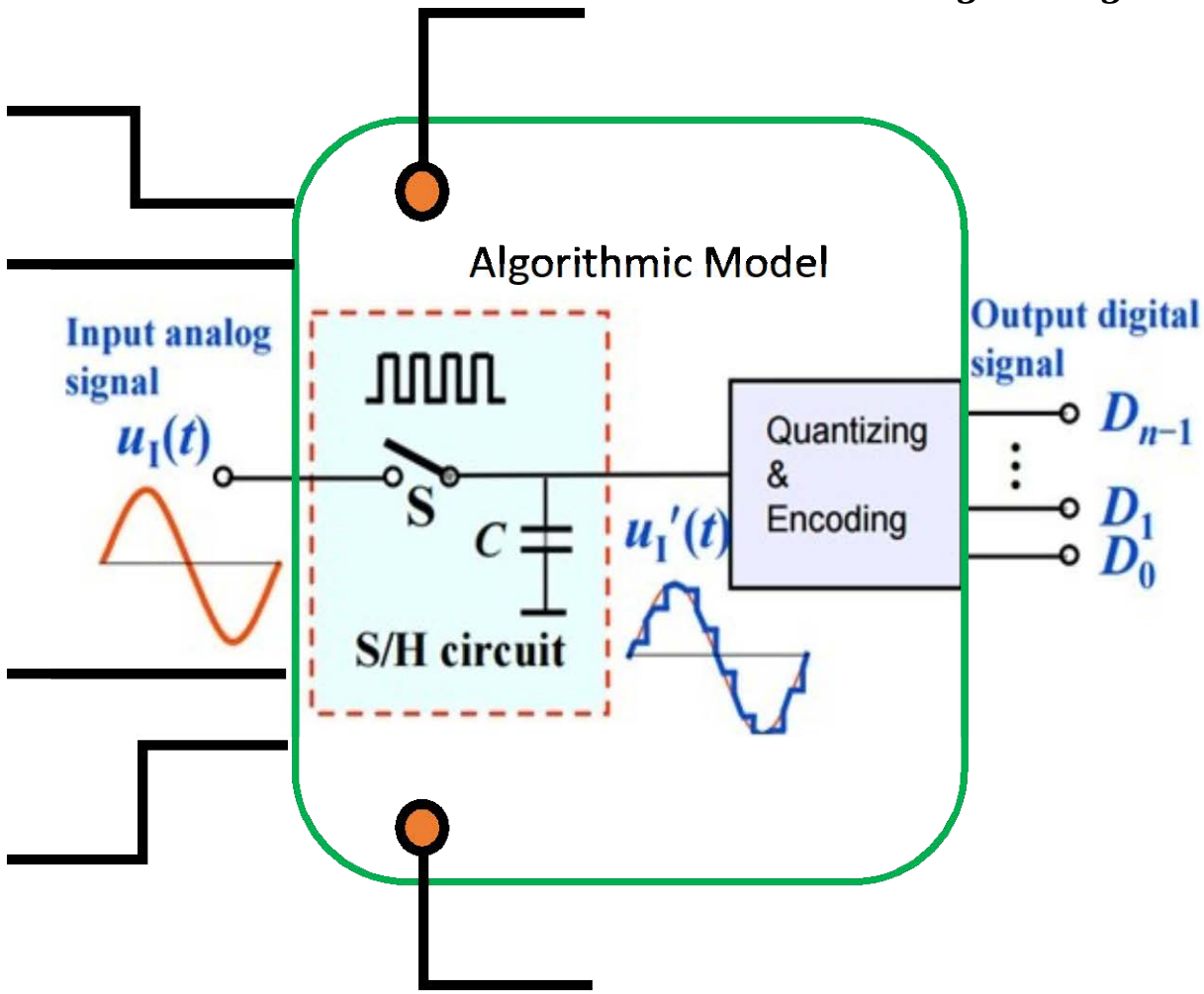
- System-level mixed signal simulation of component degradation due to radiation
- Flexible to model large number of commercial ADCs easily
- Scalability allows to calibrate with minimal effort
- Compatible with statistical and functional error sources
- Can be chosen for unipolar or bipolar (dual supply) conversion with a sign bit
- Verilog-AMS models enable designers to reflect analog and digital behavior
- Compatible with advanced Questa-ADMS simulation platform

ADC Architectural Model

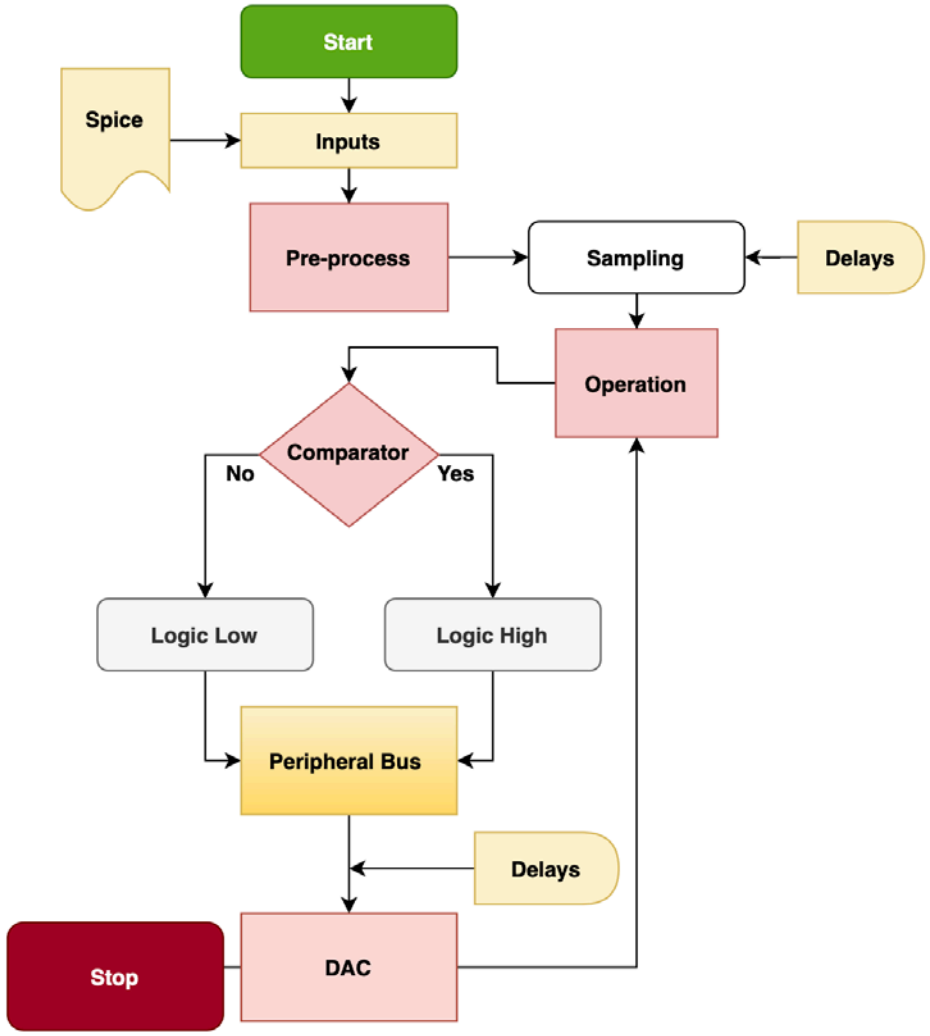
- Implements architecture based algorithm with degradation added
- Takes user input and calls Spice setups
- Evaluates static performance
- Evaluates dynamic performance
- Circuit functions performed using Verilog re-usable code structures



Symbolic diagram of ADC architectural models

Typical Flow Chart of an Architectural Model

- Includes major circuit components sensitive to radiation
- Combinational and switching delays adds improved accuracy
- SPI and Parallel peripheral interfaces



Flow chart of an ADC model

Recipe for architectural modeling of a commercial ADC

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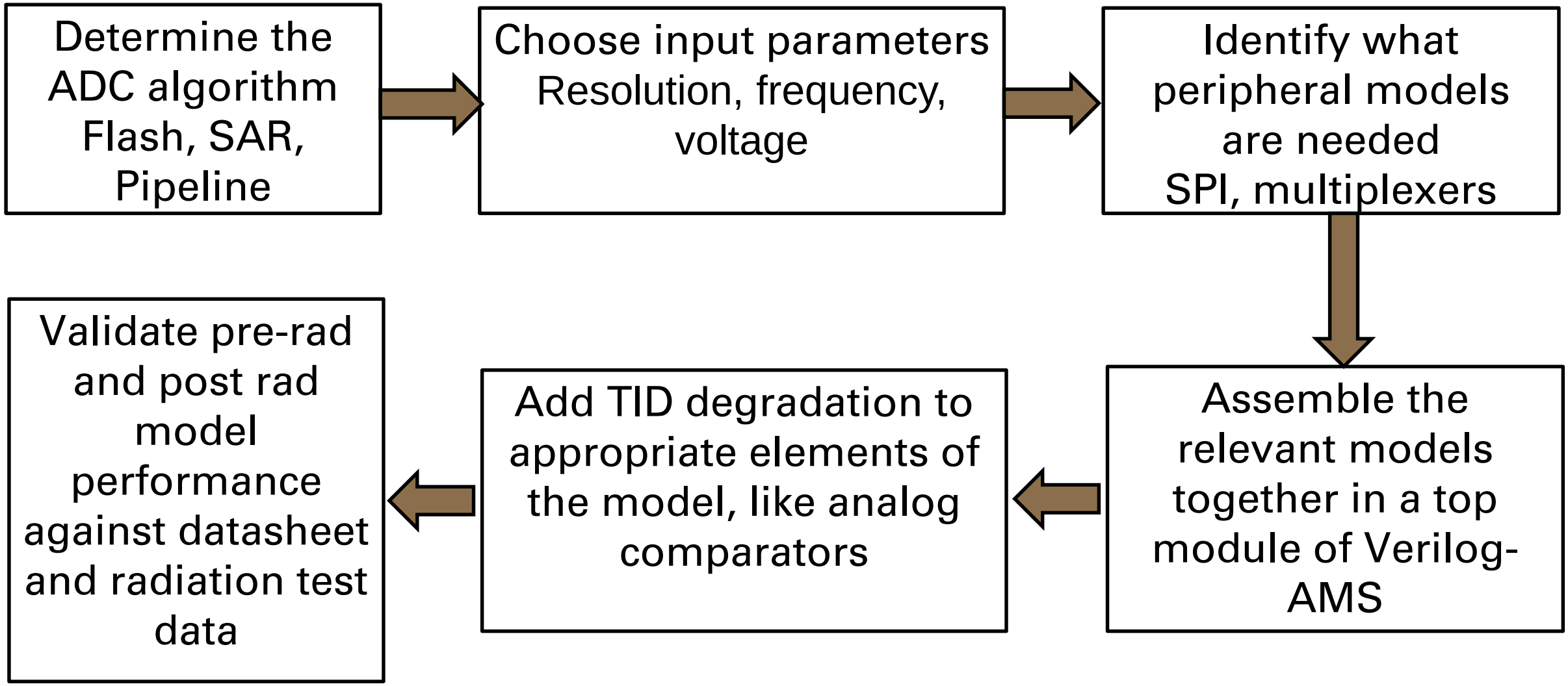
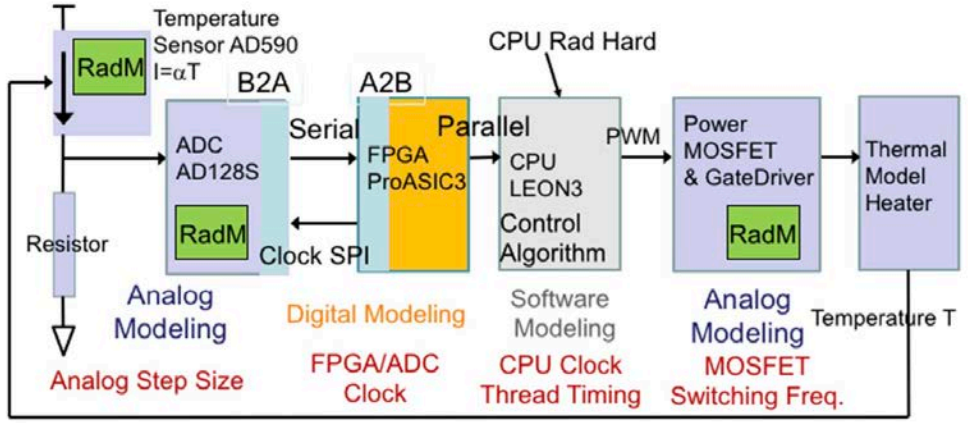
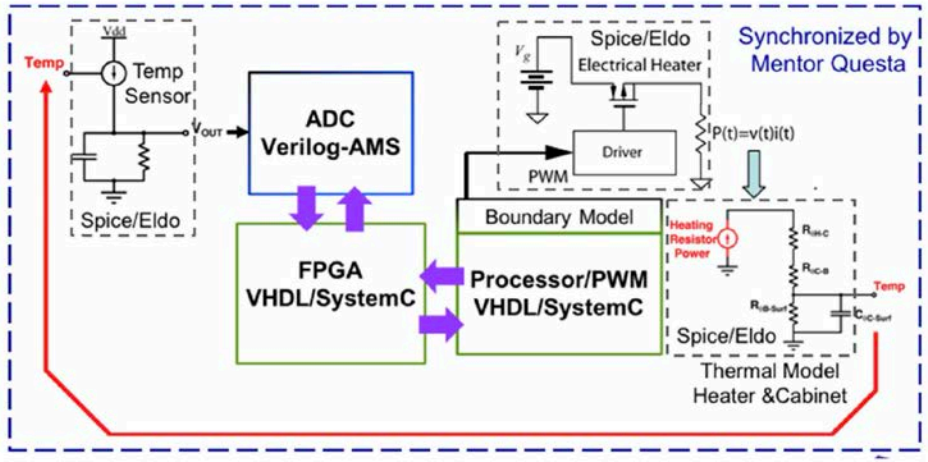


Mentor Questa-ADMS as a Simulation Platform

- Performs system level simulation by Integrating many kind of models in a single time domain
- Compatible to VHDL-AMS, Verilog-AMS, VHDL, Verilog, SystemVerilog, SPICE and SystemC
- Includes the versatile waveform viewer and calculation tool for display and analysis

Temperature regulation function of the Sphinx C&DH board





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Generic ADC Model vs Commercial ADC

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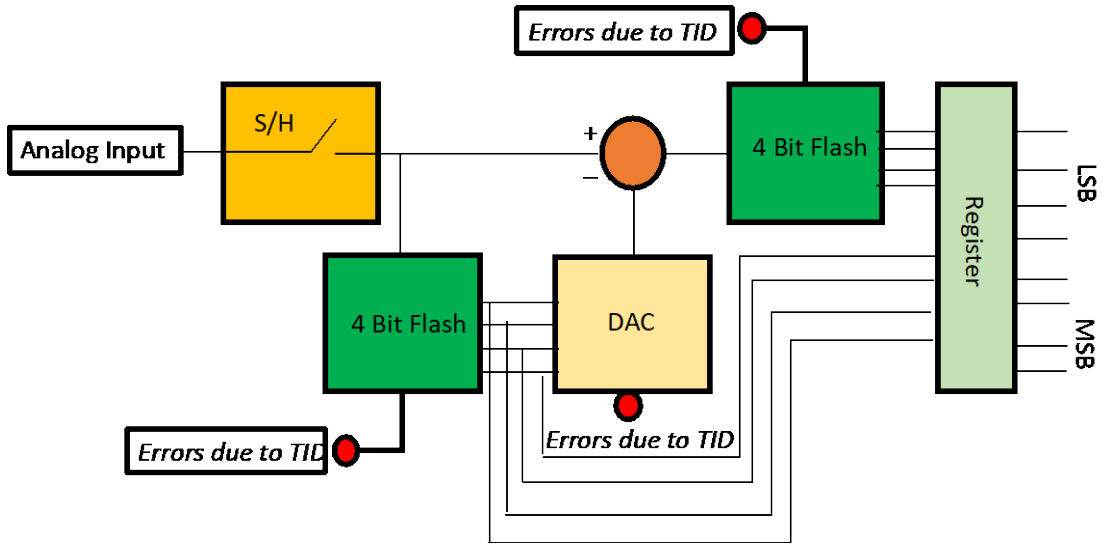
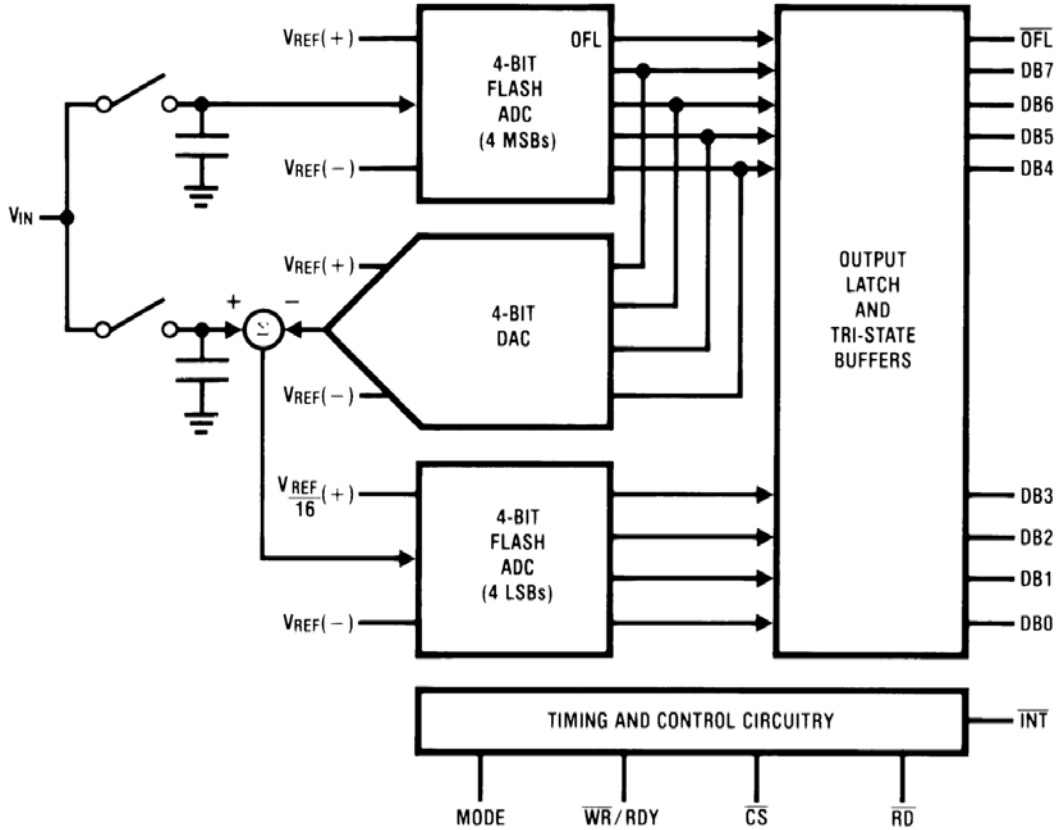
Generic models are used with other sub-blocks to characterize a fully functional commercial part

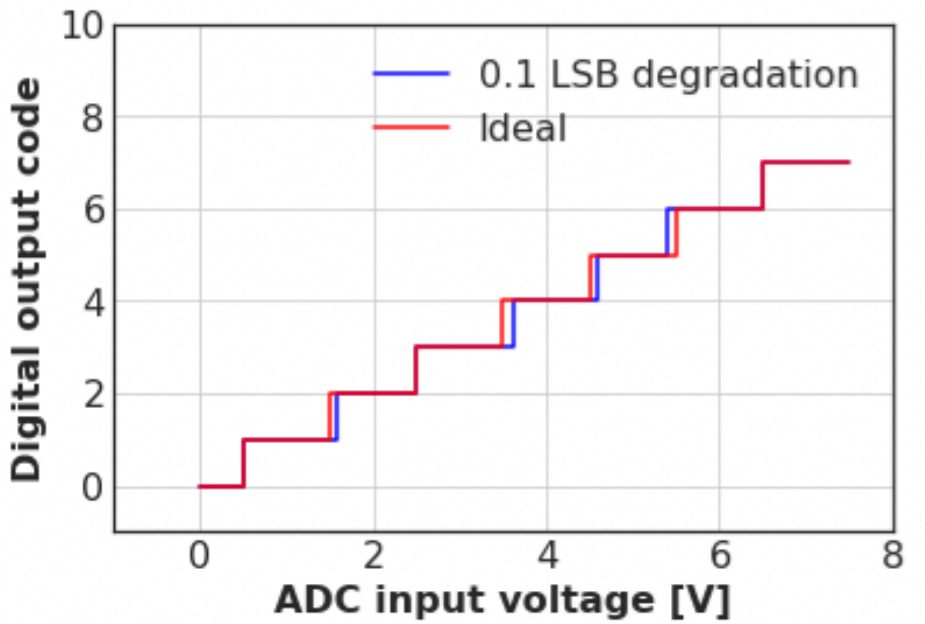


8-bit Flash ADC model

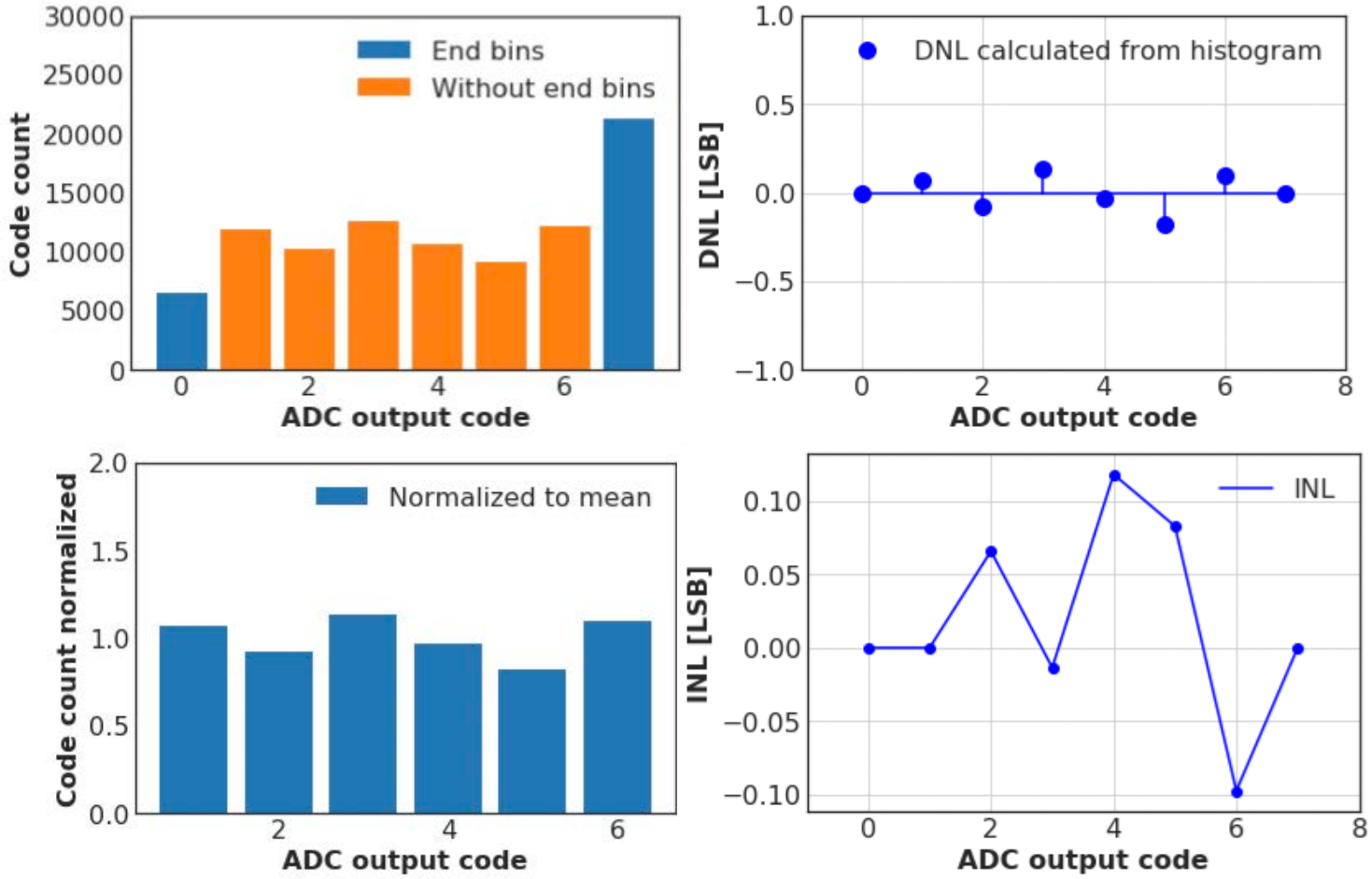


ADC0820-N from TI

Representative Results of a 3 Bit Flash ADC



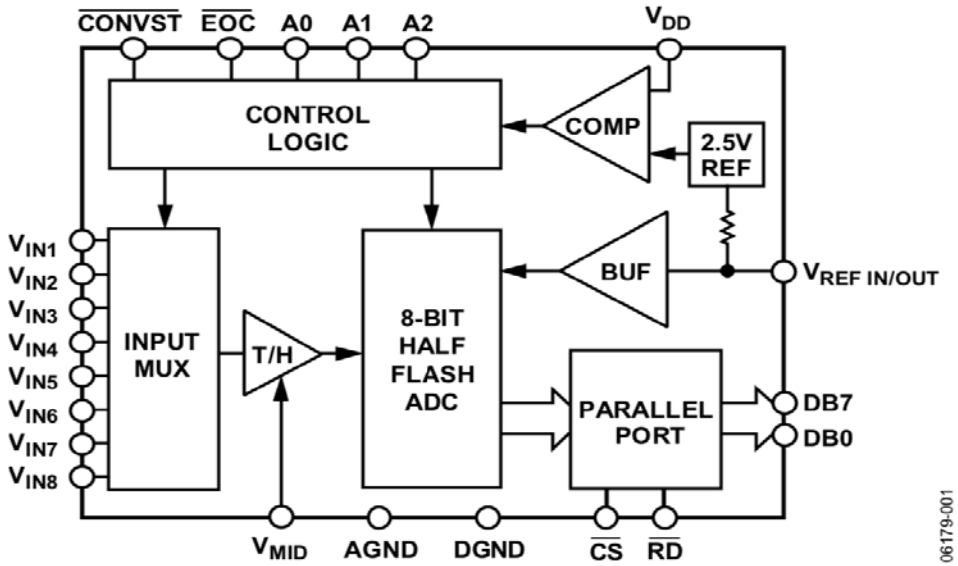
Transfer characteristics of a 3 bit flash ADC with degradation added



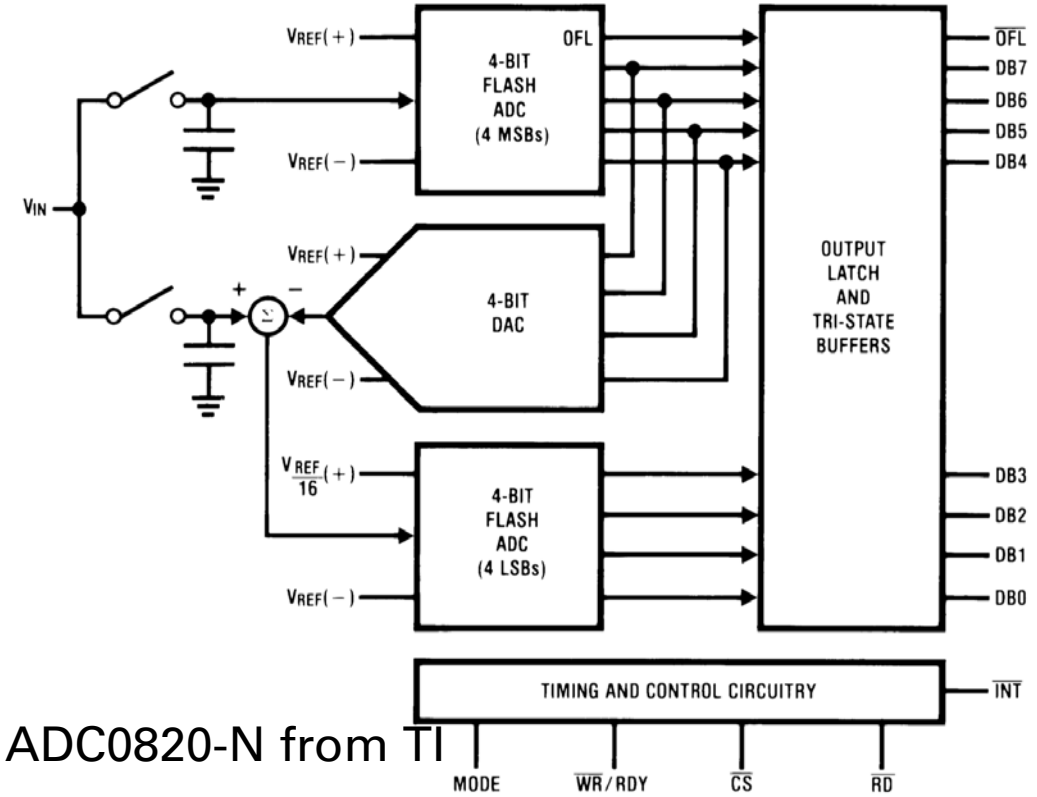
Histogram method of extracting DNL & INL

Peripherals and Auxiliary Sub-blocks in ADC

- Commercial ADCs have peripheral interfaces and auxiliary sub-blocks
- Variations come from manufacturer and architecture
- A parameterized sub-block repository is created by considering variations



AD7829 from analog devices



ADC0820-N from TI

Calibration and Validation of Architectural Models

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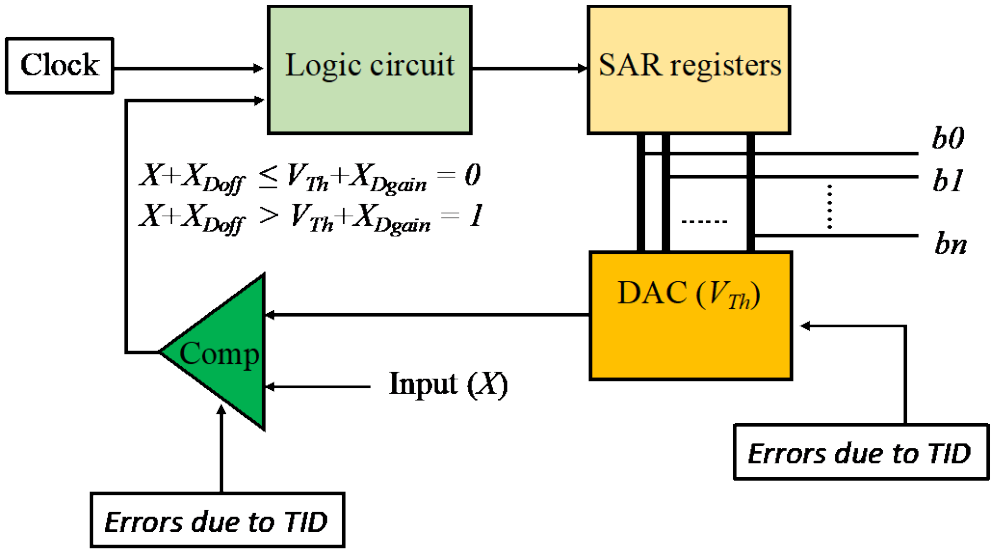
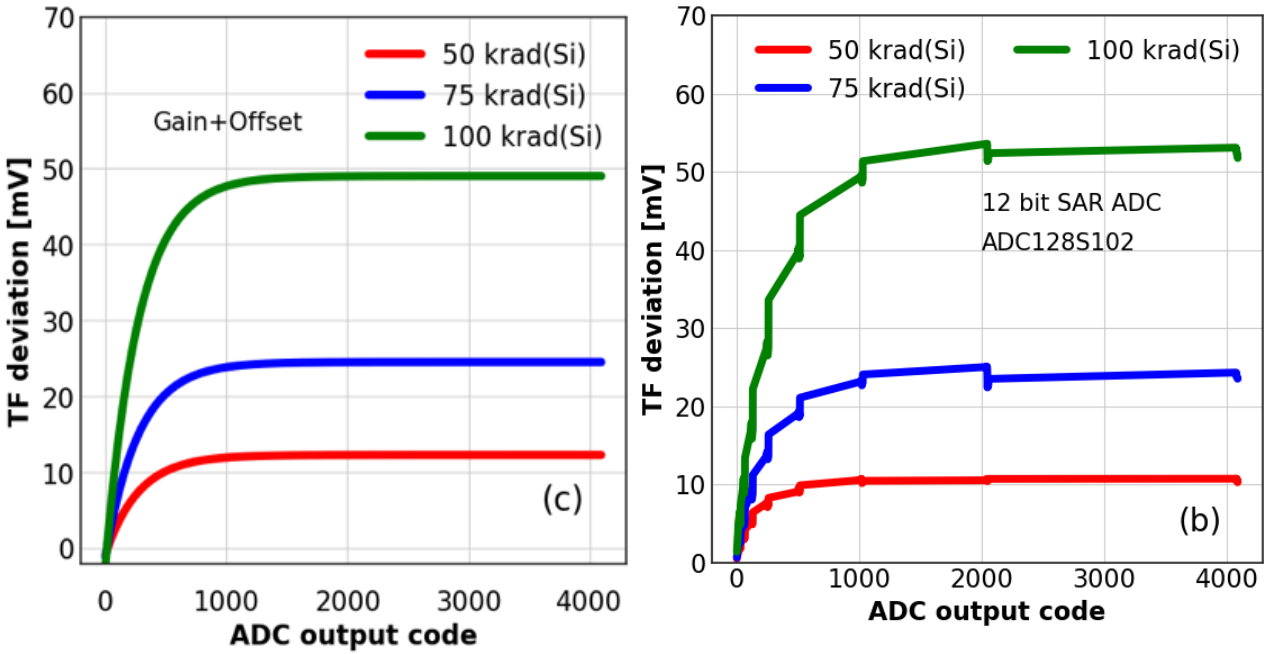
- JPL test results are used to calibrate SAR model (Accepted NSREC-2020 Abstract)
- Finding critical components and parameters sensitive to radiation degradation

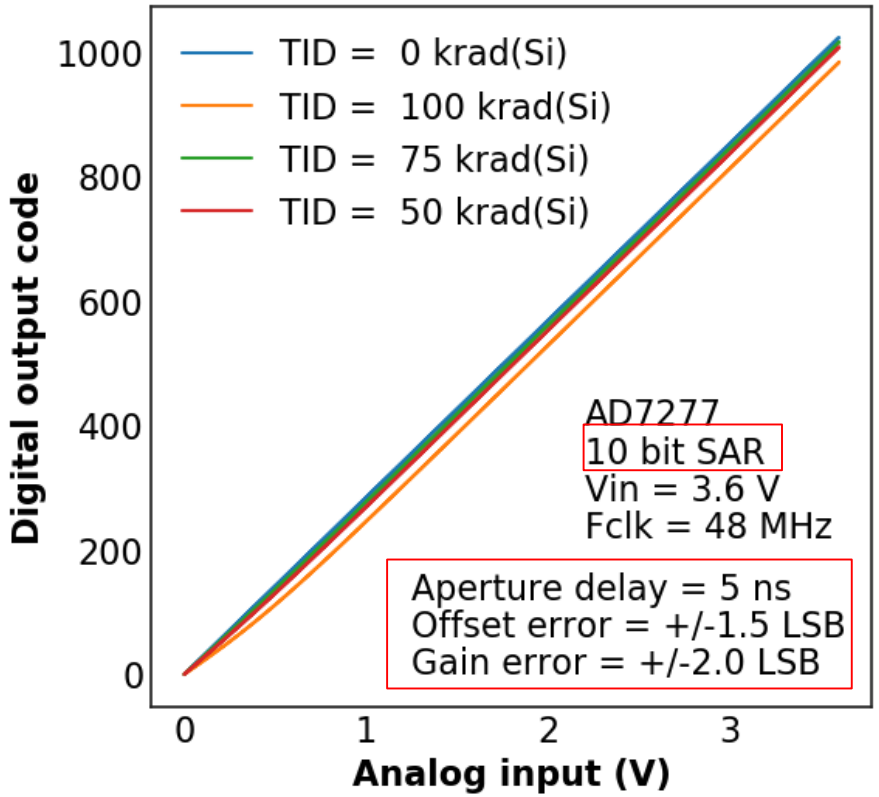


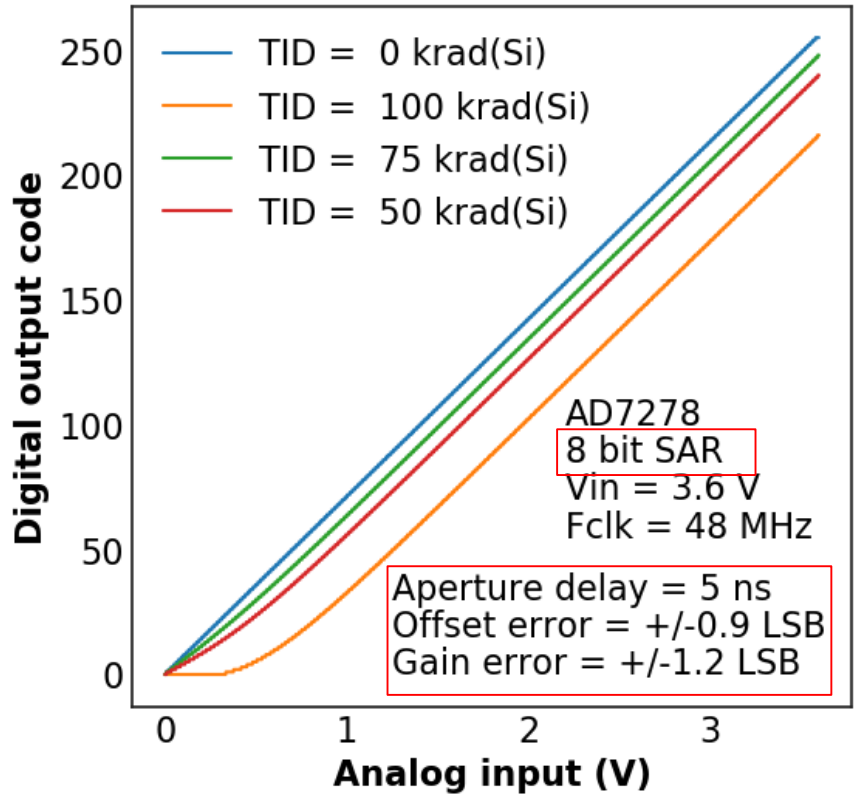
SAR ADC



Experimental and calibrated transfer function (TF) deviation for ADC128S102

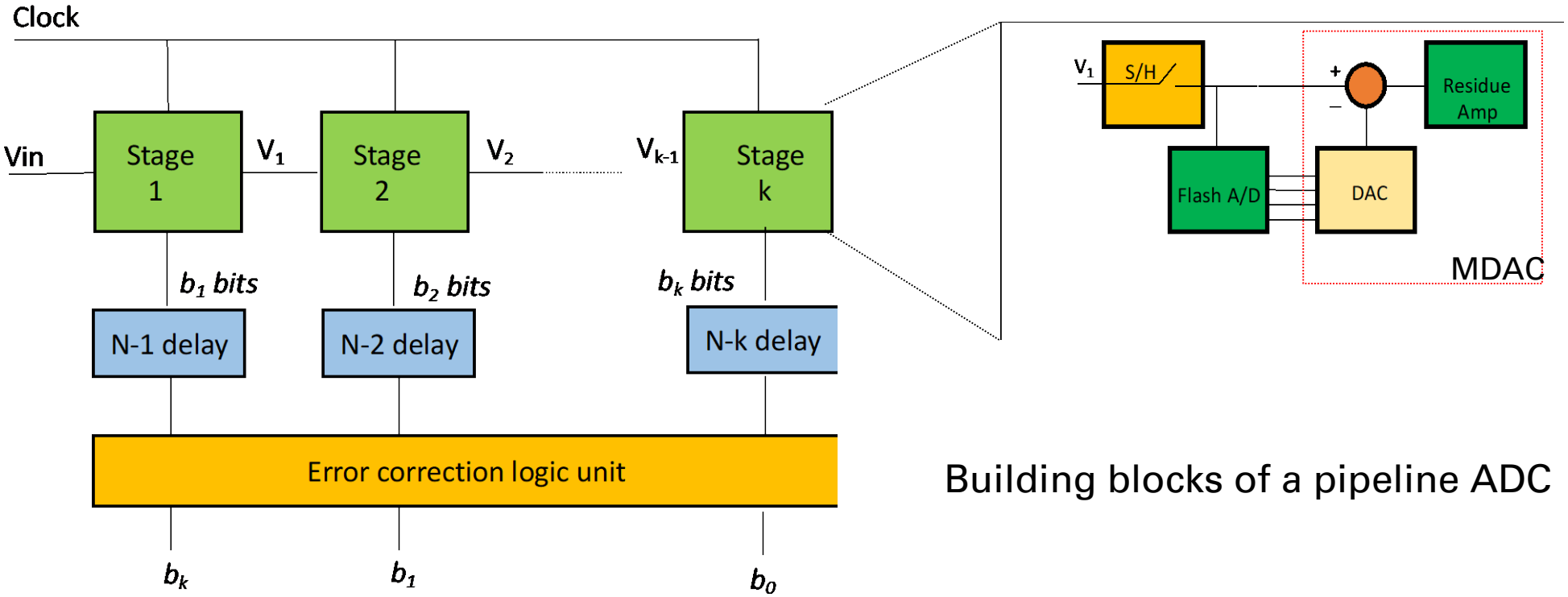
Portability of Architectural Models





Calibrated SAR ADC model is used to characterize TID degradation in various commercial SAR ADCs

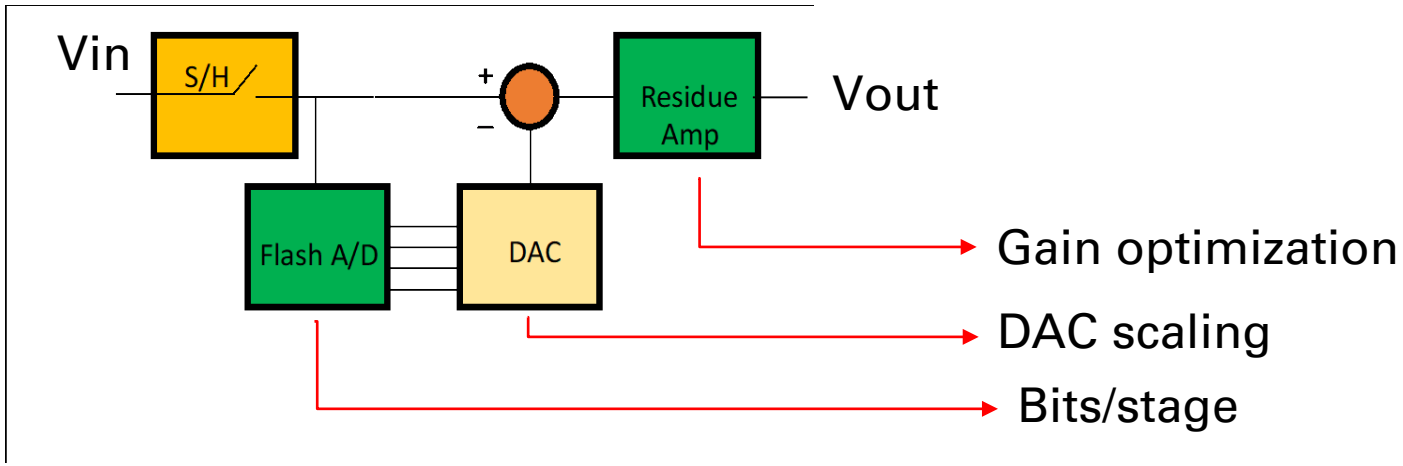
Re-usable Core Blocks to Increase Resolution



Building blocks of a pipeline ADC

- 1.5/2.5 bit stage Pipeline ADC
- Individual stages have degree of freedom in terms of input, output and gain
- Latencies and error correction logic unit consistent with input and output bits

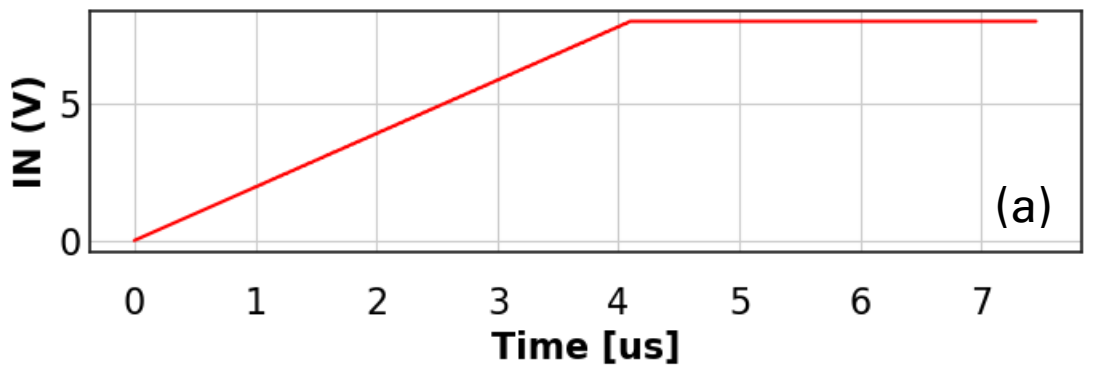
Stage Implementation

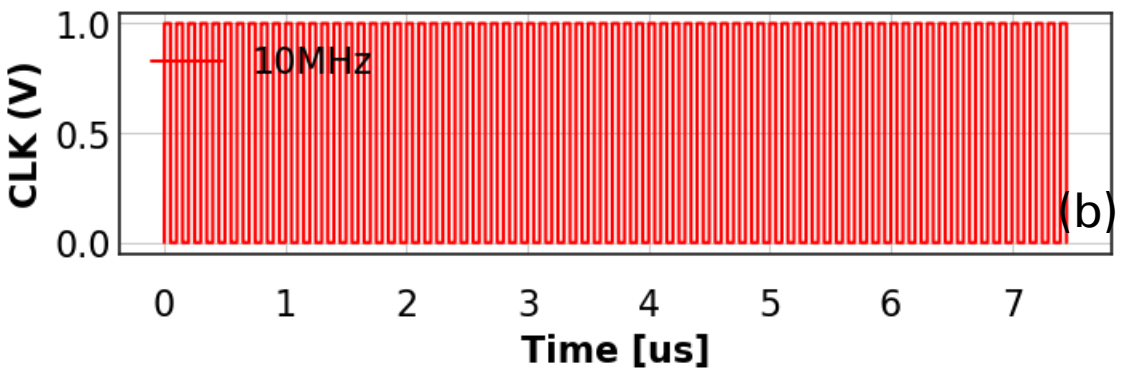


Elements in a stage of pipeline ADC

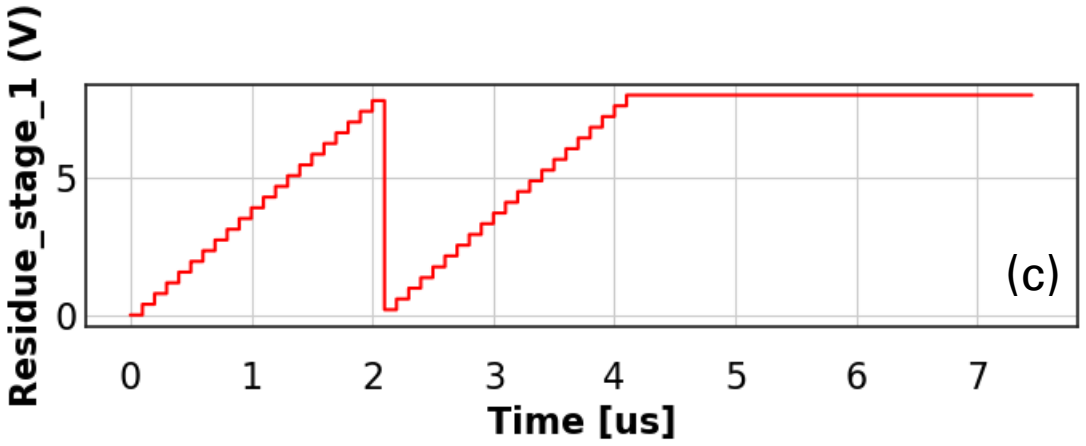
- Sample & Hold (S/H) implicitly available in stage building blocks,
- Input range can be selected based on requirement
- Calibrated building blocks allows user to choose any number of output bits per
- Residue amplifier gain is optimized automatically for user defined resolution

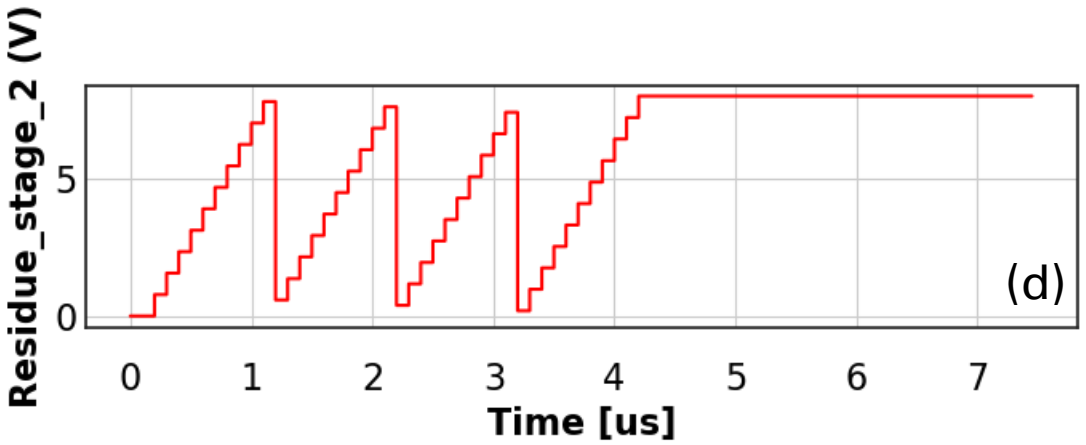
Results for a 3 Bit Pipeline ADC (1.5 Bit Stages)





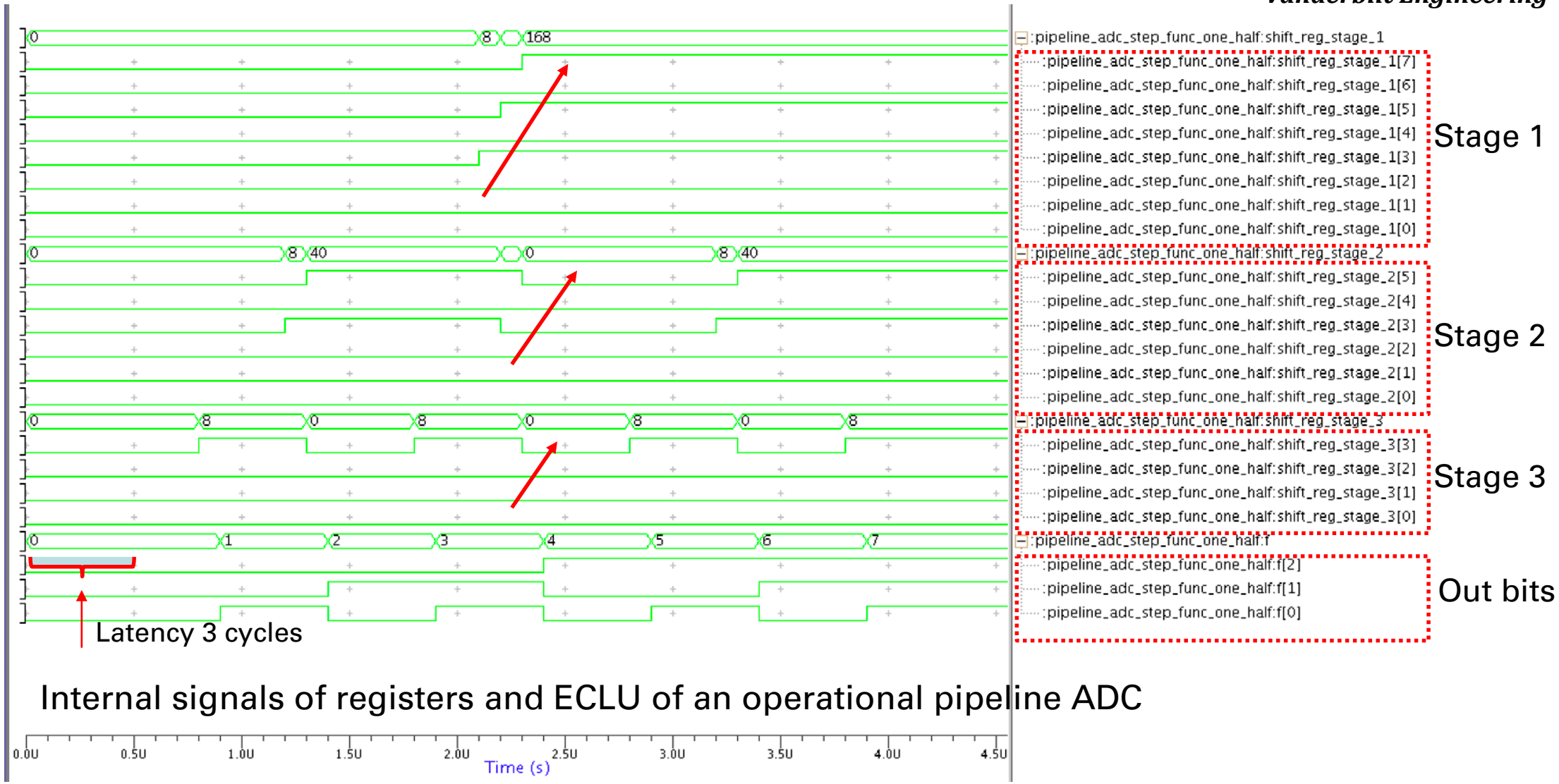
Analog input and sampling clock in a 3 bit pipeline ADC





Residual input voltage at different stages

Shift Registers and Error Correction Logic Unit (ECLU)



Internal signals of registers and ECLU of an operational pipeline ADC

Conclusions

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- Hundreds of ADCs with only 4-5 algorithms, architectural models are re-usable and scalable for wide variety of commercial parts
- Can be calibrated pre- and post-rad for commonly known ADC figure of merits such as signal to noise, THD, etc.
- Ionizing-dose-aware models can degrade the ADC for any measurable range of TID
  - Degradation can be expressed as distributions of parameters
  - Can be used in Monte-Carlo system simulations
- Architectural models run quickly in electrical or degraded post-rad system (board-level) simulations