MILSPEC Training

Basic Review of:

MIL-PRF-19500 - Semiconductor Devices

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing

MIL-PRF-38534 - Hybrid Microcircuits

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Acronyms

Abbreviation	Definition
AF	Air Force
BGA	Ball Grid Array
BN	Bayesian Network
BoK	Body of Knowledge
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off the Shelf
CPU	Central Processing Unit
DDR	Double Data Rate
DLA	Defense Logistics Agency
DMEA	Defense Microelectronics Activity
DoD	Department of Defense
DoE	Department of Energy
EEE	Electrical, Electronic, and Electromechanical
ETW	Electronics Technology Workshop
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
GIDEP	Government Industry Data Exchange Program
GPU	Graphics Processing Unit
GRC	Glenn Research Center
GSFC	Goddard Space Flight Center
GSN	Goal Structuring Notation
HQ	Headquarters
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
JPL	Jet Propulsion Laboratory
JSC	Johnson Space Center
LaRC	Langley Research Center
LGA	Land Grid Array
MAPLD	Military and Aerospace Programmable Logic Devices (Workshop)
MBMA	Model-Based Mission Assurance
MRAM	Magnetic Random Access Memory
MSFC	Marshall Space Flight Center

Abbreviation	Definition
NASA	National Aeronautics and Space Administration
NEPAG	NASA Electronic Parts Assurance Group
NEPP	NASA Electronic Parts and Packaging (Program)
NESC	NASA Engineering and Safety Center
NODIS	NASA Online Directives Information System
NPR	NASA Procedural Requirement
NRO	National Reconnaissance Office
NSREC	Nuclear and Space Radiation Effects Conference
OCE	Office of the Chief Engineer
OGA	Other Government Agency
PIC	Photonic Integrated Circuit
POC	Point of Contact
PoF	Physics of Failure
RF	Radio Frequency
RH	Radiation Hardened
RHA	Radiation Hardness Assurance
SAPP	Space Asset Protection Program
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single-Event Effects
SiC	Silicon Carbide
SMA	Safety and Mission Assurance
SMC	Space and Missile Systems Center
SOA	Safe Operating Area
SoC	System on a Chip
SRAM	Static Random Access Memory
SSAI	Science Systems and Applications, Inc.
STMD	Space Technology Mission Directorate
STT	Spin Transfer Torque
SysML	System Modeling Language
TID	Total Ionizing Dose
TSV	Thru-Silicon Via

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MIL-PRF-19500

Semiconductor Devices, General Specification for (w/Amendment 4)

FSC: 5961, Revision: P, Dated: 18 May 2018

MIL-PRF-38534

Hybrid Microcircuits, General Specification for

FSC: 5962, Revision: L, Dated: 03 December 2019

MIL-PRF-38535

Integrated Circuits (Microcircuits) Manufacturing, General Specification for

FSC: 5962, Revision: L, Dated: 06 December 2018

General / Common Points

A Performance Spec

19500….The main body specifies the **performance requirements** and requires the manufacturer to verify that their devices are capable of meeting those performance requirements.

38534…..This document is a **performance specification**. It is intended to provide the device manufacturers an acceptable established **baseline…** These appendices **provide guidance** to manufacturers on demonstrated **successful approaches to meeting defense performance requirements**.

38535…allow the device manufacturer the **flexibility to implement best commercial practices** to the maximum extent possible while still providing product that **meets military performance needs**.

General / Common Points

- DLA certified manufacturers have to comply with the following requirements:
  - Has to sign up to be part of the military components standardization program in order to manufacture products to the required quality levels.
  - Successfully audited and certified by Defense Logistics Agency (DLA) Land & Maritime for their manufacturing facility. Multiple audits may be required if more than 1 facility is involved.
  - Successfully pass periodic DLA re-audits to remain in the MIL-PRF-19500 standardization program.

General / Common Points

- Document control encompasses various areas:
  - Design control requires that DLA (and user community) have to review and approve any proposed military specification sheet product design changes.
  - Procedures for each manufacturing and testing process step
- Traceability of a specific production lot back to the original wafer lot and other internal elements.
- Participate in the GIDEP alert system
- Changes IAW specification requirements
- Failures reported to DLA

RHA Designator & Levels

RHA level designator	Radiation total ionizing dose level (krad(Si))
- (dash)	No RHA
M	3
D	10
P	30
L	50
R	100
F	300
G	500
H	1000

19500 – Table E-II 38534 – Table G-I 38535 - Section 3.4.3

MIL-PRF-19500 - Semiconductor Devices

MIL-PRF-19500
Semiconductor Devices, General Specification for (w/Amendment 4)
FSC: 5961, Revision: P, Dated: 18 May 2018

JANS – Joint Army Navy Space parts are the highest quality level parts manufactured and supplied to military and space programs.
JANTXV – highest military quality level with additional screening
JANTX – standard military quality level with standard screening.
JAN – lowest quality level with minimal screening to verify parts are functional. Cost is slightly more expensive than commercial grade parts; however, JAN parts have a pedigree and reliability built in.

Military and space grade parts are identified with the JAN, JANTX, JANTXV, and JANS in the part number, e.g. JAN2N2222AUB, JANTX2N2222AUB, JANTXV2N2222AUB, and JANS2N2222AUB.

19500 - Screening tests comparison

Screen	JANS	JANTXV	JANTX	JAN
Precap visual	Yes	Yes	No	No
Stabilization bake	Optional	Optional	Optional	Optional
Temperature Cycle	Yes	Yes	Yes	N/A
Surge	Yes	Yes	Yes	As specified
Thermal impedance	Yes	Yes	Yes	As specified
Electrical test	Yes	Yes	Yes	Yes
HTRB	Yes	Yes	Yes	N/A

19500 - Screening tests comparison

Screen/Quality Level	JANS	JANTXV	JANTX	JAN
Interim electricals	Yes	Yes	Yes	N/A
Burn-in	Yes	Yes	Yes	N/A
Final electrical	Yes	Yes	Yes	N/A
Radiography	N/A	N/A	As specified	N/A
External Visual	100 percent	N/A	N/A	N/A

Qualification inspection comparison Group A

Group/Quality Level	JANS	JANTXV	JANTX	JAN
Subgroup 1, Visual & mechanical	15 devices	116 devices	45 devices	45 devices
Subgroup 2, DC electricals @ 25C	116 devices	116 devices	116 devices	116 devices
Subgroup 3, DC (static) tests at high (-0C, +10C) and low (+0C, -10C) specified temperatures.	116 devices	116 devices	116 devices	116 devices
Subgroup 4, Dynamic tests at +25°C ±3 degrees C	116 devices	116 devices	116 devices	116 devices
Subgroup 5, Safe operating area test (for transistors only): a. DC b. Clamped inductive (only when applicable) c. Unclamped inductive (only when applicable) End-point electrical measurements	45 devices	45 devices	45 devices	45 devices

Qualification inspection comparison B

Group/Quality Level		JANS	JANTXV	JANTX	JAN
Subgroup 1,	Physical Dimensions	22 devices	N/A	N/A	N/A
Subgroup 2 (Subgroup 1 for non JANS)	Solderability	15 devices	15 devices	15 devices	15 devices
	Resistance to Solvents	15 devices		15 devices	15 devices
	Salt Atmosphere	6 devices		6 devices	6 devices
Subgroup 3 (Subgroup 2 for non JANS)	Thermal shock	22 devices	22 devices	22 devices	22 devices
	Temperature Cycling				
	Surge				
	Hermeticity				
	End point Electricals				
	Decap internal visual	6 devices	1 device	1 device	1 device
	Bond Strength	22 wires	11 wires	11 wires	11 wires
	SEM	6 devices	N/A	N/A	N/A
	Die Shear	11 devices	N/A	N/A	N/A
Subgroup 4 (Subgroup 3 for non JANS)	Intermittent operational life	22 devices	22 devices	22 devices	22 devices
	Hermetic seal				
	Electrical measurements				
	Bond Strength	11 wires	11 wires	11 wires	11 wires
Subgroup 5 (Subgroups 3 and 4 for non JANS)	Accelerated steady state operation life	22 devices	N/A	N/A	N/A
	Steady state operation life/ IOL	N/A	45 devices	45 devices	45 devices
	Electrical measurements	Yes	Yes	Yes	Yes
	Bond Strength	20 wires	11 wires	11 wires	11 wires
	Decap internal visual	N/A	1 device	1 device	1 device
Subgroup 6 (Subgroup 5 for non JANS)	Thermal resistance	22 devices	15 devices	15 devices	15 devices
Subgroup 7 (Subgroup 6 for non JANS)	High Temperature life (non-operating)	32 devices	32 devices	32 devices	32 devices
	Electrical Measurements	Yes	Yes	Yes	Yes

Qualification inspection comparison C

Group/Quality Level	All quality levels (JANS, JANTXV,JANTX,JAN)
Subgroup 1, Physical dimensions	15 devices
Subgroup 2, thermal shock, temperature cycling, terminal strength, surface mount endcap bond integrity, hermeticity, moisture resistance, electrical measurements	22 devices
Subgroup 3 – Shock, variable vibration, constant acceleration, electrical measurements	22 devices
Subgroup 4 – salt atmosphere	15 devices
Subgroup 5, thermal resistance	15 devices
Subgroup 6, life test – steady state or intermittent, hermeticity, electrical measurements, bond strength	22 devices/11 wires for bond strength
Subgroup 7 – internal gas analysis	3 devices for structurally identical package family

Qualification inspection comparison D

Group/Quality Level	JANS	JANTXV	JANTX	JAN
Subgroup 1, Neutron radiation, electrical measurements	11 devices	11 devices	N/A	N/A
Subgroup 2, total ionizing radiation, electrical measurements	4 devices	11 devices	N/A	N/A
Subgroup 3, power transistor electrical dose rate electrical measurements	11 devices	11 devices	N/A	N/A

Qualification Inspection Comparison E

Group/Quality Level	All quality levels (JANS, JANTXV,JANTX,JAN)
Subgroup 1, temperature cycling, hermeticity, electrical testing	45 devices
Subgroup 2, life testing (IOL, steady state), electrical testing	45 devices
Subgroup 3 – Not applicable	N/A
Subgroup 4 – Thermal impedance	Yes, sample size based on histogram of qualification lot.
Subgroup 5 – Reduced Barometric testing	3 devices for devices rated > 200V
Subgroup 6, ESD	11 devices
Subgroup 7, Resistance to soldering heat, visual inspection,	3 devices
Subgroup 8 – Reverse Stability (bipolar transistors only)	45 devices
Subgroup 9 – Resistance to glass cracking	45 devices

MIL-PRF-38534 - Hybrid Microcircuits

MIL-PRF-38534
Hybrid Microcircuits, General Specification for
FSC: 5962, Revision: L, Dated: 03 December 2019

1.3 Classification. Seven quality assurance levels are provided for in this specification. Four of these classes, in highest to lowest order, are K, H, G and D, as defined below. The fifth class is Class E, the quality level associated with a Class E device is defined by the acquisition document.

1.3.1 **Class K**. - the **highest reliability level** provided for in this specification. It is intended for **space** applications.
1.3.2 **Class H**. - the standard **military** quality level.
1.3.5 **Class E**. - designates devices which are based upon one of the other classes (L, K, H, G, or F) with **exceptions** taken to the requirements of that class.
1.3.6 **Class L**. - the highest quality class for **non-hermetic** devices.
1.3.7 **Class F**. - the standard quality class for **non-hermetic** devices.

Element Evaluation Summary

TABLE C-I. Element evaluation summary.

Element	Paragraph	Table or MIL-STD-883 method
Microcircuit dice	C.3.3	Table C-II
Semiconductor dice	C.3.3	Table C-II-1
Wire Bondable and Surface Mount Resistors.	C.3.4	Table C-III
Capacitors, Ceramic	C.3.4	Table C III-1
Chip Capacitors, Solid Tantalum	C.3.4	Table C III-2
Capacitors, MOS – NMOS	C.3.4	Table C III-3
Coils, Transformers	C.3.4	Table C III-4
Surface acoustic wave (SAW) elements	C.3.5	Table C-IV
Alternate evaluation	C.3.6	N/A
Substrate evaluation	C.3.7	Table C-V
Package evaluation	C.3.8	Table C-VI
Integral substrate/package evaluation	C.3.9	Table C-VII
Polymeric material evaluation	C.3.10	Method 5011
Sub-assembly evaluation	C.3.11	Table C-VII-1

Microcircuit Dice Evaluation Requirements

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TABLE C-II. Microcircuit dice evaluation requirements.

Subgroup	Class K	Class H	Test	Specification or Standard	Method	Condition	Comments	Quantity (accept number)	Reference paragraph MIL-PRF-38534
1	X	X	Element Electrical	Per Acquisition Document			25°C	100%	C.3.3.1
2		X	Element Visual	MIL-STD-883	2010	B		100%	C.3.3.2
	X		Element Visual	MIL-STD-883	2010	A			
3		X	Internal Visual	MIL-STD-883	2010	B		10(0)	C.3.3.3
	X		Internal Visual	MIL-STD-883	2010	A			C.3.3.4.2
4	X		Initial Electrical	Per Acquisition Document			25°C Record Data	10(0)	
	X		Temperature Cycle	MIL-STD-883	1010	C	20 Cycles		C.3.3.3
	X		Mechanical Stress 1/	MIL-STD-883 - Constant Acceleration	2001	A	Y1 Direction		
				MIL-STD-883 - Mechanical Shock	2002	B	Y1 Direction		
	X		Interim Electrical	Per Acquisition Document			25°C Record Data		C.3.3.4.3
	X		Burn-In 2/	MIL-STD-883	1015		240hrs Min. at Tc or Ta = 125ºC Min.		
	X		Post-BI Electrical 3/	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
	X		Steady State Life 2/	MIL-STD-883	1005		1000hrs at Tc or Ta =125°C Min. or 500hrs at Tc=150°C Min.		
	X	X	Final Electrical 3/	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
5	X	X	Wirebond Evaluation 4/	MIL-STD-883	2011		Bake for 1 hour minimum @ +300ºC (Bimetallic bonds only)	10(0) or 20(1) wires	C.3.3.3 C.3.3.5
6	X		SEM 5/	MIL-STD-883	2018			See 5/	C.3.3.6

Semiconductor Dice Evaluation Requirements

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TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

Subgroup	Class		Test	Transistor - Signal	Transistor - Power	Diode - Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
	K	H													
4	X		Interim Electrical 1/ 3/	X	X	X	X	X	X	Per Acquisition Document			25°C Record Data	10(0)	C.3.3.4.3
	X		Burn-In	X	X					MIL-STD-750	1039	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X							X		MIL-STD-750	1042	A	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X					X	X			MIL-STD-750	1038	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X								X	MIL-STD-750	1040	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X		Post BI Electrical 1/ 4/	X	X	X	X	X	X	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3

See footnotes at end of table.

Device Screening

TABLE C-IX. Device screening.

Test or inspection	MIL-STD-883		Requirement		Reference paragraph
	Method	Condition	Class K	Class H	
Preseal burn-in	1030		Optional	Optional	C.5.3
Non-destructive bond pull	2023		100 percent	Optional	C.5.4
Internal visual	2017		100 percent	100 percent	C.5.5
Temperature cycling	1010	C, 10 cycles	100 percent	100 percent	C.5.6
Mechanical shock or constant acceleration	2002 2001	B, (Y1 direction only) 3,000 g's, Y1 direction only	100 percent	100 percent	C.5.6
PIND	2020	Condition A shall be used for Class K, unless otherwise specified	100 percent	Optional	C.5.7
Pre-burn-in electrical test	In accordance with applicable device specification		100 percent	Optional	C.5.8
Burn-in	1015		100 percent	100 percent	C.5.9
Final electrical test	In accordance with applicable device specification		100 percent	100 percent	C.5.10
Seal (fine and gross)	1014		100 percent	100 percent	C.5.11
Radiographic	2012		100 percent	Optional	C.5.12
External visual screen	2009		100 percent	100 percent	C.5.13

Group A Electrical Test

TABLE C-IX. Device screening.

Test or inspection	MIL-STD-883		Requirement		Reference paragraph
	Method	Condition	Class K	Class H	
Preseal burn-in	1030		Optional	Optional	C.5.3
Non-destructive bond pull	2023		100 percent	Optional	C.5.4
Internal visual	2017		100 percent	100 percent	C.5.5
Temperature cycling	1010	C, 10 cycles	100 percent	100 percent	C.5.6
Mechanical shock or constant acceleration	2002 2001	B, (Y1 direction only) 3,000 g's, Y1 direction only	100 percent	100 percent	C.5.6
PIND	2020	Condition A shall be used for Class K, unless otherwise specified	100 percent	Optional	C.5.7
Pre-burn-in electrical test	In accordance with applicable device specification		100 percent	Optional	C.5.8
Burn-in	1015		100 percent	100 percent	C.5.9
Final electrical test	In accordance with applicable device specification		100 percent	100 percent	C.5.10
Seal (fine and gross)	1014		100 percent	100 percent	C.5.11
Radiographic	2012		100 percent	Optional	C.5.12
External visual screen	2009		100 percent	100 percent	C.5.13

Group B In-line Tests

TABLE C-Xb. Group B testing (option 2 only).

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	K	H		Method	Condition		
1	X	X	Physical dimension	2016		2(0)	
2			Not used				
3	X	X	Resistance to solvents	2015		3(0)	
4	X	X	Internal visual and mechanical	2014		1(0)	C.6.4.2.1
5	X	X	Bond strength: a. Thermocompression b. Ultrasonic or wedge c. Flip-chip d. Beam lead	2011	 C or D C or D F H	2(0)	C.6.4.2.2
6	X	X	Die shear strength	2019		2(0)	C.6.4.2.3
7	X	X	Solderability	2003	Solder temperature +245°C ± 5°C	1(0)	C.6.4.2.4
8		X	Seal: a. Fine b. Gross	1014	 A or B C or D	15(0)	C.6.4.2.5

Group C In-line Tests

APPENDIX C

TABLE C-Xc. Group C testing.

Subgroup	Class K	Class H	Test	MIL-STD-883 Method	MIL-STD-883 Conditions PI	MIL-STD-883 Conditions QML	Quantity (accept number)	Reference paragraph
1	X	X	Resistance to Soldering Heat	2036	1/	N/A	5 (0)	C.6.3.3.5
	X	X	External visual	2009				
	X	X	PIND 2/	2020	N/A	A 3/		C.7.5.4.1
	X		Temperature cycling	1010	C, 20 cycles	C, 100 cycles		C.7.5.4.2
		X	Temperature cycling	1010	C, 10 cycles	C, 100 cycles		C.7.5.4.2
	X	X	Mechanical shock	2002	B, Y1 direction 4/	B, Y1 direction		C.7.5.4.3
	X	X	Constant acceleration	2001	3,000 g's, Y1 direction 4/	5,000 g's, Y1 direction		C.7.5.4.4
	X	X	Random vibration 5/	2026	N/A	F		C.7.5.4.5
	X	X	Seal (fine and gross) 6/	1014				
	X	X	PIND	2020	N/A	A, 1 pass 3/		C.7.5.4.1
	X	X	Visual examination	1010				C.7.5.4.6
	X	X	End-point electrical	7/				C.7.5.4.7
2	X	X	Steady-state life test	1005	1,000 hours at +125°C or equivalent in accordance with method 1005	1,000 hours at +125°C or equivalent in accordance with method 1005	8/ 22 (0) or 5 (0)	C.7.5.4.8
	X	X	End-point electrical	7/				C.7.5.4.7
3	X	X	Internal gas analysis	1018			9/ 3 (0)	C.7.5.4.9
4	X	X	Internal visual	2017	Option 1 only		9/ 2 (0)	C.7.5.4.10
	X	X	Wire bond strength	2011	Option 1 only			C.7.5.4.11, C.6.3.3.2
	X	X	Element shear	2019 or 2027	Option 1 only			C.7.5.4.12, C.6.3.3.3
5 10/	X	X	ESD a. End point electrical b. ESDS c. End point electrical	3015	Group A-1 Group A-1	N/A	3 (0)	C.6.3.3.4

See footnotes at end of table.

Group D Package Related Tests

TABLE C-Xd. Group D package related tests.

Subgroup	Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
		Method	Condition		
1	Thermal shock	1011	C	5(0)	
	Stabilization bake	1008	+150°C, 1 hour	5(0)	
	Lead integrity	2004 2028	B2 (lead fatigue) D (leadless chip carrier) B1 for rigid leads (pin grid array leads)	1(0)	C.6.4.4.3
	Seal: a. Fine b. Gross	1014	 A or B C or D	5(0)	
2	Not used				
3	Salt atmosphere	1009	A	5(0)	C.6.4.4.4
4	Metal package isolation	1003	600 V dc, 100 nA maximum	3(0)	C.6.4.4.5

Appendix D – Non-Hermetic Devices

- Definitions
  - **Non-hermetic device** - A device which has all or some of the elements not hermetically sealed and is categorized as follows:
    - a. **Cavity non-hermetic device** - A cavity device having construction utilizing non-hermetic (polymeric) seals.
    - b. **Non-cavity non-hermetic device** – A non-cavity device having construction utilizing molding compounds or other materials encapsulation the internal elements.
    - c. **Open non-hermetic device** – A open device having construction with minimal or no protection of the internal elements.
    - d. **Open architecture device (OA)** – A single substrate with hermetically sealed hybrid or multichip cavity(s) in which all bare die, chip and wire, or flip chip are mounted in the hermetically sealed area. Non-hermetic packaged components integral to the substrate (resistors, capacitors, coils, tranformers, and transistors) which are typically mounted on printed circuit boards are not hermetically sealed.

MIL-PRF-38535 - Integrated Circuits

MIL-PRF-38535

Integrated Circuits (Microcircuits) Manufacturing, General Specification for
FSC: 5962, Revision: L, Dated: 06 December 2018

The basic section of this specification has been structured as a performance specification, which is supplemented with detailed appendices.

Appendix A is mandatory for manufacturers of device types supplied in compliance with MIL-STD-883 and forms the basis for QML classes Q, V and Y.

Appendix B is intended for **space application** and is required for class V and class Y (class level S) devices.

Appendix C is mandatory for devices requiring **radiation hardness assurance** (RHA).

Appendix D is mandatory for statistical sampling, life test, and qualification procedures used with microcircuits.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits.

Screening Tests	MIL-STD-883, test method (TM) and conditions		
	Class Q (class level B)	Class V (class level S)	Class Y (class level S)
1. Wafer lot acceptance test	QM plan (see H.3.2.1.4) 1/	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)
2. Nondestructive bond pull (NDBP) test 2/		TM 2023	TM 2023
3. Internal visual inspection 3/	TM 2010, condition B	TM 2010, condition A	TM 2010, condition A
4. Temperature cycling 4/	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum
5. Constant acceleration 5/	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only
6. Visual inspection 6/	100%	100%	100%
7. Particle Impact Noise Detection (PIND) test 7/ 8/		TM 2020, test condition A on each device	TM 2020, test condition A on each device
8. Serialization 9/	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)
9. Pre burn-in (Interim) electrical parameters test 10/	In accordance with device specification 11/	In accordance with device specification 12/	In accordance with device specification 12/
10. Burn-in test: 10/ 13/ 14/	TM 1015 160 hours at +125°C minimum	TM 1015 240 hours at 125°C, condition D 15/	TM 1015 240 hours at 125°C , condition D 15/
11. Post burn-in (Interim) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/
12. Reverse bias burn-in test (Static burn-in) 13/ 14/ 16/		TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum
13. Post burn-in (Interim-reverse bias) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

Screening Tests	MIL-STD-883, test method (TM) and conditions		
	Class Q (class level B)	Class V (class level S)	Class Y (class level S)
14. Percent defective allowable (PDA) calculation 17/	5 percent PDA (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)
15. Final electrical tests 18/ (see table III) a. Static test : (1) at 25°C (2) Maximum and Minimum operating temperature b. Dynamic or functional test : 19/ (1) at 25°C (2) Maximum and Minimum operating temperature c. Switching test : (1) at 25°C (2) Maximum and Minimum operated temperature	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)
16. Seal test 20/ a. Fine leak b. Gross leak	TM 1014	TM 1014	Not applicable
17. Radiographic (X-ray) and/or SAM test 21/		X-ray: TM 2012, Two views; SAM TM 2030	X-ray: TM 2012, Two views; SAM TM 2030
18. External visual inspection 22/ 23/	TM 2009	TM 2009	TM 2009
19. Qualification or quality conformance inspection/TCI test sample selection	24/	24/	24/
20. Radiation dose rate induced latch-up test 25/	TM 1020	TM 1020	TM 1020

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

1/ Testing per manufacturer's QM plan. See paragraph H.3.2.1.4 of MIL-PRF-38535 or TM 5007 of MIL-STD-883.

2/ For flip chip packages Nondestructive bond pull (NDBP) test is not required.

3/ Unless otherwise specified, at the manufacturer's option for test samples selection of group B, bond strength test (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam), and unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controlled environment until sealed. Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3 method 5004 of MIL-STD-883). For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 should be used. For flip chip devices, both internal visual and SAM inspection (such as prior to bump attach to die and after bump attach to substrate and underfill cured etc.) shall be performed in accordance with TM 2010 and TM 2030.

4/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of PIDTP and QM plan.

5/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.

6/ At the manufacturer's option, external visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

7/ See paragraph A.4.6.3 of appendix A and paragraph B.4.1 of appendix B of MIL-PRF-38535. The PIND test may be performed in any sequence after temperature cycling test and prior to post burn-in (interim) electrical parameters test.

8/ For device without a cavity or for flip chip devices with underfill, PIND test is not applicable.

9/ Class V or class Y (class level S) devices shall be serialized prior to the first recorded electrical measurement in screening. Class Q (class level B) microcircuits shall be serialized if delta calculations or matching characteristics are a requirement of the device specification. Each microcircuit shall be assigned a unique serial number in order to trace the data back to an individual device within the inspection lot which shall, in turn, be traceable to the wafer lot from which the device originated.

10/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when PDA is specified (Ref. test step 14: PDA calculation, and footnote 17 herein). If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or standard microcircuit drawing (SMD). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to the time and temperature effects of burn-in and the most effective in removing electrically defective devices.

11/ When specified in the applicable device specification, 100 percent of the devices shall be tested and the results recorded for those parameters requiring delta calculations.

12/ For class V and class Y (class level S) microcircuit devices, delta measurements shall be performed. The specific delta parameters shall be as defined in the applicable device specification. Pre burn-in and post burn-in interim electrical parameters shall be read and recorded when delta measurements have been specified as part of post burn-in electrical measurements, 100 percent of the devices shall be tested and the results shall be recorded for those parameters requiring delta calculations.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

13/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with SMD section 4.2, or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the wafer lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request. For devices with solder terminations, burn-in test may be performed before solder balls/columns have been attached to the packages.

14/ When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in , it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (e.g, to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

15/ Where applicable(for new product families or new technology devices use JEDEC publication JEP163) , dynamic burn-in test shall be performed, and test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class V or class Y (class level S), burn-in test shall be performed in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the qualifying activities for dealing with lot failures.

16/ The reverse bias burn-in is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be a concern. When reverse bias burn-in is not required, interim post burn-in electrical parameter measurements shall be omitted. The order of performing the burn-in test and the reverse bias burn-in test may be inverted. Static burn-in may be substituted for high temperature reverse bias burn-in based on device technology and must be approved by the QA. Moreover, burn-in time-temperature regression table I of TM 1015 of MIL-STD-883 can be used for determination of reverse bias burn-in time and temperature.

17/ The percent defective allowable (PDA) shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class V or class Y (class level S) the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater (see A.4.6.1.1 and A.4.6.1.2 of MIL-PRF-38535). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

18/ Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of table III, group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification. For solder termination devices, ball grid array (BGA) packages electrical test shall be performed across the full military temperature range after attachment of the solder balls on the package, and for column grid array (CGA) packages, electrical test shall be performed across the full military temperature range before attachment of the solder columns on the package. After column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.

19/ Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH}(min)$ +20 percent, -0 percent; $V_{IL} = V_{IL}(max)$ +0 percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH}(min)$ and $V_{IL}(max)$ requirements are not violated at the device terminals.

20/ The fine and gross leak seal tests shall be performed separately or together, between constant acceleration and external visual inspection test. For class level S and class level B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal or external visual inspection shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method TM 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (method TM 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class level S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal, but before external visual, if the devices are installed in individual carriers during electrical test.

21/ The radiographic and/or SAM screening test may be performed in any sequence after serialization. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides. For flip chip technology, only SAM inspection is required. SAM inspection may be performed in any sequence after underfill cure for flip chip technology. For additional requirements for this test, see appendix B paragraph B.4.1 of MIL-PRF-38535.

22/ External visual inspection shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

23/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

24/ Samples shall be randomly selected from the assembled inspection lot for testing in accordance with the specific device class and lot requirements of Group A, B, C, D, E and applicable appendices of MIL-PRF-38535 or TM 5005 of MIL-STD-883; after the specified screen requirements herein table IA or TM 5004 have been satisfactorily completed.

25/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, it may be performed at any screening operation step after seal test, at the manufacturer's option. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the device specification. The PDA for each inspection lot for class V or class Y (class level S) sublot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.

TABLE III. Group A (electrical tests) . 1/

Subgroups	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.) 2/ 3/ 4/ 5/		
		Class Q (class level B)	Class V 6/ (class level S)	Class Y 6/ (class level S)
1	Static tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
2	Static tests at maximum rated operating temperature			
3	Static tests at minimum rated operating temperature			
4	Dynamic tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
5	Dynamic tests at maximum rated operating temperature			
6	Dynamic tests at minimum rated operating temperature			
7	Functional tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
8A	Functional tests at maximum rated operating temperature			
8B	Functional tests at minimum rated operating temperature			
9	Switching tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
10	Switching tests at maximum rated operating temperature			
11	Switching tests at minimum rated operating temperature			

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/ herein) may be conducted individually or combined into sets of tests, subgroups (as defined in table III), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in 2/ herein, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For those lots having a quantity of less than 116 devices, the test shall be imposed on a 100 percent basis with zero failure.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For device class V or class Y (class level S), if the testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

6/ For class V and class Y, group A electrical tests additional requirements see paragraph B.4.3 appendix B of MIL-PRF-38535.

TABLE II. Group B tests (Mechanical and environmental test)

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 1	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)		a. Physical dimensions 3/ TM 2016 2(0) b. Internal gas analysis (IGA) test TM 1018 3(0) 3/ 4/ 5/ (5,000 ppm maximum water content at 100°C)
Subgroup 2 6/	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Resistance to solvents 2/ TM 2015 3(0)	a. Resistance to solvents 2/ TM 2015 3(0) b. Internal visual and mechanical TM 2013, TM 2014 2(0) c. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H d. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) e. Flip chip pull off test TM 2031 or TM 2011 2(0) f. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)

TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 3 sample size 22(0) (22 leads from 3 devices) 8/	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C
Subgroup 4 sample size 45(0) 3/		For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)	For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package - TM 2038 (45 columns from 2 devices minimum)		a. Lead integrity TM 2004 9/ (Test condition B2, lead fatigue) b. Seal test TM 1014 as applicable (1) Fine leak (2) Gross leak c. Lid torque TM 2024 10/ as applicable d. For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)

TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 5				a. Bond strength TM 2011 15(0) 11/ (1) Thermo compression - Test condition C or D (2) Ultrasonic - condition C or D (4) Beam lead - condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	sample size 45(0) a. End-point electrical parameters 12/ - As specified in the applicable device specification b. Steady state life test 13/ TM 1005 Test condition C, D or E c. End-point electrical parameters 12/ - As specified in the applicable device specification
Subgroup 6 Sample size 15(0) 14/					a. Temperature cycling TM 1010, condition C, 100 cycles minimum b. Constant acceleration TM 2001, condition E, Y_1 orientation only c. Seal test TM 1014 (1) Fine leak (2) Gross leak d. End-point electrical parameters - As specified in the applicable device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.

2/ Resistance to solvents testing required only on devices using inks or paints as a marking medium.

3/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot. For devices with solder terminations, Physical dimension test shall be performed with balls/columns.

4/ This test is required only, if it is a glass-frit-sealed package. Unless handling precautions for beryllium packages are available and followed TM 1018, procedure 3 shall be used (see group D, subgroup 6 of table V). For class Y non-hermetic microcircuits devices Internal gas analysis (IGA) test is not applicable.

5/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturer's option, if the initial test sample fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the test data from both submissions is submitted to the qualifying activity.

6/ For all devices, except flip chip, the die shear test or substrate attach strength or stud pull test including passive elements shall be performed per TM 2019 or TM 2027, as applicable. For flip chip devices, flip chip pull off test shall be performed per TM 2031 or TM 2011. Flip chip die shear test or substrate attach strength test shall be performed after underfill is cured per TM 2019 or TM 2027. If the flip chip device uses passive elements the substrate attach strength or stud pull test shall also be performed per TM 2019 or TM 2027. For solder termination devices, subgroup 2 test may be performed without balls and columns attached.

7/ Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition H is the number of dice (not bonds) (see TM 2011).

8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003.

9/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 10/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use TM 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need to be performed only on packages having leads exiting through a glass seal. For LGA/BGA/CGA packages, TM 2004 does not apply.

10/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

11/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in table IA herein or TM 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see TM 2011).

12/ Read and record group A subgroups 1, 2 and 3.

13/ The alternate removal-of-bias provisions of 3.3.1 of TM 1005 shall not apply for test temperature above 125°C.

14/ For devices with solder terminations, Temperature cycling and Constant acceleration test may be performed without balls/columns attachment.

TABLE IV. Group C life tests .

Subgroup	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B) 1/	Class V (class level S) 1/ 2/	Class Y (class level S) 1/ 2/
Subgroup 1	a. Steady-state life test	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C
	b. End-point electrical parameters	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification

1/ Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-months period.

2/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with table IV herein. Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

(a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

(b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

(c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

TABLE V. Group D tests (Package related test) .

Subgroups test	Tests 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 1 sample size 15(0) 2/	Physical dimensions	TM 2016	TM 2016	TM 2016
Subgroup 2 sample size 45(0) 2/ 3/	a. Lead/terminal integrity test	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style
	b. Seal test 4/ (1) Fine leak (2) Gross leak	b. TM 1014 Test condition as applicable	b. TM 1014 Test condition as applicable	b. 5/
	c. For BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages
	(i) Ball shear test for BGA package	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)
	(ii) Solder column pull test for CGA package	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)
Subgroup 3 sample size 15(0) 6/ 7/	a. Thermal shock	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum
	b. Temperature cycling	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum
	c. Moisture resistance	c. TM 1004 8/	c. TM 1004 8/	c. HAST in accordance with JESD22-A118, condition B
	d. Visual examination	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010
	e. Seal test 9/ (1) Fine leak (2) Gross leak	e. TM 1014 test condition as applicable	e. TM 1014 test condition as applicable	e. 5/
	f. End-point electrical parameters 10/	f. As specified in the applicable device	f. As specified in the applicable device	f. As specified in the applicable device

TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 4 sample size 15(0) 6/ 7/	a. Mechanical shock	a. TM 2002 condition B minimum	a. TM 2002 condition B minimum	a.TM 2002 condition B minimum
	b. Vibration, variable frequency	b. TM 2007 condition A minimum	b. TM 2007 condition A minimum	b.TM 2007 condition A minimum
	c. Constant acceleration 11/	c. TM 2001 Test condition E, Y1 orientation only	c. TM 2001 Test condition E, Y1 orientation only	c.TM 2001 Test condition E, Y1 orientation only
	d. Seal test (1) Fine leak (2) Gross leak	d. TM 1014 condition as applicable	d. TM 1014 condition as applicable	d. 5/
	e. Visual examination	e. In accordance with visual criteria of TM 2007	e. In accordance with visual criteria of TM 2007	e. In accordance with visual criteria of TM 2007
	f. End-point electrical parameters	f. As specified in the applicable device specification	f. As specified in the applicable device specification	f. As specified in the applicable device specification
Subgroup 5 sample size 15(0) 2/	a. Salt atmosphere	a. TM 1009 Test condition A minimum	a. TM 1009 Test condition A minimum	a. TM 1009 Test condition A minimum
	b. Visual examination	b. In accordance with visual criteria of TM 1009	b. In accordance with visual criteria of TM 1009	b. In accordance with visual criteria of TM 1009
	c. Seal 9/ (1) Fine leak (2) Gross leak	c. TM 1014 condition as applicable	c. TM 1014 condition as applicable	c. 5/
Subgroup 6 2/ 12/	Internal gas analysis (IGA) test (cavity packages)	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	5/
Subgroup 7 sample size 15(0) 2/ 13/ 14/	Adhesion of lead finish	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025

TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 8 sample size 5(0) 2/	Lid torque 15/	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024
Subgroup 9 sample size 3(0) (3 leads minimum) 16/	a. Soldering heat	Where applicable a. TM 2036	Where applicable a. TM 2036	Where applicable a. TM 2036
	b. Seal (1) Fine leak (2) Gross leak	b. TM 1014 condition as applicable	b. TM 1014 condition as applicable	b. 5/
	c. External Visual examination	c. TM 2009	c. TM 2009	c. TM 2009
	d. End-point electrical	d. As specified in the applicable device specification	d. As specified in the applicable device specification	d. As specified in the applicable device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

1/ In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.

2/ Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5 and 8 tests shall be performed with balls and columns.

3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use TM 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum. For LGA/BGA/CGA packages, TM 2004 does not apply.

4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

5/ This test is not applicable for class Y non-hermetic microcircuits devices.

6/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

TABLE V. Group D tests (Package related test). - Continued.

7/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns.

8/ Lead bend stress initial conditioning is not required for leadless chip carrier packages or BGA/CGA packages. For fine pitch packages (25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.

9/ After completion of the required visual examinations and prior to submittal to TM 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

10/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

11/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.

12/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes, the lot shall be accepted provided the test data from both submissions is submitted to the qualifying activity.

13/ The adhesion of lead finish test shall not apply for leadless chip carrier, land grid array (LGA), ball grid array (BGA), and column grid array (CGA) packages.

14/ Sample size number 15 leads from 3 devices minimum are based on number of leads with zero failure.

15/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

16/ This test is performed at qualification/re-qualification of design changes which may affect this test. The manufacturer shall determine, for each package, the applicable conditions from TM 2036 that are appropriate for the mounting conditions, and assure by testing, or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

Questions?