Testing of Complex FPGAs, Memorys and Microprocessors

Jonathan Hochstetler (Host) / Sultan Lilani (Co-host)

Celebrating Over 35 Years of Providing High Quality Semiconductor Services

INTEGRA TECHNOLOGIES

Webinar Outline

1. What do AC, DC and Functional Testing Mean

2. Advanced Microprocessors / FPGA / Memory
    1. AC/DC and Functional Testing
    2. Device bus cycle timing implementation in ATE environment
    3. Development of ATE based software
    4. Compiled device assembly language loaded to the device
    5. Testing independent of manufacturer proprietary test methods
    6. Tools of testing
    7. How to develop the test vectors and configuration vectors
    8. DDR /DDR2 /DDR3 / DDR4 SDRAM, SSRAM QDR testing protocols
    9. NAND Flash testing protocols
    10. Data Retention and Endurance protocols

3. Temperature Testing

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Let Us Talk Basics

What does AC / DC / Functional Testing Mean

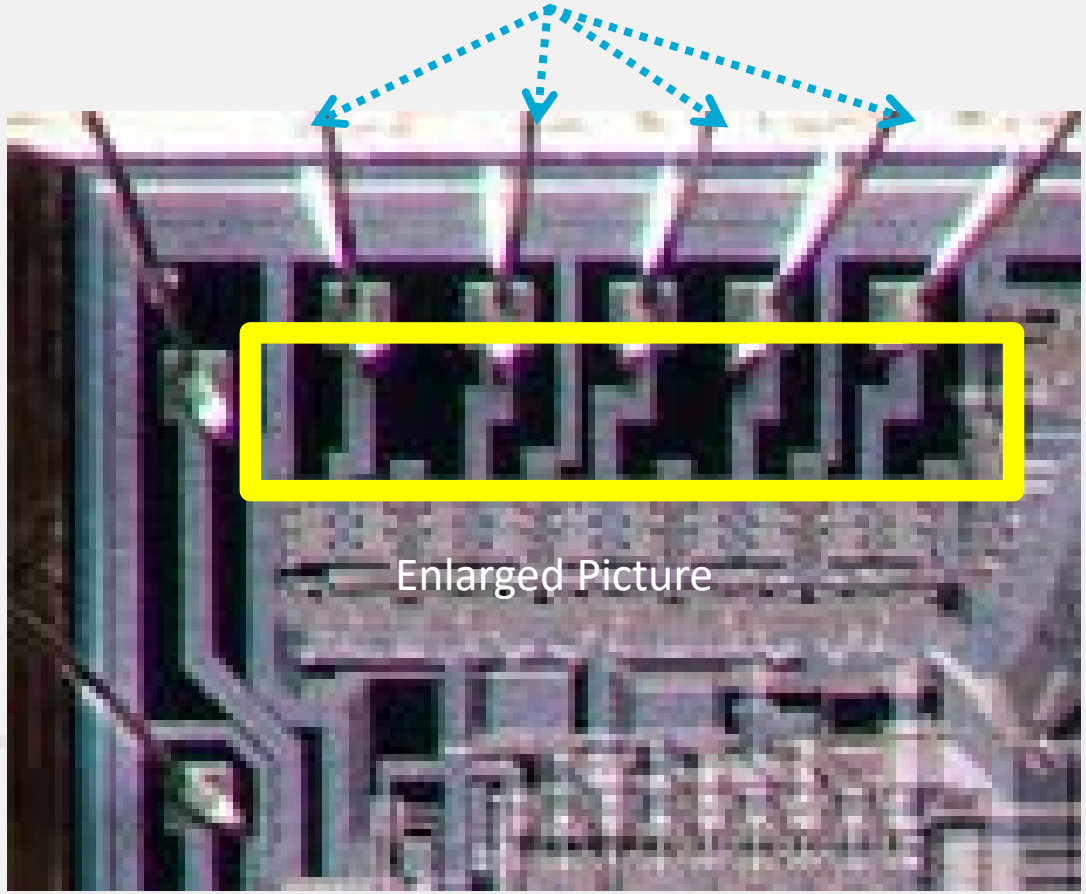
What is DC Testing?

1

Bond wires to the lead frame and then to the external device pins

DC testing only covers the circuitry enclosed in the yellow square

- Essentially the first few transistors of each pin of the device.

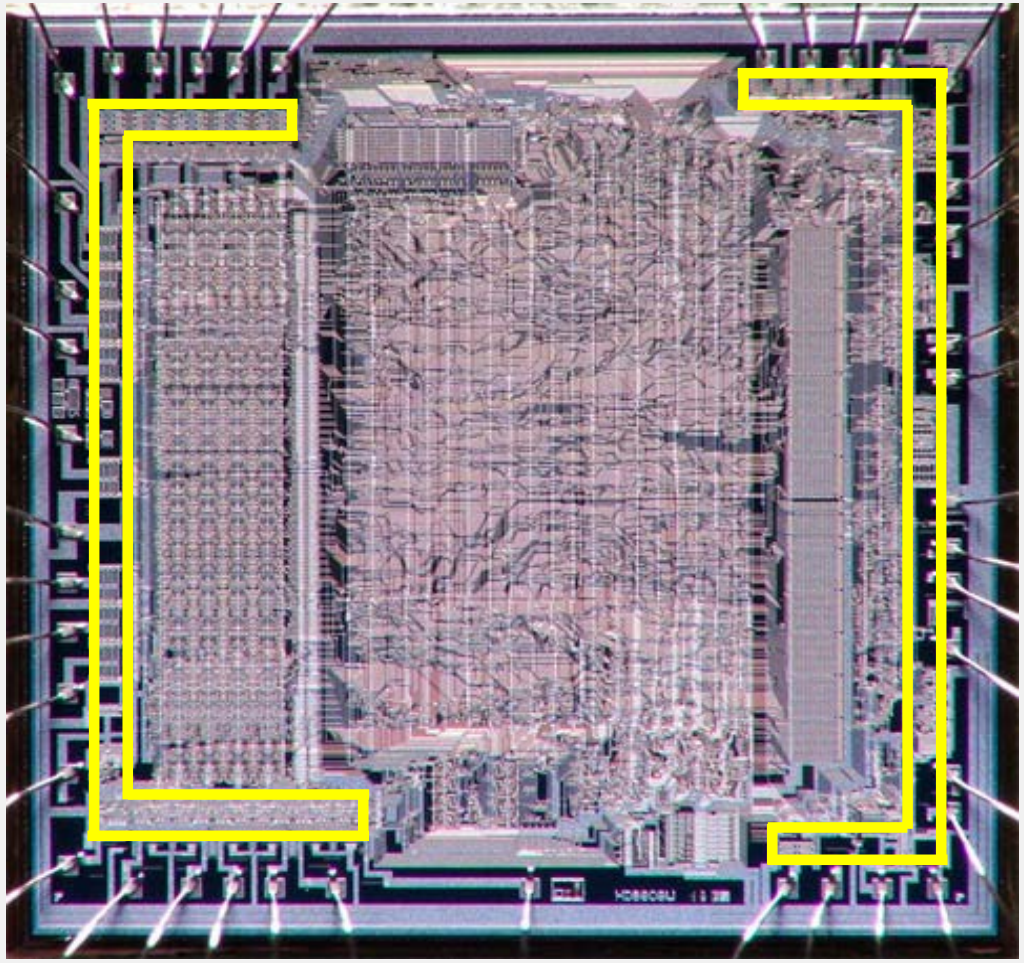


What is DC Testing? [2]

The yellow portion is an estimate of the circuitry that might be tested by DC only testing

What can typical DC testing tell you?

- Electrical Over Stress (EOS) or Electro Static Discharge (ESD).
- If a pin is damaged, but not failing (indicated by higher than normal leakage current).
- IDD power supply current failures.



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What is AC Testing?

1

Table 38: AC Electrical Characteristics (1 of 2)
T_A = -40°C to +85°C, V_{DD} = 2.7-3.6V@33MHz, 4.5-5.5V@40MHz, V_{SS} = 0V

Symbol	Parameter	Oscillator						Units
		33 MHz (x1 Mode) 16 MHz (x2 Mode)[1]		40 MHz (x1 Mode) 20 MHz (x2 Mode)[1]		Variable		
		Min	Max	Min	Max	Min	Max	
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	33	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	16	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	46		35		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low	5				T_{CLCL} - 25 (3V)		ns
				10		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low	5				T_{CLCL} - 25 (3V)		ns
				10		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In		56				$4T_{CLCL}$ - 65 (3V)	ns
					55		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low	5				T_{CLCL} - 25 (3V)		ns
				10		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	66		60		$3T_{CLCL}$ - 25 (3V) $3T_{CLCL}$ - 15 (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In		35				$3T_{CLCL}$ - 55 (3V)	ns
					25		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#					0		ns
T_{PXIZ}	Input Instr Float After PSEN#		25				T_{CLCL} - 5 (3V)	ns
					10		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	22		17		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In		72				$5T_{CLCL}$ - 80 (3V)	ns
					65		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T_{RLRH}	RD# Pulse Width	142		120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	142		120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{RLDV}	RD# Low to Valid Data In		62				$5T_{CLCL}$ - 90 (3V)	ns

Example AC Parametric Table From Data Sheet:

Table 38: AC Electrical Characteristics (Continued) (2 of 2)
T_A = -40°C to +85°C, V_{DD} = 2.7-3.6V@33MHz, 4.5-5.5V@40MHz, V_{SS} = 0V

Symbol	Parameter	Oscillator						Units
		33 MHz (x1 Mode) 16 MHz (x2 Mode)[1]		40 MHz (x1 Mode) 20 MHz (x2 Mode)[1]		Variable		
		Min	Max	Min	Max	Min	Max	
					75		$5T_{CLCL}$ - 50 (5V)	ns
T_{RHDX}	Data Hold After RD#	0		0		0		ns
T_{RHDZ}	Data Float After RD#		36				$2T_{CLCL}$ - 25 (3V)	ns
					38		$2T_{CLCL}$ - 12 (5V)	ns
T_{LLDV}	ALE Low to Valid Data In		152				$8T_{CLCL}$ - 90 (3V)	ns
					150		$8T_{CLCL}$ - 50 (5V)	ns
T_{AVDV}	Address to Valid Data In		183				$9T_{CLCL}$ - 90 (3V)	ns
					150		$9T_{CLCL}$ - 75 (5V)	ns
T_{LLWL}	ALE Low to RD# or WR# Low	66	116	60	90	$3T_{CLCL}$ - 25 (3V) $3T_{CLCL}$ - 15 (5V)	$3T_{CLCL}$ + 25 (3V) $3T_{CLCL}$ + 15 (5V)	ns
T_{AVWL}	Address to RD# or WR# Low	46				$4T_{CLCL}$ - 75 (3V)		ns
				70		$4T_{CLCL}$ - 30 (5V)		ns
T_{WHQX}	Data Hold After WR#	3				T_{CLCL} - 27 (3V)		ns
				5		T_{CLCL} - 20 (5V)		ns
T_{QVWH}	Data Valid to WR# High	142				$7T_{CLCL}$ - 70 (3V)		ns
				125		$7T_{CLCL}$ - 50 (5V)		ns
T_{QVWX}	Data Valid to WR# High to Low Transition	10		5		T_{CLCL} - 20		ns
T_{RLAZ}	RD# Low to Address Float		0		0		0	ns
T_{WHLH}	RD# to WR# High to ALE High	5	55			T_{CLCL} - 25 (3V)	T_{CLCL} + 25 (3V)	ns
				10	40	T_{CLCL} - 15 (5V)	T_{CLCL} + 15 (5V)	ns

T0-0.0 25093

1. Calculated values are for x1 Mode only

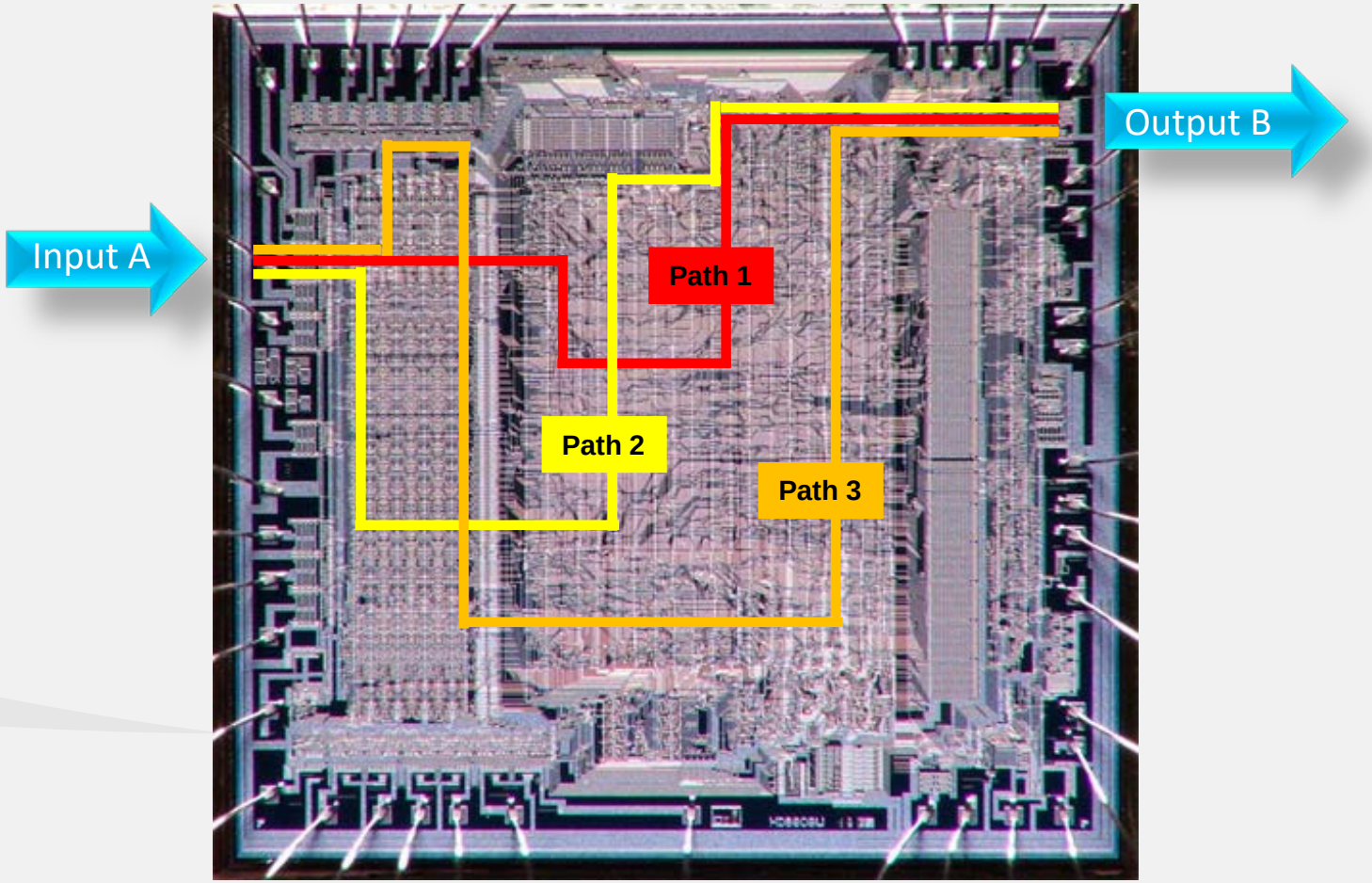
Source: Microchip FlashFlex MCU Datasheet, 02/13

What is AC Testing?

Propagation Delay Example

There may be several 100's or 1000's of paths through a device that are represented by a single AC parameter. Each path needs to be evaluated to determine if they all work.

In this case there are 3 paths from Input A to Output B. Path 3 is clearly the longest and is likely the worst case propagation delay path for this AC parameter.



What is AC Testing? [3]

AC testing will tell you the speed at which things happen in the device like:

- How long does it take to access an address (access time).
- How long does it take for one signal occur after another (prop. delay).
- Maximum operating frequency.
- Signal rise and fall times.

But AC testing by itself, while better than just DC testing, still only tests a small percentage of the die at any one time.

What is Functional Testing?

1

Functional testing is making sure that all of the functions that a device can perform are exercised.

Ironically it is usually the area of the device that is the least explained in the datasheet.

The development of the functional test area of a complex parts accounts for 50% to 90% of the overall test development effort and cost

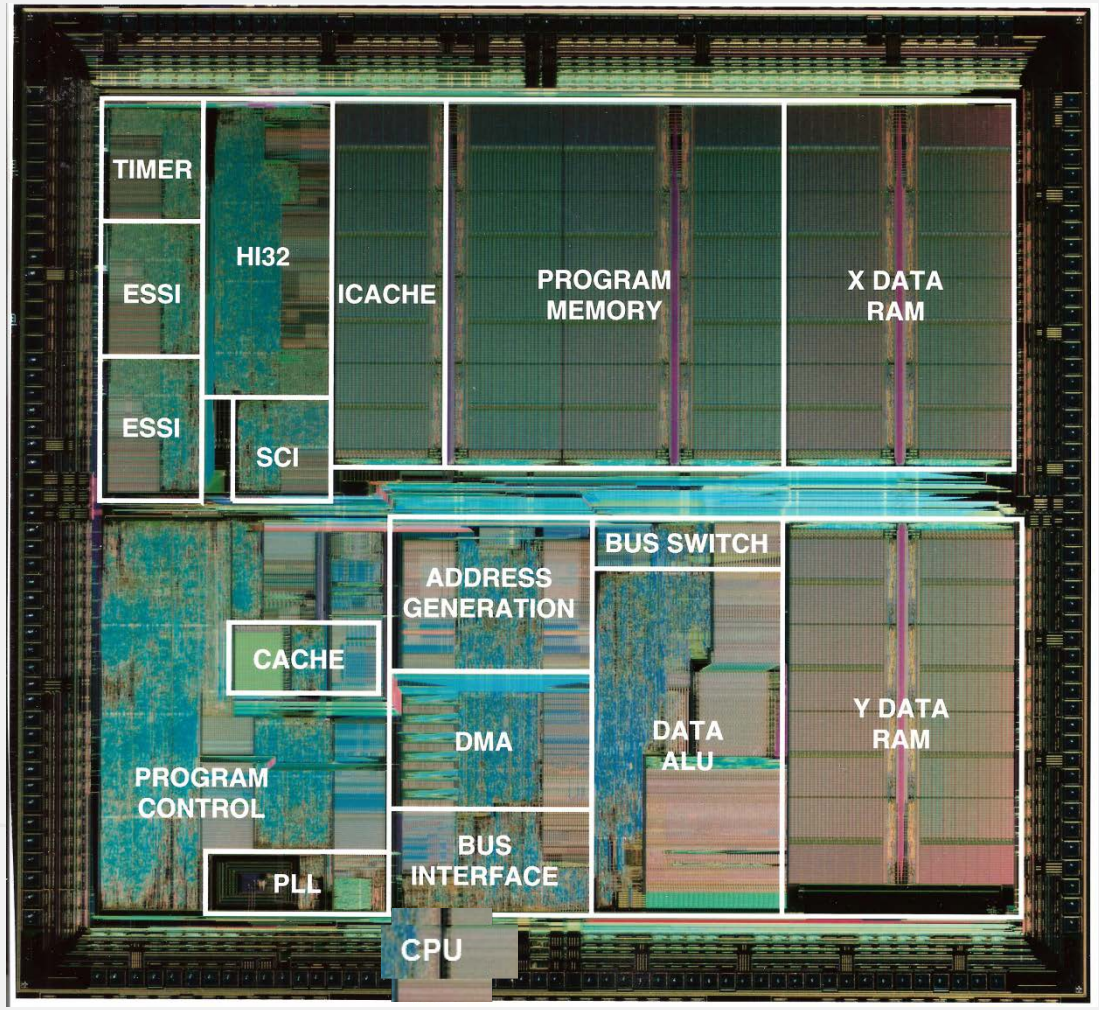
What is Functional Testing?

2

Functional testing requires that each functional block in a device be thoroughly tested.

This is where up to 90% of the test development effort lies when doing a complex part.

Each white named area is a functional block for this device.

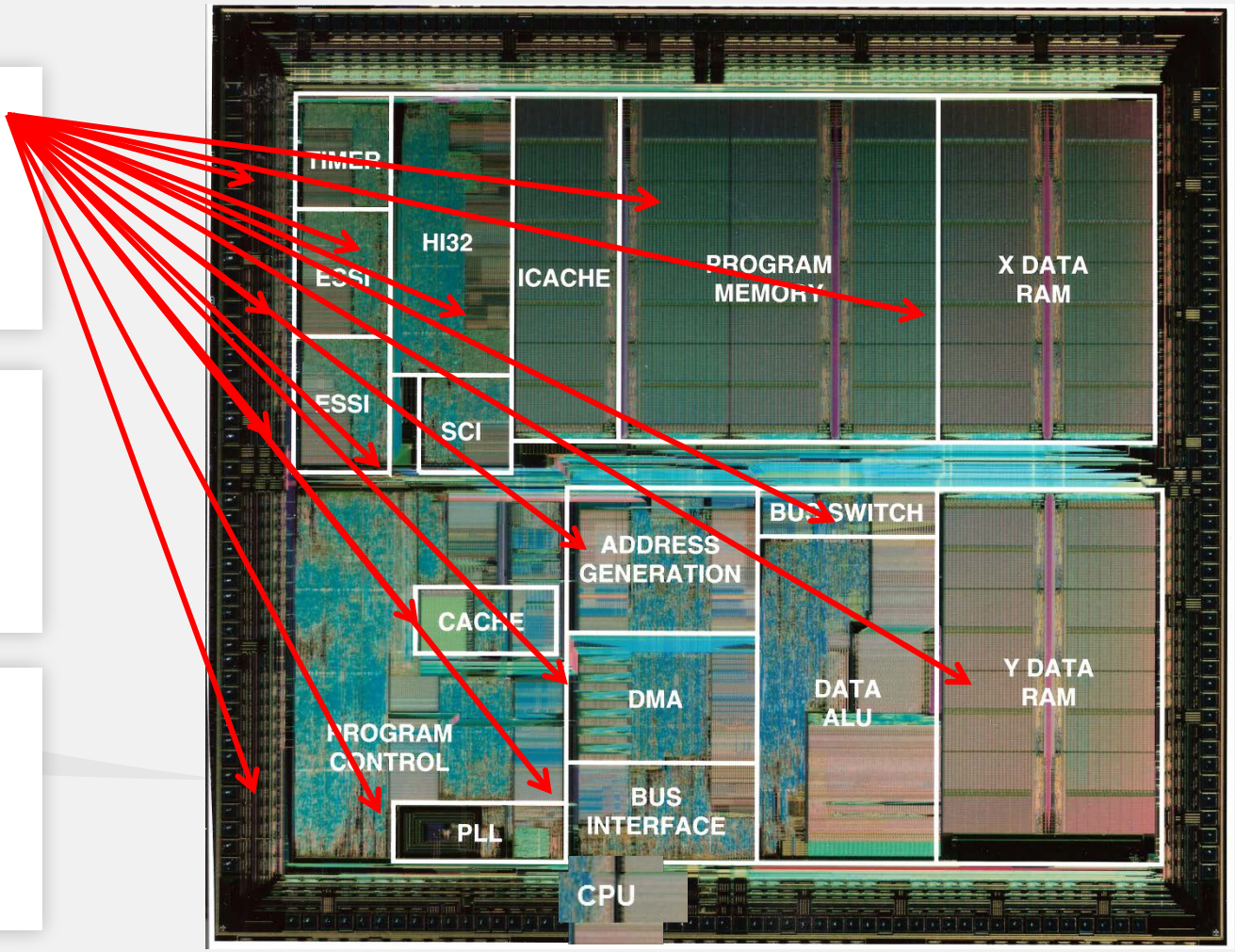


What is Functional Testing?

For a full coverage test plan; we need each of the 16 functional blocks in this device.

This can make functional testing very time consuming and very expensive.

What can happen if all functional blocks are not tested? Test escape!



Cost to Develop A Relatively Simple 8051 8-bit Microcontroller

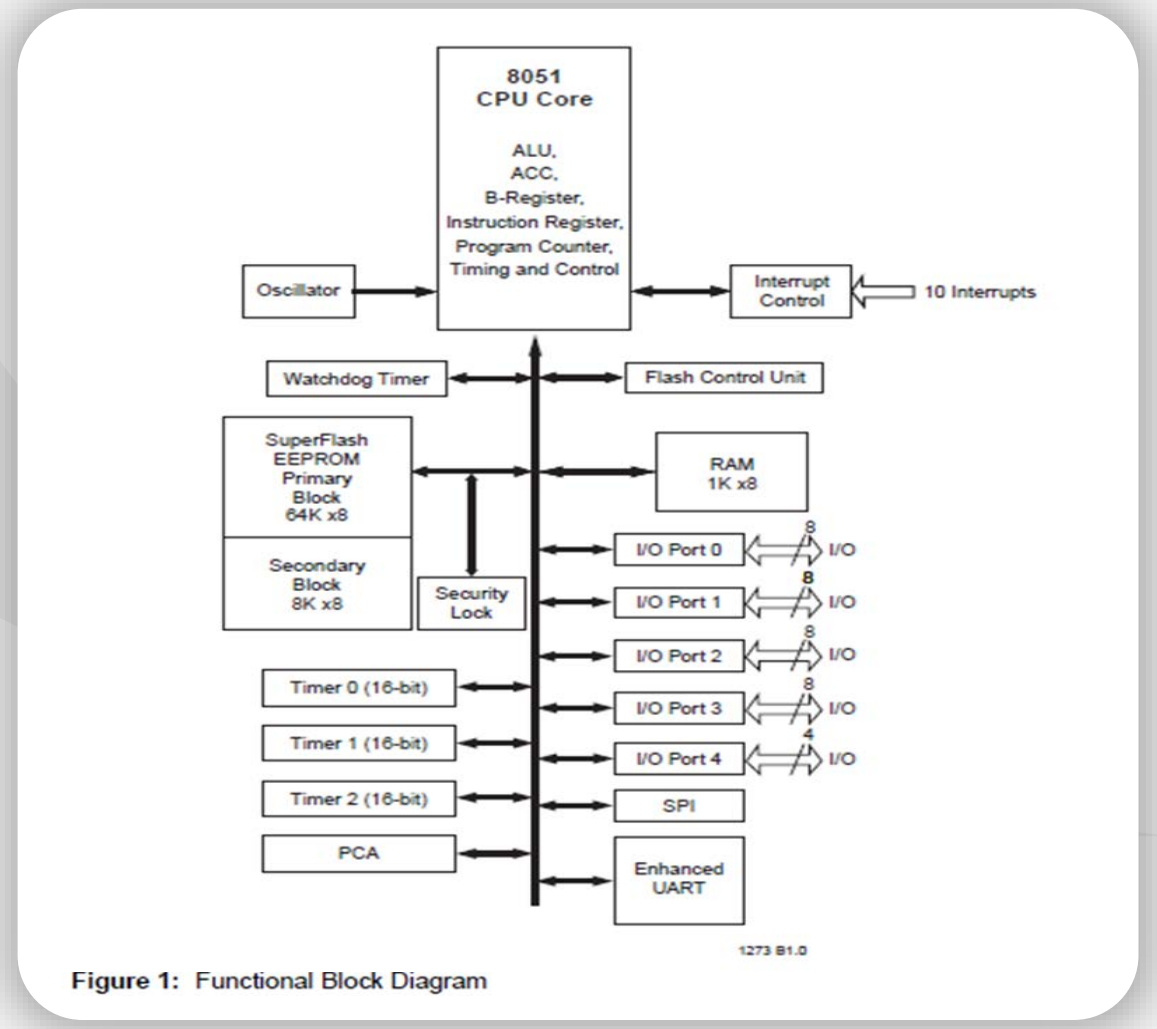
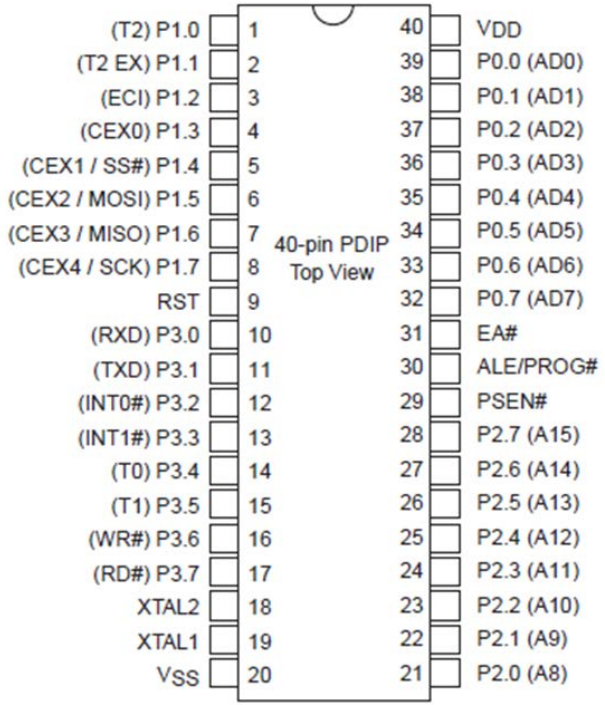


Figure 1: Functional Block Diagram

Example Block Diagram and pin-out for a legacy 8051 device.



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Test Development Cost Example?

Comprehensive Test Program Development Quotation Example

This is how your test lab should be quoting your project.

Test Development Cost Example			
Test Development Activities	**Engineering Hours**	**Tester Hours**	**Cost***
Test Specifcation Development	20	0	$ 3,000
Test System Selection/Speed	3	0	$ 450
Load Board Design & Fabrication	20	5	$ 3,750
DC Tests	25	20	$ 6,750
Functional Test - MIN/Max Voltages	10	5	$ 2,250
Functional Test - Timing Sets	15	10	$ 3,750
Functional Test - CPU Core	120	80	$ 30,000
Functional Test - Interupt Control	30	20	$ 7,500
Functional Test - Watchdog Timer	20	15	$ 5,250
Functional Test - Flash Control Unit	10	7	$ 2,550
Functional Test - SuperFlash	10	7	$ 2,550
Functional Test - Ram	10	7	$ 2,550
Functional Test - Security Lock	15	10	$ 3,750
Functional Test - I/O Ports	25	17	$ 6,300
Functional Test - Timers	25	20	$ 6,750
Functional Test - SPI Bus	15	10	$ 3,750
Functional Test - UART	40	30	$ 10,500
AC Tests	60	40	$ 15,000
Total	**473**	**303**	**$ 116,400**

* Assumes $150/hr for Engineering time and tester time

* Figures for discussion purposes only - not an actual quotation.

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How Can Test Development Costs be Saved?

Saving Test Development Costs

Since the manufacturer has already thoroughly tested the devices as a part of their original manufacturing flow, the developer is able to limit the counterfeit device testing to match only the actual application conditions.

- ✓ Use actual application speeds.
- ✓ Use actual application programing code (uP and memory).
- ✓ Use actual application designs (FPGA).
- ✓ Test only functional blocks actually used in the application.
- ✓ Test only the AC parameters that are critical to the application.
- ✓ Leverage test programs already developed for the same or similar parts.
- ✓ Use device emulators.
- ✓ Use golden devices to “learn” device functionality.

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2

Testing of Complex Microprocessors, Memories and FPGA

Integra’s Microprocessor Testing Experience

Test Engineering Experience

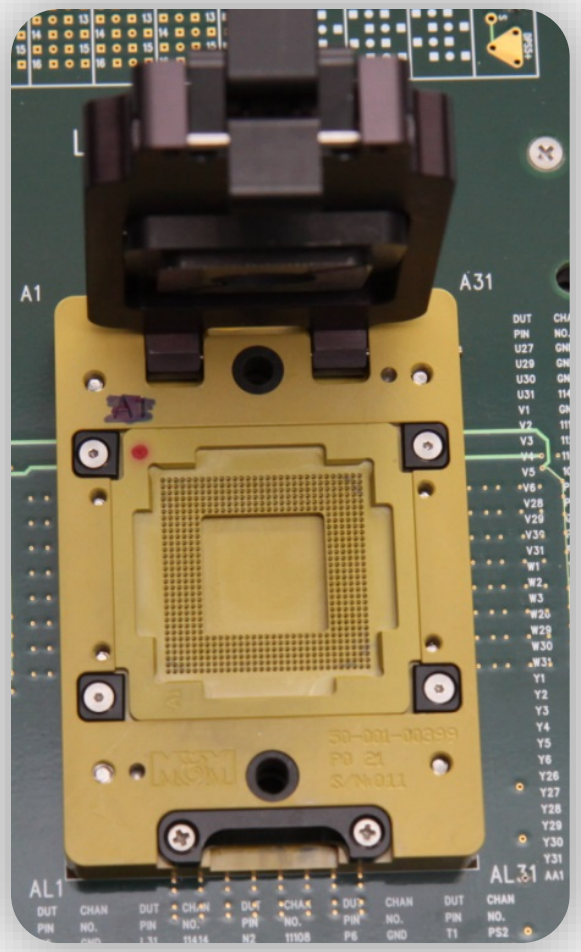
- Integra has developed more than 100 test programs for Processors
- Independent generation techniques without manufacturer support
- 4 engineers with processor development experience

Device Experience

- Intel Family 186,286, 386, 486, Pentium
- Free scale/Motorola Family 68000 to 68040, Power PC and P2020
- Other Manufacturers such as PMC RM7965, TI TMS320C Family

Examples of Programs Include:

- P2020NXE2HHC
- MPC603RRX266TC
- A8050266-133SY022
- RM7965-835T
- TMS320C6713BGDPA200
- ADSP2181BSZ133QM5326



Test Development of Free scale P2020 Microprocessor

- Comprehensive Test Coverage – All Integra Generated Patterns
- 3 Engineers 1400 Engineering Hours - Test Program Development From Scratch
- Completed in Less Than 24 Weeks

Test Coverage	Notes
Continuity	Verify device connectivity
POR	Power On Reset and initialize through the eSPI bus
1st Instruction	1st CPU instruction cycle using eLB and instruction formatting. Part configured for 133Mhz Sysclk, 4:1 ratio for 533 CCB clock and then 1.5:1 ratio for 800MHz eCORE clock.
Dual CPU	Sample math and move instructions for both CPUs using local bus
eLB	The Local Bus will be used for all register read & writes so it will be tested during all blocks. Will test all DC parameters, CLOCK to out, CLOCK to data valid, CLOCK to address valid and CLOCK to LALE assertion
UART	Set all registers to send and receive data on both UARTs using transceiver holding register and receiver buffer register. All DC and max baud rate for AC.
eSPI	Set all registers to send and receive data using FIFO for all chip selects. All DC and Master Data out delay for AC
I2C	Set registers for basic data transfer. All DC except pulse spike. Max clock frequency for AC
DDR3	Enable DDR interface configured for DDR3. AC parametric testing (6) parameters listed below. No DC parametric. Will do some data transfers at 800Mhz. 2.7.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications MCK[n] cycle time tMCK (min)2.5 ns (max)5 ns ADDR/CMD output setup with respect to MCK tDDKHAS 800 Mbps data rate (Min) 0.767 ns ADDR/CMD output hold with respect to MCK tDDKHAX 800 Mbps data rate (Min) 0.767 ns MCS[n] output setup with respect to MCK tDDKHCS 800 Mbps data rate (Min) 0.767 ns MCS[n] output hold with respect to MCK tDDKHCX 800 Mbps data rate (Min) 0.767 ns MCK to MDQS Skew tDDKHMH 800 Mbps data rate (min) –0.525 ns (max) 0.525 ns
Ethernet	Verify Ethernet functionality
MMU, L2 Cache and FPU	Exercise L2 Cache. Assure FPU instructions are tested. Verify MMU mapping from effective addressing to physical addressing

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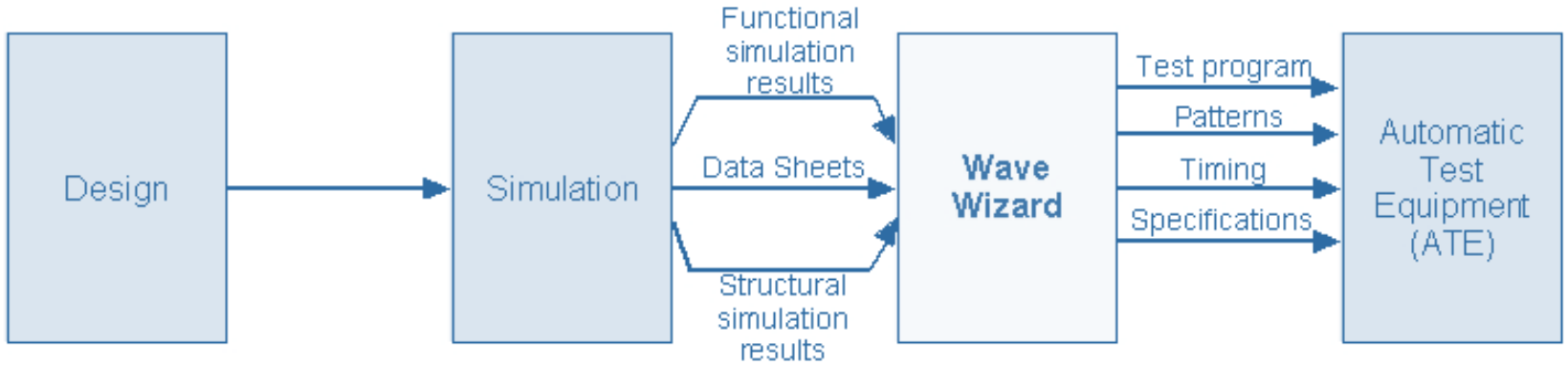
Traditional Test Vector Generation Method

- Device Design Environment
- Modeling Integrated with Design
- Simulation to Generate Test Patterns
  - BIST / SCAN Functional
- Simulation Patterns Converted to Tester Patterns
- Final Test Generated



How to Develop Microprocessor Vectors

Must Fully Understand the Device

- Testers work on time cycles / implement timing model into tester

Build a Microprocessor Development System

Use a Known Good Device

- Hardware simulator is the known good die
- Tester load board and tester resources are the hardware

On Tester Build a Software Model of the Device Interface

- Device bus cycle timing implemented in tester
- Developed tester s/w monitors device operation and pin status
- Complied device assembly language loaded to the device
- The device is operating functionally just as it would in an application

Tester Records the Device Operation

- Saved as a test vector file

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Special Tester Requirements

Tester Algorithmically Writes Vectors on the Fly

- Software routine in the tester reviews each vector
- Next vector is generated according to the device protocol
- Validity of results must be analyzed by engineer

Rewrite Vectors in Memory

- Pass fail pin register allows on-the-fly changes
- Test vector is corrected
- Executable vector code results

Tester Register Stores State of Pass/Fail

- Typically non-user tester registers are required
- Tester hardware manuals are consulted

Incremental Process

- S/W loops executable vectors to correct and add additional vectors
- At completion corrected/generated vectors are saved

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Vector by Vector Generation

Process

- Input to the program is assembled code
- First word of code is converted to binary and applied to input pins
- Control pins are monitored to determine the type of bus cycle (read/write)
- Continue clocking, recording the outputs until the end of that bus cycle
- Read the next word of assembled code and repeat
- Stop when no more input code
- Save memory to file
- Added test methods
- Memory testing
    - Algorithmic Pattern Generation
    - Checkerboard / Invers checkerboard
    - March Patterns
- High Speed BUS testing
    - Loop Back methods high speed serial buses

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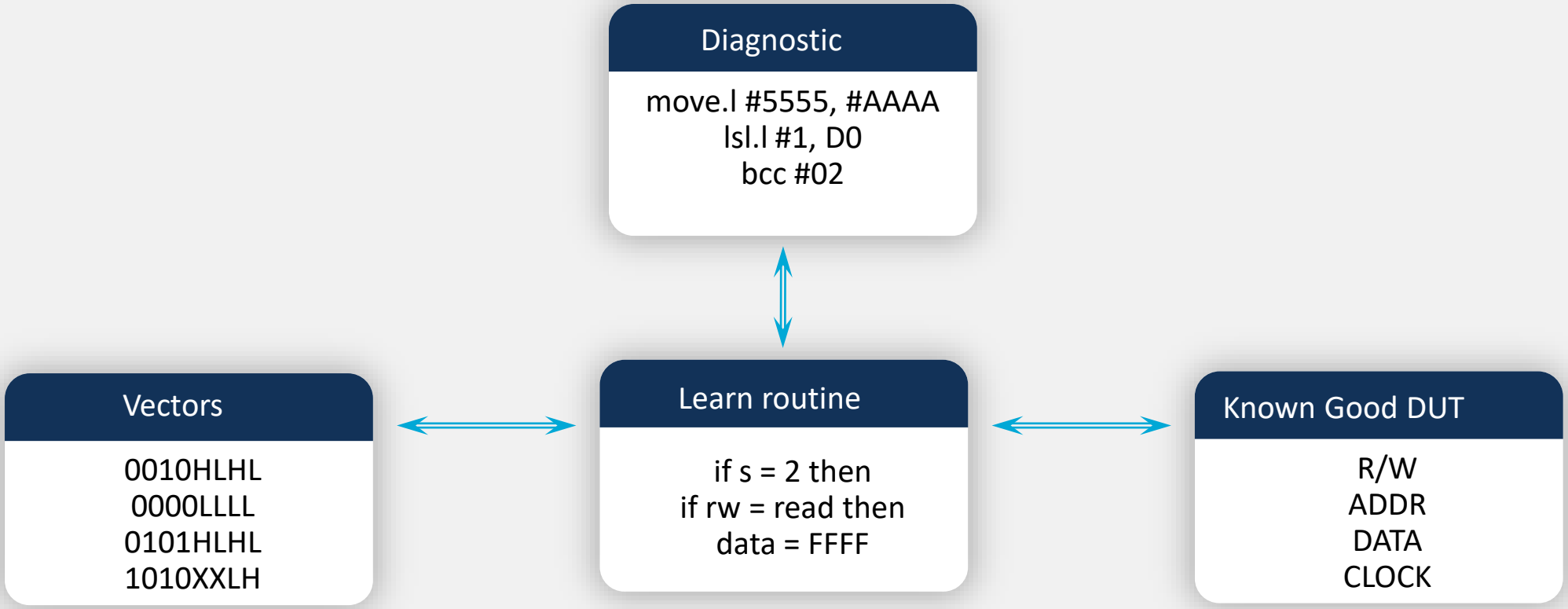
Test Generation



Recommended Test Methodology

Test the Device the Specified Performance Characteristics

- Functional at-speed
  - Application speed at a minimum may not need spec speed
  - Test frequency is a major tester cost driver
- Comprehensive functional testing
  - Test all device functionality
  - Fault grading is not possible
    - Only the manufacturer has device modeling capability
- Test key AC parameters
  - Key parameters are usually referenced to device clocks
    - Propagation delay
    - Setup and hold times
  - Use go-no-go testing to cover most AC parameters
    - Tested over the entire functional pattern
  - Selected AC characterization measurements can be made
- DC measurements to the full specified limits
  - Attempt to test 25C parameters at extended temperatures
  - Limit adjustments may be required after testing
- Select the appropriate tester
  - No one tester can effectively test all technologies

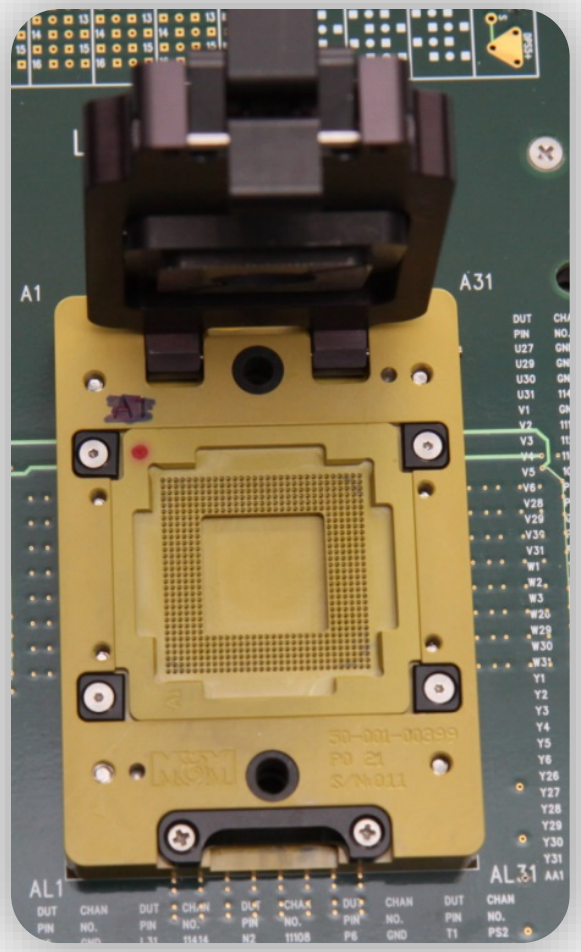
FPGA Development Experience

Over-All

- Integra engineers have developed over 300 test programs for FPGAs
  - Xilinx
  - Intel (Altera)
  - Microchip (Microsemi)
- 150+ FPGA test programs have been developed
- Design software and testing methodologies are in place for all FPGA families
- Integra has an experienced and trained staff in place
  - 5 engineers with FPGA test development experience
  - Multiple projects using Xilinx Vivado Design Suite (ISE)

Xilinx: Examples of Programs Include

- Various Iterations of Virtex 7
- Various Iteration of Virtex 5
- XC4VFX100-11FF1152C
- XQ2VP40-5FF1152N
- XC4VFX20-10FFG672C
- XC6VLX75T-3FF484C
- XC6SLX45-L1CSG324I



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FPGA Test Methodology

Integra Implements Designs into the FPGA to Support Functional and Parametric Testing

- Test develops independent of manufacturer proprietary test methods
- Integra uses in-house tools from the manufacturer
- Create the test vectors and configuration vectors for the 93K tester
- Functional at-speed testing (using design modeling not datasheet)
    - Datasheet AC specs are internal FPGA performance characteristics
    - AC parameter tests will be generated from Xilinx software simulations
- Designs implementation includes comprehensive DC parameters
- Develop functional vectors verifies design and device functionality

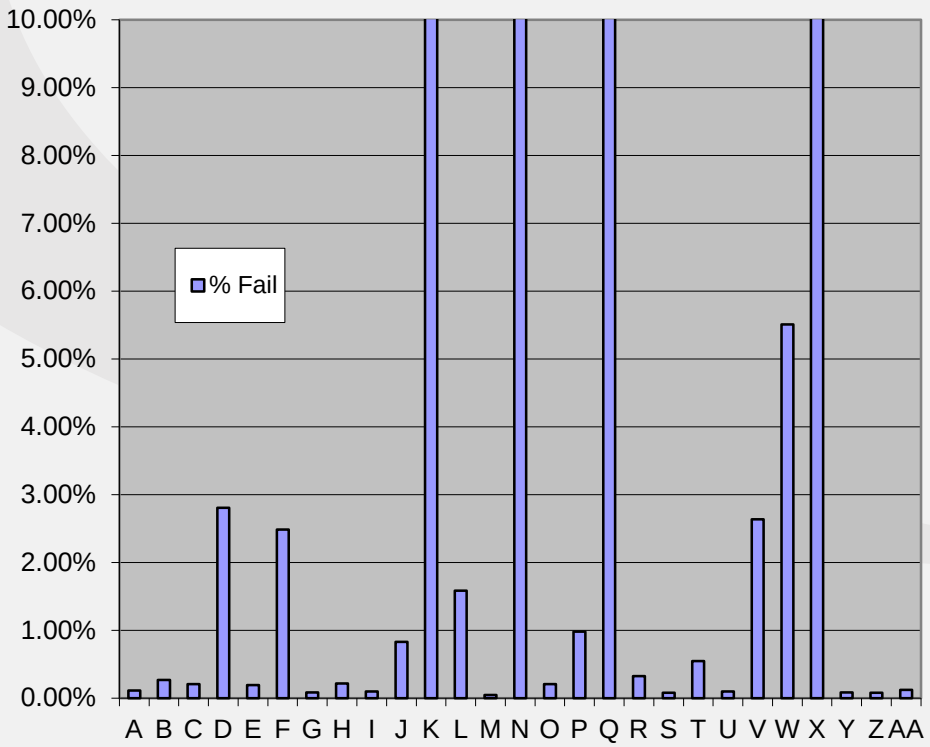
FPGA Test Methodology

Testing to the User Configuration is Also an Effective Test Method

- Functional evaluation to actual application design
- Development of test vectors to user application
- Critical timing parameters testable to the application requirements
- Characterization of device performance to application is possible

Electrical Test of Today's Complex COTs Memory Devices

Not All Manufacturers' Products Created Equal



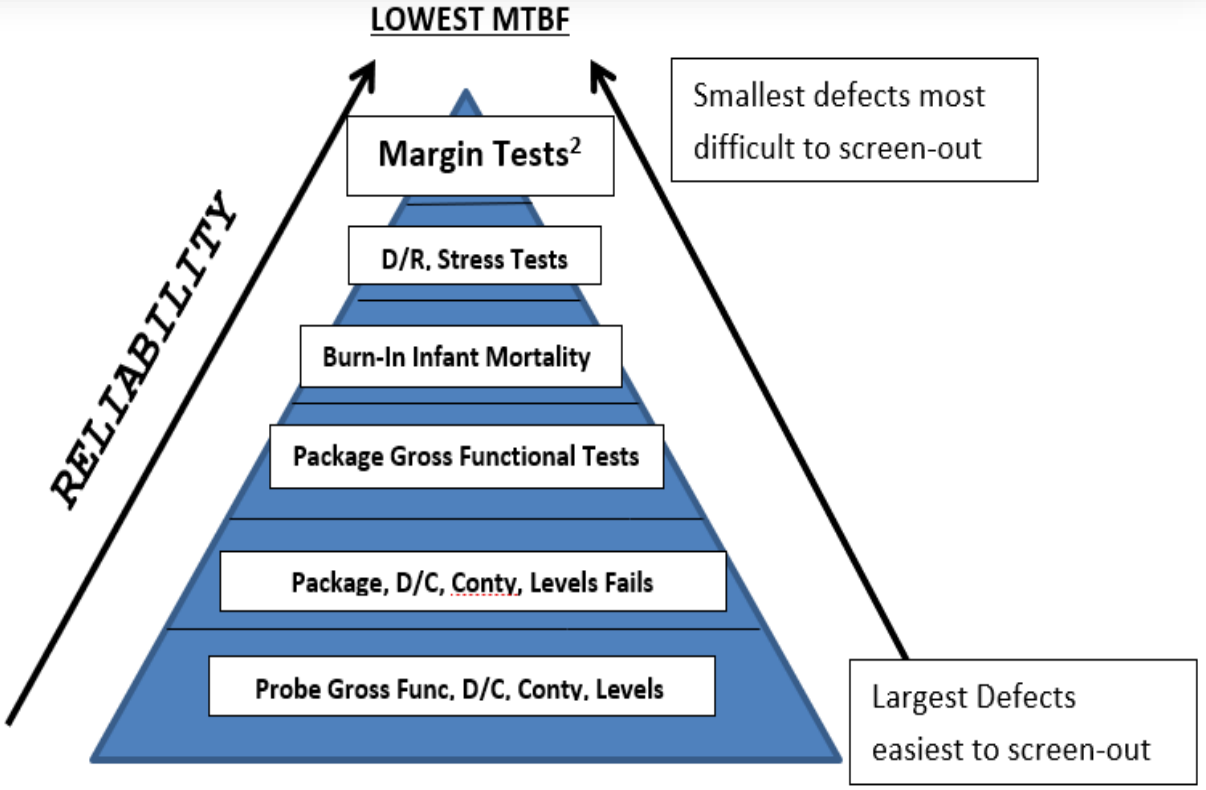


Figure 1: defect removal hierarchy pyramid

Memory Test Complexities

- **Volatile Memory**
- Topological addressing is preferred for all types of RAM memories (proprietary to OEM but covered under NDA)
  - Can't do silicon memory array F/A without this info
  - OEM tests 100% topologically where Row/Column/Block addressed is accomplished from Physical standpoint for best adjacent cell disturb testing in conjunction with Margin testing
- DRAMS: FPM, EDO, VRAM, SDRAM, QDR, DDR, DDR2, DDR3, DDR4 …..
  - TREF(Refresh) parameter always an issue for full Mil-Temp of -55C to 125C, usually ¼ of commercial spec used as TREF halves every 10-12C after 70C. Or user takes yield hit
  - For Mil-Aero use , staying away from the 'just released' versions(i.e.. Die technology shrinks, new fab process, leading edge devices) is good policy
    - Fab process maturity is key Reliability variable so unless you like looking over the edge of cliff's, best to wait 1-yr for process maturity.
    - Request CZ-Data from Commercial Mfg-er , lots of good data nuggets even if only 0-70C, most will do extended Temp CZ of typ -40C to +85C, the more Elite companies like Micron, Samsung, Cypress & TI will do -55C to 125C.
    - If enough volume , parallel site testing preferred like 4-site for lower costs and faster turn at test.
  - Speed is no issue, we can adjust our speed license on the tester as needed up to 3600Mbps.
- SRAMS: Async, Sync, QDR, Serial, NVRAM, Ultra Low Power, MRAM, FRAM. ReRAM, ……..
  - 'Cold Start Power-UP': Ask yourself this question, what power up time assumption is used by the system designer? This is One parameters not normally specified in SRAM datasheet
  - DRAM does a good job of outlining this sequence But SRAM not so good. 10ms would be assumed but I have seen small % of parts not meet this , becomes yield liability
  - ATD (Address Transition Detection) special algorithm needed to target worst case scenario of single address line change that forms the access pulse edges.
    - To catch race conditions on too fast process material
  - Ground bounce affects: this as much about the load board design and decoupling as the output switching rates. The >FFFF to >0000 output switch can be disaster on poor load board design.
  - CMOS Std-by as shown on the opening slide & Weak bit algorithms like specialized Gal-Pat.
  - Still see occasional 4T-2R SRAM cell, in which properly testing Data Retention at cold temp is paramount.

Common Reasons for Testing Memory Devices

Shrinking package sizes means higher densities which translates to increased risk of being affected by even small defects in the manufacturing or assembly processes.

- Activation of unwanted particulate may not be detected without screening at extended temperature.
- Electrical test at application usage condition temperatures can identify potential reliability issues not seen by the OCM at the temperatures used for production testing.

What are the signatures of potential reliability concerns?

- Outlier /atypical standby (quiescent) supply current readings.
- Weak bits that exhibit instabilities at extended temperature or during functional tests that are known to highlight vulnerabilities for a particular type of memory device.
- Cold start issues, especially with DRAM and fast SRAM devices.
- Refresh issues with DRAM devices at elevated temperature.

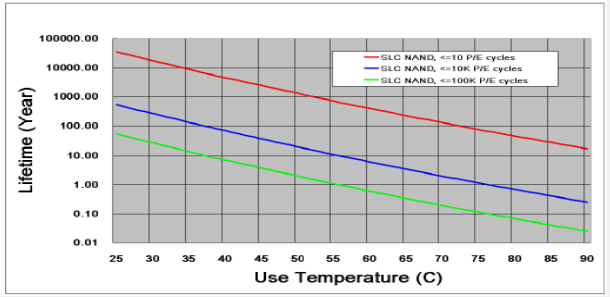
Memorys - Device Specific Functional Tests

- SRAM
  - Data retention tests.
  - Write / Read all 1's, all 0's, checker board and inverse checkerboard patterns.
- Flash
  - Pseudo Random pattern and it's inverse
- EEPROM
  - Checkerboard & Inverse Checkerboard
- DRAM
  - March X

In all cases referenced above, critical timing characteristics are validated by using them as setup parameters for the functional test.

NAND Flash Program/Erase Cycling Endurance & Data Retention

- **Cycling Endurance** defined as the capability to perform to specification if the number of P/E cycles are within the datasheet specification. Typically between 50K to 100K cycles. Certain number of Bad Blocks are allowable which is the NVB(number of valid blocks) min spec.
- **Data Retention(D/R)** defined as is the capability of retaining stored data, in unbiased condition over time; typically 10 years.
  - Note that D/R time for cycled devices decreases as P/E cycle number is increased. See chart below



  - From MXIC 'Technical Brief' on Pgm/erase cycling and D/R connection

- **SLC NAND Flash cell** is predominantly the choice of MILAERO users due to more robust threshold voltage margins on the cell state versus MLC.
  - Additional design mitigation by the user to achieve Longer D/R would be in the form of wear leveling, data refresh, & stronger ECC.
  - **JEDEC Recommended Standards to consider when designing Qual/Reliability Exercise for Endurance/Data Retention**
    - JESD47K "Stress-Test-Driven Qualification of Integrated Circuits"
    - JESD22-A117E "Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance & D/R Stress Test"
    - JESD94A "Application Specific Qualification Using Knowledge Based Test Methodology"
    - JEP122H "Failure Mechanism & Models for Semiconductors Devices"
- **Customer must select Conditions to be used for Endurance/Data Retention normally based on Application usage**
  - # of Pgm/Erase P/E Cycles, fraction of cells cycled to full Spec, Fraction cycled to other percentage(very important for esp large densities), Temperature of Cycling Chamber (25C, 55C or 85C?) , VCC level (nom or max?), Data Pattern to be cycled, If cold temp cycling needed and what conditions, Intentional delays, ECC mgmt applied , periodic reads during endurance or every cycle, UBER value if applicable, # of devices to subjected to what stresses, Arrhenius variables for acceleration calc

Advanced Memory Tester – Smart Scale from Advantest

Group 7	
	Utility
224:	220:
223:	219:
222:	218:
221:	217:
125:	129:
126:	130:
127:	131:
128:	132:
Utility	
Group4	

Group 8	
	Utility
232:	228:
231:	227/427: DPS128-HC
230/430: DPS128-HV	226:
229/429: DPS128-HV	225/425: DPS128-HC
117: PS1600	121: PS1600
118: PS1600	122: PS1600
119: PS1600	123: PS1600
120: PS1600	124: PS1600
Utility	
Group3	

Group 2	
HV-DPS #2	Utility
116: PS1600	112: PS1600
115: PS1600	111: PS1600
114: PS1600	110: PS1600
113: PS1600	109: PS1600
101: PS1600	105: PS1600
102: PS1600	106: PS1600
103: PS1600	107: PS1600
104: PS1600	108: PS1600
Utility	
Group1	

Group 6	
	Utility
216:	212:
215:	211:
214:	210:
213:	209:
201:	205:
202:	206:
203:	207:
204:	208:
Utility	
Group5	

		Number of resources
PS1600	PS1600 dig.Pin	384
DPS128 HV	-6V/15V (Max current 0,2A)	64
DPS128 HC	-2,5V/7V (Max current 0,5A)	64
HV-DPS #2	+ 0.5 V to 22 V (Max current 1A)	4

SmartTest Versions
soc64 7.2.3.5
soc64 7.4.3.4

Z640 PC w/ Red Hat Enterprise Linux 5

Existing test solutions for DDR3,DDR4 are in place with system architecture upgradable to support higher speeds and higher device pin counts.

INTEGRA TECHNOLOGIES

3 Temperature Testing Considerations

Example of Temperature Characterization – 512 NAND Flash - BGA

Characterization Tools & Method

- Four calibrated and certified RTDs part number # HEL-705-U-1-12-C2
- Four calibrated Keithley 2402B source meters
- Threaded ferrules for holding RTDs in socket lid
- One calibrated Temptronic TP04300A Thermostream

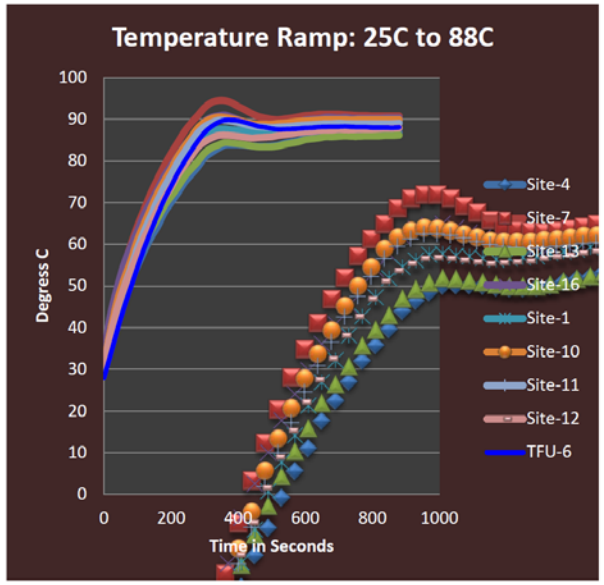
- 8 of 16 sites were measured. The thermostream thermocouple was used in **Site 6**. The measured sites were the four corner and four center sites.
- Temperature was measured from 25C to 88C, 88C to 25C, 25c to -43c, and -43c to 25c; Four sites at a time.
- A program was written to sample the measurements in 20 second increments for a total duration of 15 minutes for each temperature sweep.
- Floor temperature was 22C.
- Data was taken without bias.

Temperature Testing

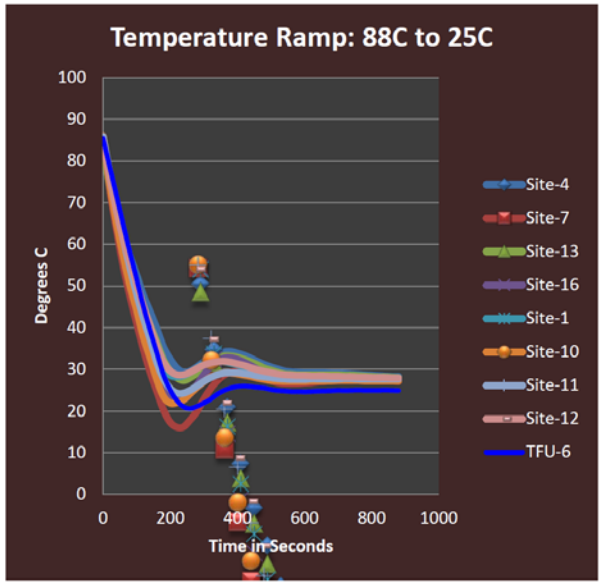
1

Room to High Temperature Characterization Plots

Ramp Temperature for Corner and Center Sites: 25C to 88C



Temperature Ramp for Corner and Center Sites: 88C to 25C



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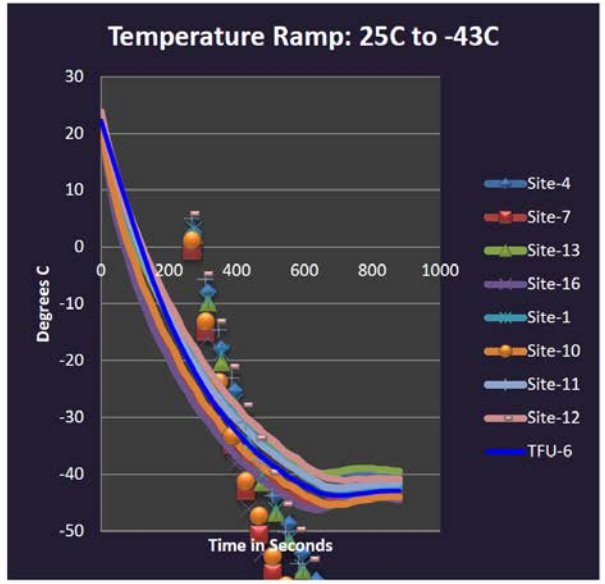
Temperature Testing

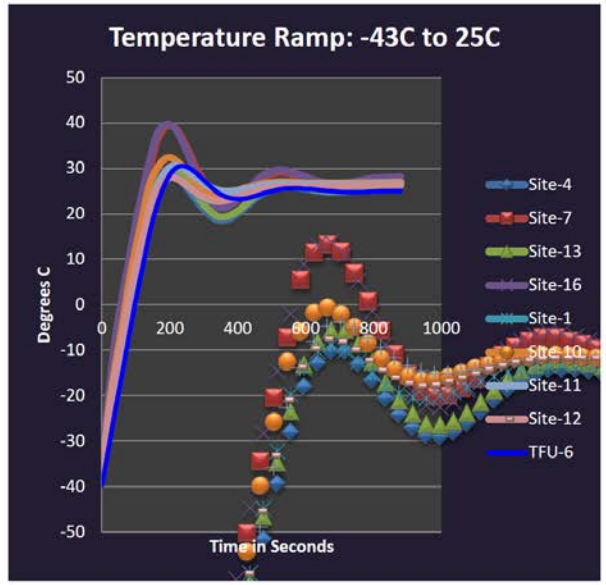
2

Room to Low Temperature Characterization Plots

Ramp Temperature for Corner and Center Sites: 25C to -43C



Temperature Ramp for Corner and Center Sites: -43C to 25C



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Temperature Testing

3

Summary

- Site temperature distribution was within a 6c window for all sites at all temperatures measured within 15 minute time window with the following observations:
  - Corner sites 4 and 13 for the 25C to 85C ramp contributed to wider temp distribution.
  - Corner sites 4 and 13 for the 25C to -43C ramp contributed to wider temp distribution.
  - In both cases, sites 4 and 13 had not reached final temperature within 15 minute window.
  - Temperature ranges for all sites and all cases were within +/- 3C of the temperature measured by the thermostream after 15 minutes.
  - Additional soak times would further narrow the overall site to site tolerance
- Overall, temperature uniformity is good.
- Internal sites reach temperature faster than corner sites.
- Placing thermocouple on an internal site is best location based on data.
- Soak time to guarantee proper test temperatures:
  - 25C to 88C: 12 Minutes Ramp Time (min) plus 5 Minutes Soak Time.
  - 25C to -43C: 14 Minutes Ramp Time (min) plus 5 Minutes Soak Time.
  - -43C to 88C: 17 Minutes Ramp Time (min) plus 5 Minutes Soak Time. (Pleliminary)

INTEGRA TECHNOLOGIES

Temperature Testing

4

Recommendations

- Place Thermocouple at any of 4 interior sites for Thermostream control
- In the test program for 25C to -43C, place 19 minute delay after Thermostream starts ramp before test begins.
  - Place a 14 minute wait time in the test program after thermostream start.
  - Check to see if thermostream is at temperature and continue is yes.
  - Wait 5 additional minutes for soak.
  - Begin device test.
- In the test program for -43C to 88C (Preliminary), place a 22 minute delay after Thermostream starts ramp before test begins.
  - Place a 17 minute wait time in the test program after thermostream starts.
  - Check to see if thermostream is at temperature and continue is yes.
  - Wait 5 additional minutes for soak.
  - Begin device test.
- In the test program for any temperature to 25C, place a 12 minute delay after Thermostream starts ramp. Wait 5 additional minutes for soak.

INTEGRA TECHNOLOGIES

Questions?

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Thank you from the Employee Owners of Integra Technologies!!