Testing of Complex FPGAs, Memorys and Microprocessors

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Celebrating Over 35 Years of Providing High Quality Semiconductor Services

NASA NEPP Workshop - June 18, 2020
1. What do AC, DC and Functional Testing Mean

2. Advanced Microprocessors / FPGA / Memory
   1. AC/DC and Functional Testing
   2. Device bus cycle timing implementation in ATE environment
   3. Development of ATE based software
   4. Compiled device assembly language loaded to the device
   5. Testing independent of manufacturer proprietary test methods
   6. Tools of testing
   7. How to develop the test vectors and configuration vectors
   8. DDR /DDR2 /DDR3 / DDR4 SDRAM, SSRAM QDR testing protocols
   9. NAND Flash testing protocols
   10. Data Retention and Endurance protocols

3. Temperature Testing
Let Us Talk Basics

What does AC / DC / Functional Testing Mean
What is DC Testing?

DC testing only covers the circuitry enclosed in the yellow square:
- Essentially the first few transistors of each pin of the device.

Bond wires to the lead frame and then to the external device pins.
What is DC Testing?

The yellow portion is an estimate of the circuitry that might be tested by DC only testing.

What can typical DC testing tell you?

- Electrical Over Stress (EOS) or Electro Static Discharge (ESD).
- If a pin is damaged, but not failing (indicated by higher than normal leakage current).
- IDD power supply current failures.
What is AC Testing?

Example AC Parametric Table From Data Sheet:

Source: Microchip FlashFlex MCU Datasheet, 02/13
There may be several 100’s or 1000’s of paths through a device that are represented by a single AC parameter. Each path needs to be evaluated to determine if they all work.

In this case there are 3 paths from Input A to Output B. Path 3 is clearly the longest and is likely the worst case propagation delay path for this AC parameter.
AC testing will tell you the speed at which things happen in the device like:

- How long does it take to access an address (access time).
- How long does it take for one signal occur after another (prop. delay).
- Maximum operating frequency.
- Signal rise and fall times.

But AC testing by itself, while better than just DC testing, still only tests a small percentage of the die at any one time.
What is Functional Testing?

Functional testing is making sure that all of the functions that a device can perform are exercised.

Ironically it is usually the area of the device that is the least explained in the datasheet.

The development of the functional test area of a complex parts accounts for 50% to 90% of the overall test development effort and cost.
Functional testing requires that each functional block in a device be thoroughly tested.

This is where up to 90% of the test development effort lies when doing a complex part.

Each white named area is a functional block for this device.
What is Functional Testing?

For a full coverage test plan; we need each of the 16 functional blocks in this device.

This can make functional testing very time consuming and very expensive.

What can happen if all functional blocks are not tested? Test escape!
Example Block Diagram and pin-out for a legacy 8051 device.

Figure 1: Functional Block Diagram
### Test Development Cost Example

<table>
<thead>
<tr>
<th>Test Development Activities</th>
<th>Engineering Hours</th>
<th>Tester Hours</th>
<th>Cost*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Specification Development</td>
<td>20</td>
<td>0</td>
<td>$3,000</td>
</tr>
<tr>
<td>Test System Selection/Speed</td>
<td>3</td>
<td>0</td>
<td>$450</td>
</tr>
<tr>
<td>Load Board Design &amp; Fabrication</td>
<td>20</td>
<td>5</td>
<td>$3,750</td>
</tr>
<tr>
<td>DC Tests</td>
<td>25</td>
<td>20</td>
<td>$6,750</td>
</tr>
<tr>
<td>Functional Test - MIN/Max Voltages</td>
<td>10</td>
<td>5</td>
<td>$2,250</td>
</tr>
<tr>
<td>Functional Test - Timing Sets</td>
<td>15</td>
<td>10</td>
<td>$3,750</td>
</tr>
<tr>
<td>Functional Test - CPU Core</td>
<td>120</td>
<td>80</td>
<td>$30,000</td>
</tr>
<tr>
<td>Functional Test - Interrupt Control</td>
<td>30</td>
<td>20</td>
<td>$7,500</td>
</tr>
<tr>
<td>Functional Test - Watchdog Timer</td>
<td>20</td>
<td>15</td>
<td>$5,250</td>
</tr>
<tr>
<td>Functional Test - Flash Control Unit</td>
<td>10</td>
<td>7</td>
<td>$2,550</td>
</tr>
<tr>
<td>Functional Test - SuperFlash</td>
<td>10</td>
<td>7</td>
<td>$2,550</td>
</tr>
<tr>
<td>Functional Test - Ram</td>
<td>10</td>
<td>7</td>
<td>$2,550</td>
</tr>
<tr>
<td>Functional Test - Security Lock</td>
<td>15</td>
<td>10</td>
<td>$3,750</td>
</tr>
<tr>
<td>Functional Test - I/O Ports</td>
<td>25</td>
<td>17</td>
<td>$6,300</td>
</tr>
<tr>
<td>Functional Test - Timers</td>
<td>25</td>
<td>20</td>
<td>$6,750</td>
</tr>
<tr>
<td>Functional Test - SPI Bus</td>
<td>15</td>
<td>10</td>
<td>$3,750</td>
</tr>
<tr>
<td>Functional Test - UART</td>
<td>40</td>
<td>30</td>
<td>$10,500</td>
</tr>
<tr>
<td>AC Tests</td>
<td>60</td>
<td>40</td>
<td>$15,000</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>473</strong></td>
<td><strong>303</strong></td>
<td><strong>$116,400</strong></td>
</tr>
</tbody>
</table>

* Assumes $150/hr for Engineering time and tester time

* Figures for discussion purposes only - not an actual quotation.

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**This is how your test lab should be quoting your project.**

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**Comprehensive Test Program Development Quotation Example**
How Can Test Development Costs be Saved?

Since the manufacturer has already thoroughly tested the devices as a part of their original manufacturing flow, the developer is able to limit the counterfeit device testing to match only the actual application conditions.

- Use actual application speeds.
- Use actual application programing code (uP and memory).
- Use actual application designs (FPGA).
- Test only functional blocks actually used in the application.
- Test only the AC parameters that are critical to the application.
- Leverage test programs already developed for the same or similar parts.
- Use device emulators.
- Use golden devices to “learn” device functionality.
Testing of Complex Microprocessors, Memories and FPGA
Integra’s Microprocessor Testing Experience

Test Engineering Experience

- Integra has developed more than 100 test programs for Processors
- Independent generation techniques without manufacturer support
- 4 engineers with processor development experience

Device Experience

- Intel Family 186, 286, 386, 486, Pentium
- Free scale/Motorola Family 68000 to 68040, Power PC and P2020
- Other Manufacturers such as PMC RM7965, TI TMS320C Family

Examples of Programs Include:

- P2020NXE2HHC
- MPC603RRX266TC
- A8050266-133SY022
- RM7965-835T
- TMS320C6713BGDPA200
- ADSP2181BSZ133QM5326
Test Development of Free scale P2020 Microprocessor

- Comprehensive Test Coverage – All Integra Generated Patterns
- 3 Engineers 1400 Engineering Hours - Test Program Development From Scratch
- Completed in Less Than 24 Weeks

<table>
<thead>
<tr>
<th>Test Coverage</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuity</td>
<td>Verify device connectivity</td>
</tr>
<tr>
<td>POR</td>
<td>Power On Reset and initialize through the eSPI bus</td>
</tr>
<tr>
<td>1st Instruction</td>
<td>1st CPU instruction cycle using eLB and instruction formatting. Part configured for 133Mhz Sysclk, 4:1 ratio for 533 CCB clock and then 1.5:1 ratio for 800MHz eCORE clock.</td>
</tr>
<tr>
<td>Dual CPU</td>
<td>Sample math and move instructions for both CPUs using local bus</td>
</tr>
<tr>
<td>eLB</td>
<td>The Local Bus will be used for all register read &amp; writes so it will be tested during all blocks. Will test all DC parameters, CLOCK to out, CLOCK to data valid, CLOCK to address valid and CLOCK to LALE assertion</td>
</tr>
<tr>
<td>UART</td>
<td>Set all registers to send and receive data on both UARTs using transceiver holding register and receiver buffer register. All DC and max baud rate for AC.</td>
</tr>
<tr>
<td>eSPI</td>
<td>Set all registers to send and receive data using FIFO for all chip selects. All DC and Master Data out delay for AC</td>
</tr>
<tr>
<td>I2C</td>
<td>Set registers for basic data transfer. All DC except pulse spike. Max clock frequency for AC</td>
</tr>
<tr>
<td>DDR3</td>
<td>Enable DDR interface configured for DDR3. AC parametric testing (6) parameters listed below. No DC parametric. Will do some data transfers at 800Mhz. 2.7.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications MCK[n] cycle time IMCK (min)2.5 ns (max)5 ns ADDRCMD output setup with respect to MCK IDDKHAS 600 Mbps data rate (Min) 0.767 ns ADDRCMD output hold with respect to MCK IDDKHAX 800 Mbps data rate (Min) 0.767 ns MCS[n] output setup with respect to MCK IDDKHCS 800 Mbps data rate (Min) 0.767 ns MCS[n] output hold with respect to MCK IDDKHCX 800 Mbps data rate (Min) 0.767 ns MCK to MDQS Skew IDDKHMH 800 Mbps data rate (min)–0.525 ns (max) 0.525 ns</td>
</tr>
<tr>
<td>Ethernet</td>
<td>Verify Ethernet functionality</td>
</tr>
<tr>
<td>MMU, L2</td>
<td>Exercise L2 Cache. Assure FPU instructions are tested. Verify MMU mapping from effective addressing to physical addressing</td>
</tr>
<tr>
<td>Cache and FPU</td>
<td></td>
</tr>
</tbody>
</table>
Traditional Test Vector Generation Method

- Device Design Environment
- Modeling Integrated with Design
- Simulation to Generate Test Patterns
  - BIST / SCAN Functional
- Simulation Patterns Converted to Tester Patterns
- Final Test Generated
How to Develop Microprocessor Vectors

Must Fully Understand the Device
- Testers work on time cycles / implement timing model into tester

Build a Microprocessor Development System

Use a Known Good Device
- Hardware simulator is the known good die
- Tester load board and tester resources are the hardware

On Tester Build a Software Model of the Device Interface
- Device bus cycle timing implemented in tester
- Developed tester s/w monitors device operation and pin status
- Compiled device assembly language loaded to the device
- The device is operating functionally just as it would in an application

Tester Records the Device Operation
- Saved as a test vector file
## Special Tester Requirements

<table>
<thead>
<tr>
<th>Tester Algorithmically Writes Vectors on the Fly</th>
<th>Rewrite Vectors in Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Software routine in the tester reviews each vector</td>
<td>• Pass fail pin register allows on-the-fly changes</td>
</tr>
<tr>
<td>• Next vector is generated according to the device protocol</td>
<td>• Test vector is corrected</td>
</tr>
<tr>
<td>• Validity of results must be analyzed by engineer</td>
<td>• Executable vector code results</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tester Register Stores State of Pass/Fail</th>
<th>Incremental Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Typically non-user tester registers are required</td>
<td>• S/W loops executable vectors to correct and add additional vectors</td>
</tr>
<tr>
<td>• Tester hardware manuals are consulted</td>
<td>• At completion corrected/generated vectors are saved</td>
</tr>
</tbody>
</table>
Vector by Vector Generation

Process

- Input to the program is assembled code
- First word of code is converted to binary and applied to input pins
- Control pins are monitored to determine the type of bus cycle (read/write)
- Continue clocking, recording the outputs until the end of that bus cycle
- Read the next word of assembled code and repeat
- Stop when no more input code
- Save memory to file
- Added test methods
- Memory testing
  - Algorithmic Pattern Generation
  - Checkerboard / Invers checkerboard
  - March Patterns
- High Speed BUS testing
  - Loop Back methods high speed serial buses
Test Generation

Vectors

0010HLHL
0000LLLL
0101HLHL
1010XXLH

Learn routine

if s = 2 then
if rw = read then
data = FFFF

Known Good DUT

R/W
ADDR
DATA
CLOCK

Diagnostic

move.l #5555, #AAAA
lsl.l #1, D0
bcc #02
Recommended Test Methodology

Test the Device the Specified Performance Characteristics

- Functional at-speed
  - Application speed at a minimum may not need spec speed
  - Test frequency is a major tester cost driver

- Comprehensive functional testing
  - Test all device functionality
  - Fault grading is not possible
    Only the manufacturer has device modeling capability

- Test key AC parameters
  - Key parameters are usually referenced to device clocks
    Propagation delay
    Setup and hold times
  - Use go-no-go testing to cover most AC parameters
    Tested over the entire functional pattern
  - Selected AC characterization measurements can be made

- DC measurements to the full specified limits
  - Attempt to test 25C parameters at extended temperatures
  - Limit adjustments may be required after testing

- Select the appropriate tester
  - No one tester can effectively test all technologies
FPGA Development Experience

Over-All

- Integra engineers have developed over 300 test programs for FPGAs
  - Xilinx
  - Intel (Altera)
  - Microchip (Microsemi)
- 150+ FPGA test programs have been developed
- Design software and testing methodologies are in place for all FPGA families
- Integra has an experienced and trained staff in place
  - 5 engineers with FPGA test development experience
  - Multiple projects using Xilinx Vivado Design Suite (ISE)

Xilinx: Examples of Programs Include

- Various Iterations of Virtex 7
  - XC4VFX20-10FFG672C
  - XC6VLX75T-3FF484C
  - XC6SLX45-L1CSG324I
- Various Iteration of Virtex 5
  - XC4VFX100-11FF1152C
  - XQ2VP40-5FF1152N
FPGA Test Methodology

Integra Implements Designs into the FPGA to Support Functional and Parametric Testing

- Test develops independent of manufacturer proprietary test methods
- Integra uses in-house tools from the manufacturer
- Create the test vectors and configuration vectors for the 93K tester
- Functional at-speed testing (using design modeling not datasheet)
  - Datasheet AC specs are internal FPGA performance characteristics
  - AC parameter tests will be generated from Xilinx software simulations
- Designs implementation includes comprehensive DC parameters
- Develop functional vectors verifies design and device functionality
FPGA Test Methodology

Testing to the User Configuration is Also an Effective Test Method

- Functional evaluation to actual application design
- Development of test vectors to user application
- Critical timing parameters testable to the application requirements
- Characterization of device performance to application is possible
Electrical Test of Today’s Complex COTs Memory Devices

Not All Manufacturers’ Products Created Equal

Figure 1: defect removal hierarchy pyramid

Lowest MTBF
Margin Tests
D/R, Stress Tests
Burn-In Infant Mortality
Package Gross Functional Tests
Package, D/C, Contv, Levels Fails
Probe Gross Func, D/C, Contv, Levels

Smallest defects most difficult to screen-out
Largest Defects easiest to screen-out
Memory Test Complexities

- **Volatile Memory**
  - Topological addressing is preferred for all types of RAM memories (proprietary to OEM but covered under NDA)
    - Can’t do silicon memory array F/A without this info
    - OEM tests 100% topologically where Row/Column/Block addressed is accomplished from Physical standpoint for best adjacent cell disturb testing in conjunction with Margin testing
  - DRAMS: FPM, EDO, VRAM, SDRAM, QDR, DDR, DDR2, DDR3, DDR4 .....
    - TREF(Refresh) parameter always an issue for full Mil-Temp of -55C to 125C, usually ¼ of commercial spec used as TREF halves every 10-12C after 70C. Or user takes yield hit
    - For Mil-Aero use, staying away from the ‘just released’ versions (i.e. Die technology shrinks, new fab process, leading edge devices) is good policy
      - Fab process maturity is key Reliability variable so unless you like looking over the edge of cliff’s, best to wait 1-yr for process maturity.
      - Request CZ-Data from Commercial Mfg-er, lots of good data nuggets even if only 0-70C, most will do extended Temp CZ of typ -40C to +85C, the more Elite companies like Micron, Samsung, Cypress & TI will do -55C to 125C.
      - If enough volume, parallel site testing preferred like 4-site for lower costs and faster turn at test.
    - Speed is no issue, we can adjust our speed license on the tester as needed up to 3600Mbps.
  - SRAMS: Async, Sync, QDR, Serial, NVRAM, Ultra Low Power, MRAM, FRAM, ReRAM, .......
    - ‘Cold Start Power-UP’: Ask yourself this question, what power up time assumption is used by the system designer? This is one parameters not normally specified in SRAM datasheet
    - DRAM does a good job of outlining this sequence But SRAM not so good. 10ms would be assumed but I have seen small % of parts not meet this, becomes yield liability
    - ATD (Address Transition Detection) special algorithm needed to target worst case scenario of single address line change that forms the access pulse edges.
      - To catch race conditions on too fast process material
    - Ground bounce affects: this as much about the load board design and decoupling as the output switching rates. The >FFFF to >0000 output switch can be disaster on poor load board design.
    - CMOS Std-by as shown on the opening slide & Weak bit algorithms like specialized Gal-Pat.
    - Still see occasional 4T-2R SRAM cell, in which properly testing Data Retention at cold temp is paramount.
Common Reasons for Testing Memory Devices

Shrinking package sizes means higher densities which translates to increased risk of being affected by even small defects in the manufacturing or assembly processes.

- Activation of unwanted particulate may not be detected without screening at extended temperature.
- Electrical test at application usage condition temperatures can identify potential reliability issues not seen by the OCM at the temperatures used for production testing.

What are the signatures of potential reliability concerns?

- Outlier /atypical standby (quiescent) supply current readings.
- Weak bits that exhibit instabilities at extended temperature or during functional tests that are known to highlight vulnerabilities for a particular type of memory device.
- Cold start issues, especially with DRAM and fast SRAM devices.
- Refresh issues with DRAM devices at elevated temperature.
Memorys - Device Specific Functional Tests

- **SRAM**
  - Data retention tests.
  - Write / Read all 1’s, all 0’s, checker board and inverse checkerboard patterns.
- **Flash**
  - Pseudo Random pattern and it’s inverse
- **EEPROM**
  - Checkerboard & Inverse Checkerboard
- **DRAM**
  - March X

In all cases referenced above, critical timing characteristics are validated by using them as setup parameters for the functional test.
NAND Flash Program/Erase Cycling Endurance & Data Retention

- **Cycling Endurance** defined as the capability to perform to specification if the number of P/E cycles are within the datasheet specification. Typically between 50K to 100K cycles. Certain number of Bad Blocks are allowable which is the NVB(number of valid blocks) min spec.

- **Data Retention (D/R)** defined as is the capability of retaining stored data, in unbiased condition over time; typically 10 years.
  - Note that D/R time for cycled devices decreases as P/E cycle number is increased. See chart below

- **SLC NAND Flash cell** is predominantly the choice of MILAERO users due to more robust threshold voltage margins on the cell state versus MLC.
  - Additional design mitigation by the user to achieve Longer D/R would be in the form of wear leveling, data refresh, & stronger ECC.
  - **JEDEC Recommended Standards to consider when designing Qual/Reliability Exercise for Endurance/Data Retention**
    - JESD47K “Stress-Test-Driven Qualification of Integrated Circuits”
    - JESD94A “Application Specific Qualification Using Knowledge Based Test Methodology”
    - JEP122H “Failure Mechanism & Models for Semiconductors Devices”

- **Customer must select Conditions to be used for Endurance/Data Retention normally based on Application usage**
  - # of Pgm/Erase P/E Cycles, fraction of cells cycled to full Spec, Fraction cycled to other percentage(very important for esp large densities), Temperature of Cycling Chamber (25C, 55C or 85C?), VCC level (nom or max?), Data Pattern to be cycled, If cold temp cycling needed and what conditions, Intentional delays, ECC mgmt applied, periodic reads during endurance or every cycle, UBER value if applicable, # of devices to subjected to what stresses, Arrhenius variables for acceleration calc
## Advanced Memory Tester – Smart Scale from Advantest

<table>
<thead>
<tr>
<th>Group 7</th>
<th>Utility</th>
</tr>
</thead>
<tbody>
<tr>
<td>224:</td>
<td>220:</td>
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<tr>
<td>223:</td>
<td>219:</td>
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<td>222:</td>
<td>218:</td>
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<td>221:</td>
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<tr>
<td>232:</td>
<td>228:</td>
</tr>
<tr>
<td>231:</td>
<td>227/427: DPS128-HC</td>
</tr>
<tr>
<td>230/430: DPS128-HV</td>
<td>226:</td>
</tr>
<tr>
<td>229/429: DPS128-HV</td>
<td>225/425: DPS128-HC</td>
</tr>
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<table>
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<tr>
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<td>116: PS1600</td>
<td>112: PS1600</td>
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<td>114: PS1600</td>
<td>110: PS1600</td>
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<tr>
<td>113: PS1600</td>
<td>109: PS1600</td>
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<td>212:</td>
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<td>214:</td>
<td>210:</td>
</tr>
<tr>
<td>213:</td>
<td>209:</td>
</tr>
</tbody>
</table>

### Number of resources

- **PS1600** dig.Pin: 384
- **DPS128 HV** -6V/15V (Max current 0.2A): 64
- **DPS128 HC** -2.5V/7V (Max current 0.5A): 64
- **HV-DPS #2** +0.5V to 22V (Max current 1A): 4

**SmartTest Versions**
- soc64 7.2.3.5
- soc64 7.4.3.4

**Z640 PC w/ Red Hat Enterprise Linux 5**

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*Existing test solutions for DDR3, DDR4 are in place with system architecture upgradable to support higher speeds and higher device pin counts.*
Temperature Testing Considerations
Example of Temperature Characterization – 512 NAND Flash - BGA

Characterization Tools & Method

- Four calibrated and certified RTDs part number # HEL-705-U-1-12-C2
- Four calibrated Keithley 2402B source meters
- Threaded ferrules for holding RTDs in socket lid
- One calibrated Tempronic TP04300A Thermostream

- 8 of 16 sites were measured. The thermostream thermocouple was used in Site 6. The measured sites were the four corner and four center sites.
- Temperature was measured from 25C to 88C, 88C to 25C, 25c to -43c, and -43c to 25c; Four sites at a time.
- A program was written to sample the measurements in 20 second increments for a total duration of 15 minutes for each temperature sweep.
- Floor temperature was 22C.
- Data was taken without bias.
Temperature Testing

Room to High Temperature Characterization Plots

Ramp Temperature for Corner and Center Sites: 25C to 88C

Temperature Ramp for Corner and Center Sites: 88C to 25C

9/22/2018
16 Site Temperature Characterization
Temperature Testing

Room to Low Temperature Characterization Plots

Ramp Temperature for Corner and Center Sites: 25C to -43C

Temperature Ramp for Corner and Center Sites: -43C to 25C

9/22/2018

16 Site Temperature Characterization
Summary

- Site temperature distribution was within a 6σ window for all sites at all temperatures measured within 15 minute time window with the following observations:
  - Corner sites 4 and 13 for the 25C to 85C ramp contributed to wider temp distribution.
  - Corner sites 4 and 13 for the 25C to -43C ramp contributed to wider temp distribution.
  - In both cases, sites 4 and 13 had not reached final temperature within 15 minute window.
  - Temperature ranges for all sites and all cases were within +/- 3C of the temperature measured by the thermostream after 15 minutes.
  - Additional soak times would further narrow the overall site to site tolerance
- Overall, temperature uniformity is good.
- Internal sites reach temperature faster than corner sites.
- Placing thermocouple on an internal site is best location based on data.
- Soak time to guarantee proper test temperatures:
  - 25C to 88C: 12 Minutes Ramp Time (min) plus 5 Minutes Soak Time.
  - 25C to -43C: 14 Minutes Ramp Time (min) plus 5 Minutes Soak Time.
  - -43C to 88C: 17 Minutes Ramp Time (min) plus 5 Minutes Soak Time. (Preliminary)
Temperature Testing

Recommendations

- Place Thermocouple at any of 4 interior sites for Thermostream control
- In the test program for 25C to -43C, place 19 minute delay after Thermostream starts ramp before test begins.
  - Place a 14 minute wait time in the test program after thermostream start.
  - Check to see if thermostream is at temperature and continue is yes.
  - Wait 5 additional minutes for soak.
  - Begin device test.
- In the test program for -43C to 88C (Preliminary), place a 22 minute delay after Thermostream starts ramp before test begins.
  - Place a 17 minute wait time in the test program after thermostream starts.
  - Check to see if thermostream is at temperature and continue is yes.
  - Wait 5 additional minutes for soak.
  - Begin device test.
- In the test program for any temperature to 25C, place a 12 minute delay after Thermostream starts ramp. Wait 5 additional minutes for soak.
Questions?

Contact info:
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Sultan.Lilani@Integra-tech.com (510.830.9216)

Thank you from the Employee Owners of Integra Technologies!!