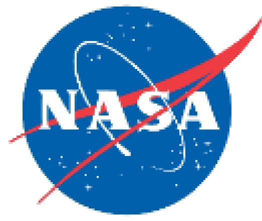

Is High Energy Heavy Ion Testing the Future for Single-Event Effects (SEE) in Devices and Systems?

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Acronyms

Three Dimensional (3D)
Atomic Mass Unit (amu)
Bump Plating Photoresist (BPR)
Complementary Field Effect Transistor (CFET)
Complementary Metal Oxide Semiconductor (CMOS)
Commercial Off The Shelf (COTS)
Chip to Wafer (CtW)
continuous wave (CW)
Dynamic Random Access Memory (DRAM)
Design Technology Co-Optimization/Synthesis Technology Co-Optimization (DTCO/STCO)
embedded Dynamic Random Access Memory (eDRAM)
Extreme Ultraviolet Lithography (EUV)
Ferroelectric Field Effect Transistor (FeFET)
Ferroelectric Random Access Memory (FeRAM)
Fully Self Aligned Via (FSAV)
Ferroelectric Tunnel Junction (FTJ)
Grand Accélérateur National d'Ions Lourds (GANIL)
GSI Helmholtz Centre for Heavy Ion Research (GSI)
High Bandwidth Memory (HBM)
Input/Output (I/O)
Integrated Circuits (ICs)
Josephson Junction (JJ)
Lawrence Berkeley National Laboratories (LBNL)
Linear Energy Transfer (LET)
Micro Three Dimensional (M3D)
Magnetic Shielding (Mag.)
Magnetoresistive Random Access Memory (MRAM)
NOT-AND (NAND)
Negative Capacitance Field-Effect Transistor (NCFET)
Nanoelectromechanical Systems (NEMS)
NASA Space Radiation Lab (NSRL)
NASA Space Radiation Laboratory (NSRL)
Phase Change Memory (PCM)
Phase Change Memory (PCM)
Redistribution Layer (RDL)
Resistive Random Access Memory (ReRAM)
Radiation Hardness Assurance (RHA)
Return on Investment (ROI)
Self-Aligned Gate Contact (SAGC)
Single Diffusion Break (SDB)
Single Event Effects (SEE)
Single Event Effect Symposium/Military and Aerospace Programmable Logic Devices Workshop (SEEMAPLD)
Single-Electron Transistor (SET)
Single Event Upset (SEU)
Super-steep Slope (SS)
Structural Simulation Toolkit (SST) Random Access Memory (RAM)
Statistical Variability (SV)
Texas A&M University (TAMU)
Tunnel Field Effect Transistor (TFET)
Through Silicon Via/Through Mold Via/Through Die Via (TSV/TMV/TDV)
Vertical Field Effect Transistor (VFET)
Wafer-To-Wafer (WTW)

Outline

- High Energy Heavy Ions and SEE
- Enabling Characteristics of High Energy Heavy Ion Facilities
- Technical Rationale for Using High Energy Heavy Ions
  - Devices – moving to 3D
  - Systems – validation
- Test Efficiency/Return on Investment (ROI)
- Caveats
- Summary

Partial List of High Energy SEE Facilities

- Currently Accessible
  - NASA Space Radiation Lab (NSRL)
  - Grand Accélérateur National d'Ions Lourds (GANIL)
  - GSI Helmholtz Centre for Heavy Ion Research (GSI)
- Extinct
  - National Superconducting Cyclotron Laboratory (NSCL)
  - Lawrence Berkeley National Laboratory (LBNL) Bevalac
  - Chalk River Tandem Accelerator Superconducting Cyclotron

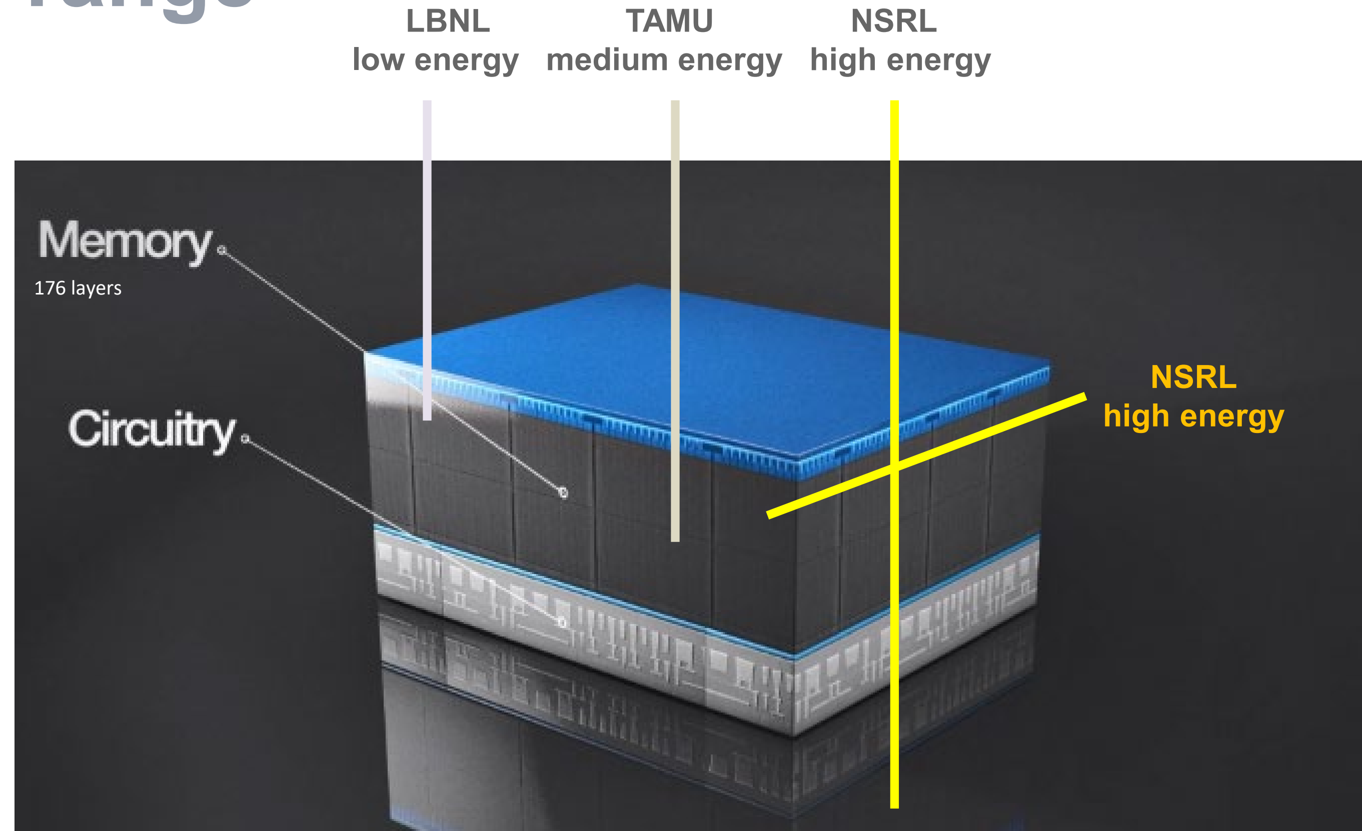
High Energy Heavy Ion SEE Testing - Background

- **Definition:** testing electronics with ions of Z=2 to 92 with kinetic energies roughly greater than 100 MeV/amu
- Testing electronics with high energy heavy ions is not new
  - Work has included the following topics
    - Ion range of penetration (energy deposition at sensitive portions of the semiconductor)
    - Angular issues (increased packaging material challenges and ion track effects)
    - Assembly/system tests (validation or gross risk evaluation)
    - Environment considerations and particle beam physics issues (accuracy and data analysis)
- This presentation focuses on some of the factors increasing the need to capitalize on high energy for SEE testing from the technical perspective with a nod to utilization
  - Evolution of electronics/semiconductor technologies
  - Increased consideration of space system test and validation

Technical Reasons to Use High Energy

- Increased penetration range of the ions
  - Ability to test 2.5/3D devices without requiring deprocessing of package/device
  - Ability to test articles at extreme angles
- Large beam irradiation area
  - Ability to test systems
  - Ability to test large batches of devices simultaneously
- Mimicking of the actual space environment

Notional ion energy and device testability-penetration range



Micron's proprietary CMOS-under-Array technique constructs the multilayered stack over the chip's logic, packing more memory into a tighter space and shrinking 176-layer NAND's die size, yielding more gigabytes per wafer.

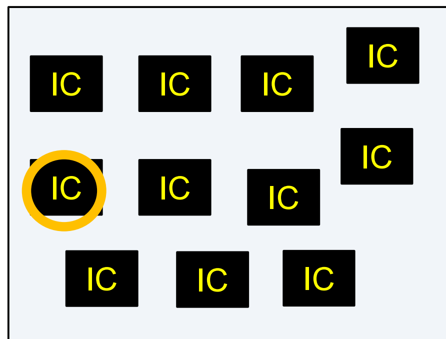
Courtesy of Micron , https://www.eetimes.com/micron-leapfrogs-to-176-layer-3d-nand-flash-memory/#

Note that non-3D devices are not disappearing from space systems and the energies at LBNL and TAMU will still be needed as well.

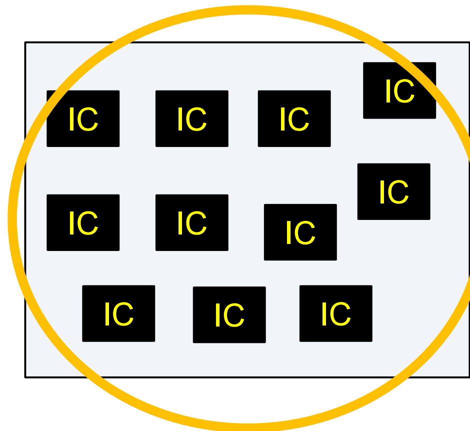
High energy ions are needed to ensure penetration to all radiation sensitive portions of modern 3D devices. These are the state-of-the art devices that have enabling properties for space applications.

Large Beam Irradiation Area - Ground rules

- Standard SEE Testing
  - Irradiate one device at a time



- Batch Device Irradiation
  - Irradiate large number of devices simultaneously

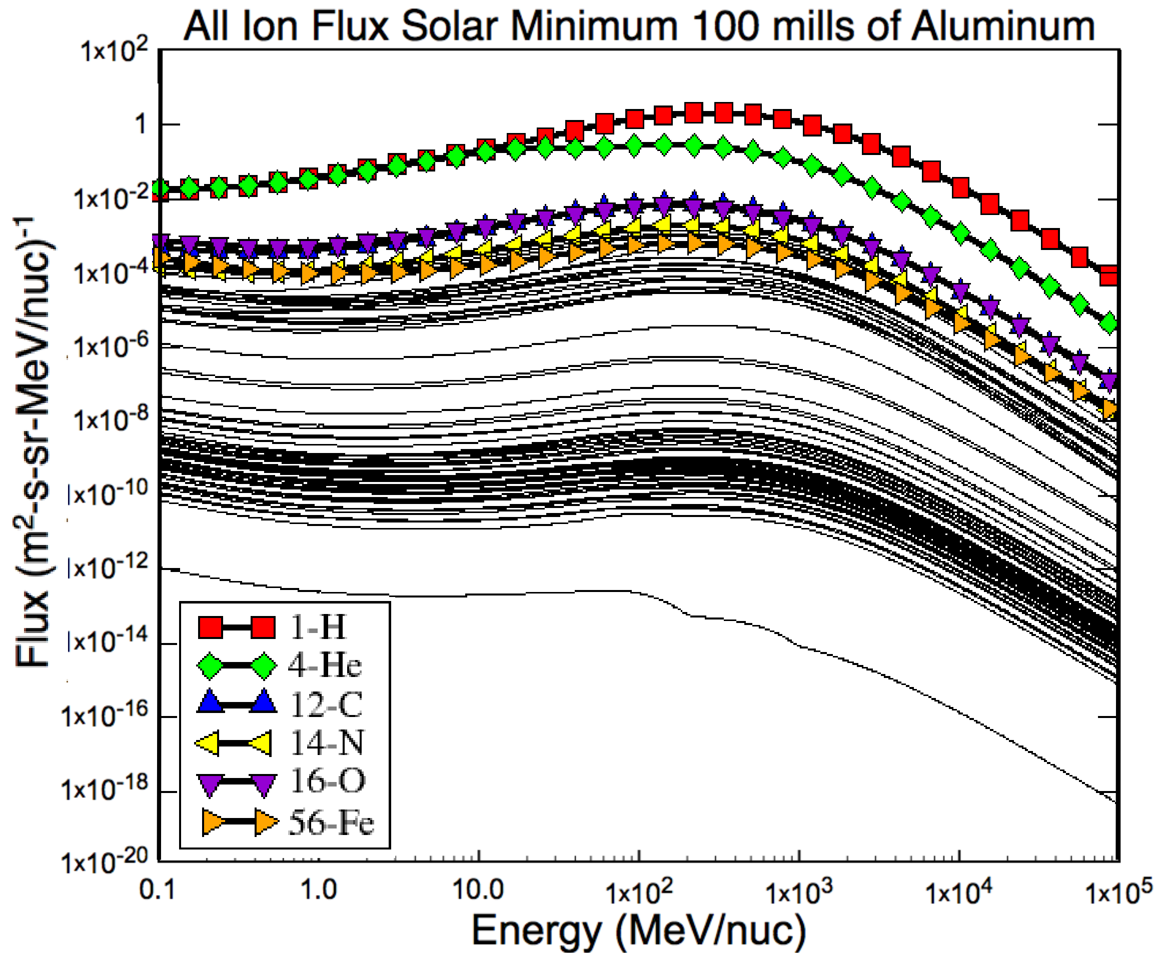


- System Irradiation
  - Irradiate entire card or system simultaneously

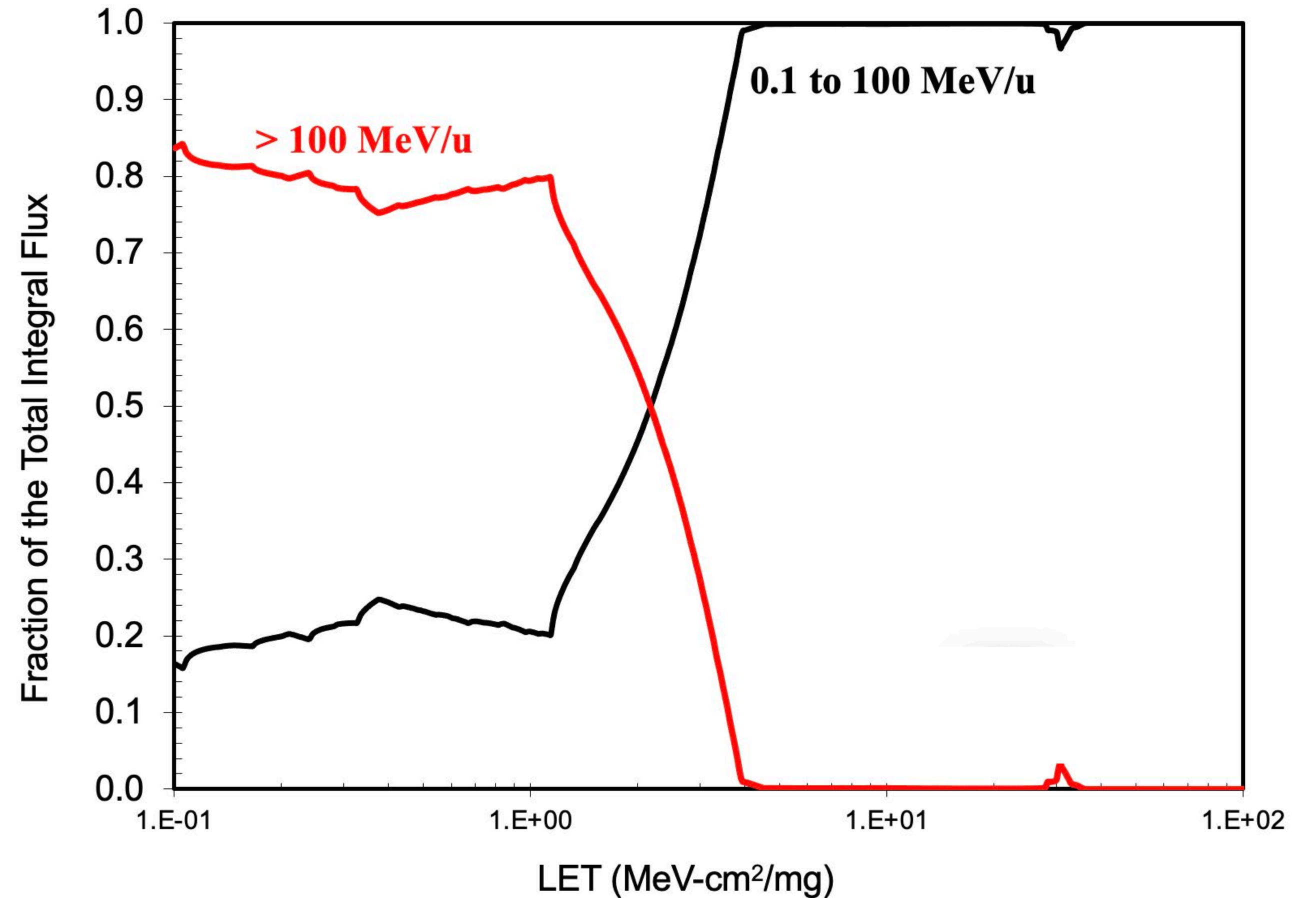
Image courtesy of Vanderbilt University

High energy allows an option for a large irradiation area due to the kinematics of the accelerator designs
- **NSRL is an example of this**

Natural Space Environment – Heavy Ion Coverage



Courtesy of Vanderbilt
https://creme.isde.vanderbilt.edu/



Typically :

- higher LETs - destructive events
- lower LETs - soft commercial devices Z

Integrate Circuits (ICs) – Evolving Technologies

- ICs and their related packaging are continuing to evolve for packing as many features in as small a space as possible
  - Device transistor geometries
  - Changing architectures and materials
  - Heterogeneous devices
  - 3D packaging

"IBM states that the technology can fit '50 billion transistors onto a chip the size of a fingernail'. IBM's press relations stated that a fingernail in this context is 150 square millimeters. That puts IBM's transistor density at **333 million transistors per square millimeter** (MTr/mm2)." - *https://www.anandtech.com/show/16656/ibm-creates-first-2nm-chip*

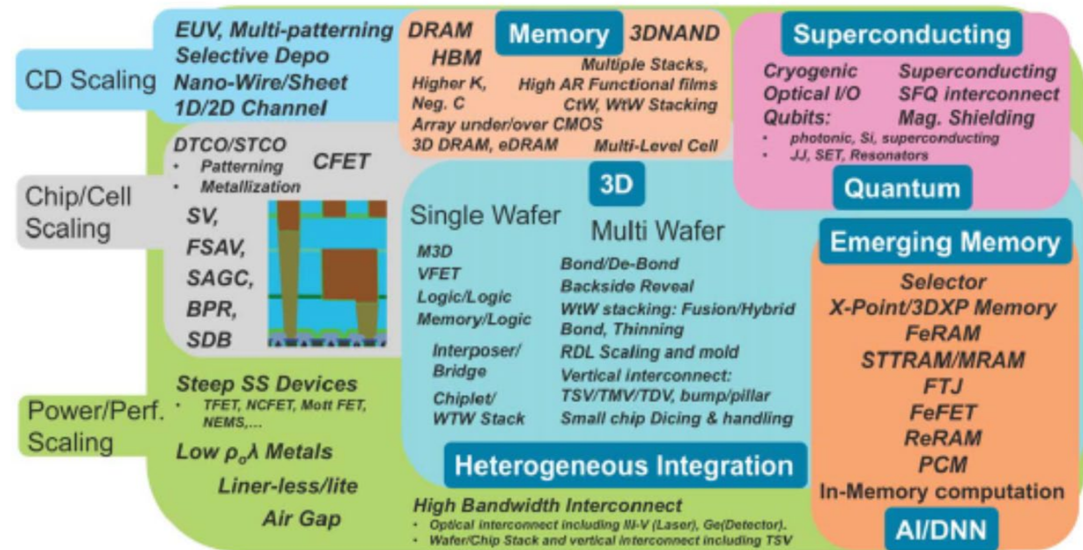
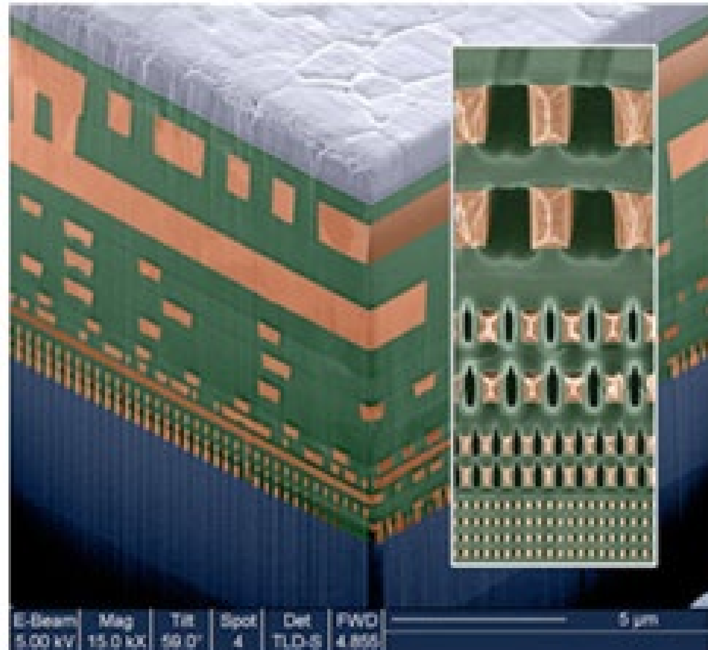


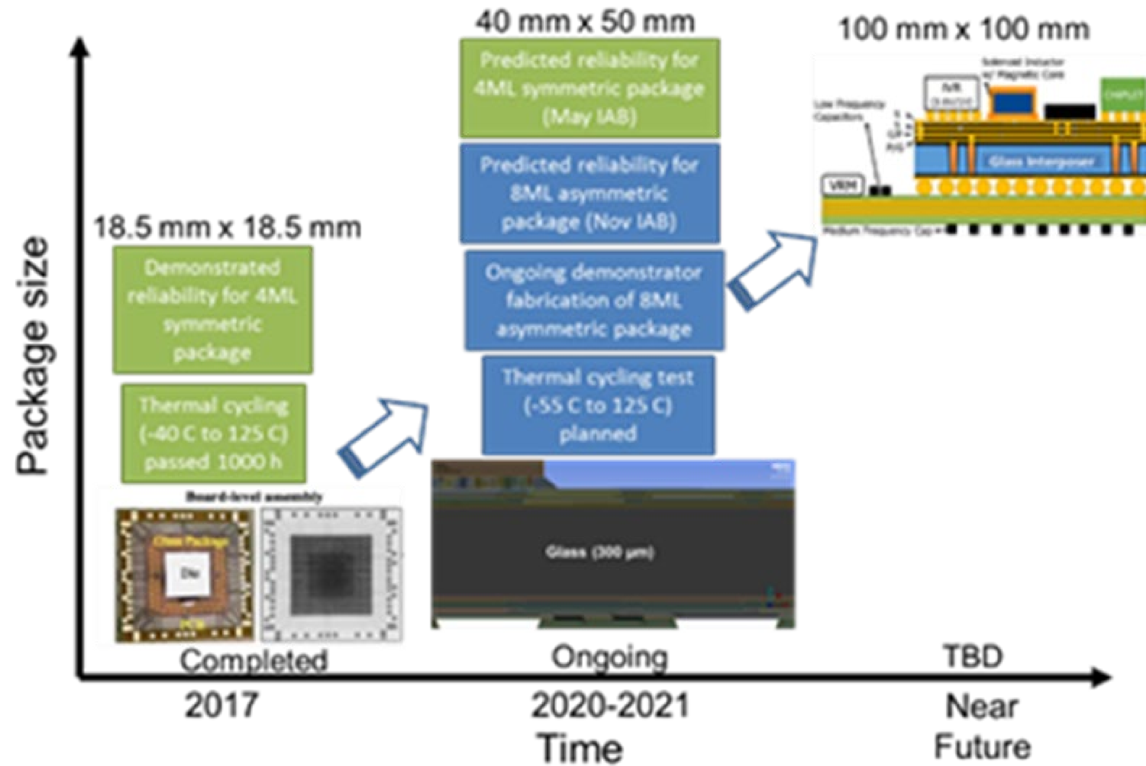
Figure 5.9: Drivers and technologies for better power, performance, area, and cost Scaling[24] (courtesy of Robert Clark, Tokyo Electron)

https://www.src.org/about/decadal-plan/ Full Report

Ions Need to Penetrate Complex Structures

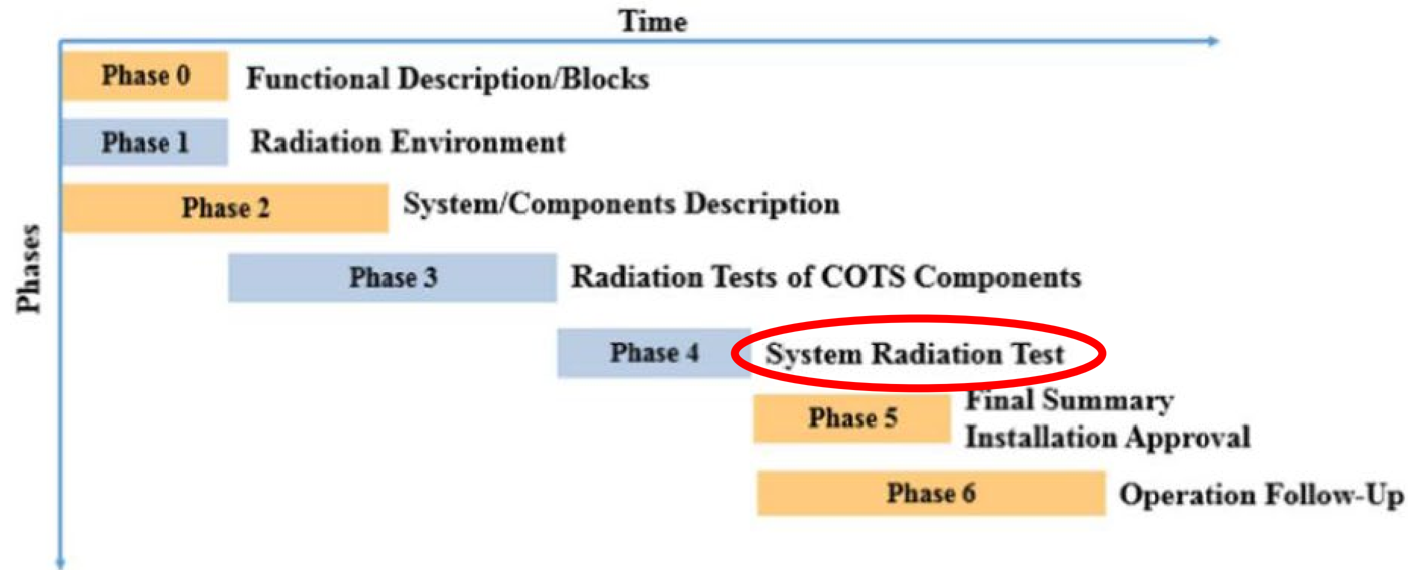


Courtesy of Daniel Fleetwood, IEEE NSREC 2020 Short Course



Courtesy of Doug Sheldon and Eric Suh, JPL

System Level Radiation Testing is Now Part of the Radiation Hardness Assurance (RHA) Process



- *Considering radiation tolerance constraints at very early stage of design*
- *Validation of radiation tolerance at system level before final production*

Courtesy of Ruben Garcia Alia, G-Rad 2020

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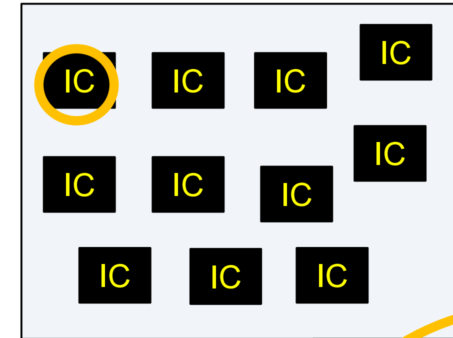
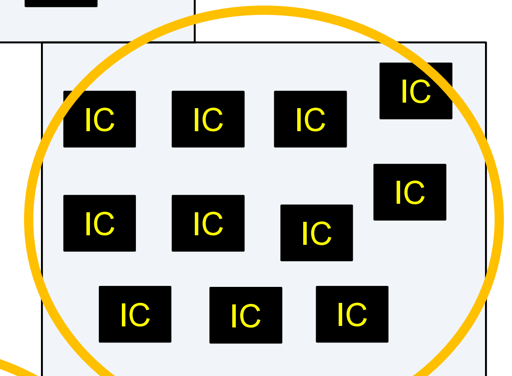
RHA for COTS is now commonplace and promulgating. ***Recommendation is always to perform radiation tasks (testing) as early as possible in a mission (or product development) lifecycle.*** ***System tests are now being included.***

SEE Test Scenarios – Return on Investment (ROI)

- Baseline: traditional IC test
- Board-level test: testing of large amounts of individual ICs on a single test board
  - 2 sub-scenarios: using traditional one part at a time irradiation, then all samples at the same time
- Board-level test: functional purpose board (e.g., space computer)
- Board-level test: SEE mitigation validation
- Assembly or stacked board test





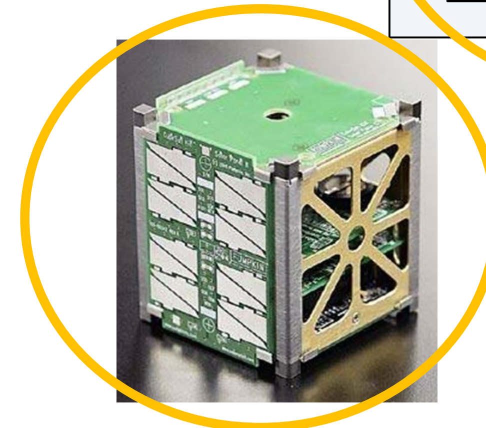


Image courtesy of Vanderbilt University

ROI Example

- At the forthcoming Single Event Effect Symposium/Military and Aerospace Programmable Logic Devices Workshop (SEEMAPLD – https://seemapld.org), a detailed presentation discussing ROI will be presented, however, here is a notional example for testing 15 parts simultaneously versus "old school"

Irradiate each device in turn	Value
# of test parts on the board	15
# of boards	1
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angle)	3
# of angles (per ion/energy)	3
Avg time per test run - min	2
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

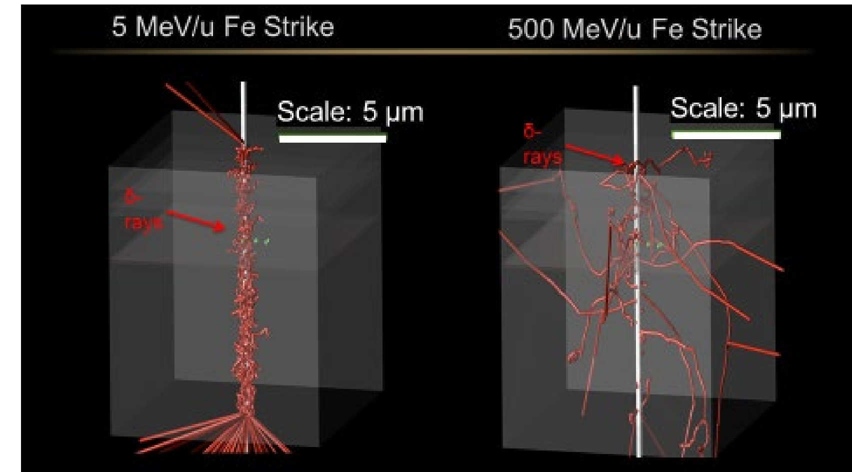
1080	# of test runs
3240	Beam run time in minutes
55.5	Total hours needed for test

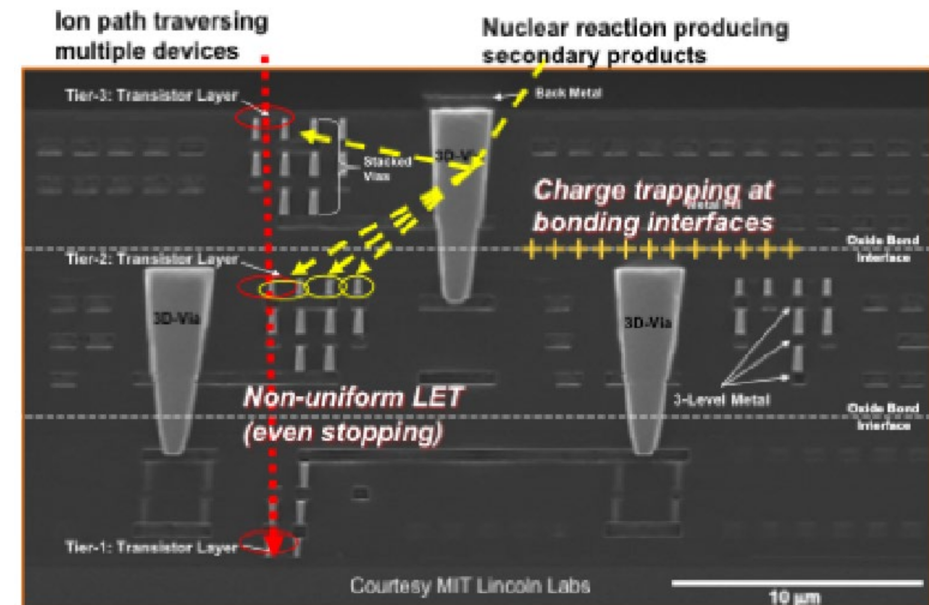
Irradiate all devices simultaneously	Value
# of test parts on the board	15
# of boards	1
# of ions	4
# of energies per ion	2
# of test runs (per ion/energy/angle)	3
# of angles (per ion/energy)	3
Avg time per test run - min	8
Avg time between test runs - min	1
Board change time in minutes	45
Ion change time - min	30

72	# of test runs
648	Beam run time in minutes
12.3	Total hours needed for test

Caveats and Challenges - Modeling

- High energy provides a wider "track"
  - As the "packing density" scales, more transistors could be affected by the track
- Linear energy transfer (LET) changes as ion transverses materials
- Nuclear reactions occur that spallate secondaries (possibly with higher LET)
- **If modeling is needed, how hard will it be to obtain the material and mechanical details required to model?**





Images courtesy of Vanderbilt University

Caveats and Challenges – Test Complications

- Test complications will vary by goal of the test being performed, but a few examples are:
  - Design of experiments for individual IC monitoring
  - Event capture fidelity for operational scenarios (i.e., event occurrence versus delay in observation and recovery)
  - “Simple” test system issues such as cabling the test board to ancillary equipment, and so on
  - Beam structure considerations (pulsed versus continuous wave (CW))

Image courtesy of NASA

Summary and Comments

- Presented herein has been a brief overview of
  - Technical advantages of using high energy heavy ions
  - The technical directions driving the need for high energy
  - ROI “teaser”
  - Sample caveats and considerations
- To be clear, the lower energy heavy ions (<50MeV/amu, for example) will still be needed for testing and research on a large number of ICs, but there are specific issues that will drive high energy (and modeling) for future heavy ion testing and research
  - Guidelines, training, and research are needed make best use of this limited resource