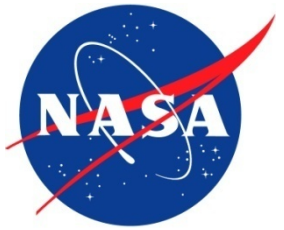
National Aeronautics
and Space Administration



Wide Bandgap Power Device Radiation Reliability

Jean-Marie Lauenstein

NASA GSFC, Greenbelt, MD, USA

Acronyms and Abbreviations

2DEG	Two-Dimensional Electron Gas
AlGaN	Aluminum Gallium Nitride
BJT	Bipolar Junction Transistor
BV_{DSS}	Drain-Source Breakdown Voltage
C	Carbon
DDD	Displacement Damage Dose
E_C	Conduction Band Energy
E_F	Fermi Level Energy
E_{gap}	Bandgap Energy
E_V	Valance Band Energy
EDMR	Electrically Detected Magnetic Resonance
FIT	Failures In Time
FOM	Figure of Merit
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GCR	Galactic Cosmic Ray
GEO	Geostationary Earth Orbit
HEMT	High Electron Mobility Transistor

I_D	Drain Current
I_{DSS}	Drain-Source Leakage Current
I_G	Gate Current
I_{GSS}	Gate-Source Leakage Current
I_R	Reverse Current
ISS	International Space Station
JBS	Junction Barrier Schottky diode
JFET	Junction Field Effect Transistor
LEO	Low Earth Orbit
LET	Linear Energy Transfer
MISFET	Metal-Insulator Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NIEL	Non-Ionizing Energy Loss
NO	Nitric Oxide
PIGS	Post-Irradiation Gate Stress
R&D	Research and Development
R_{DS_ON}	On-State Drain-Source Resistance

RF	Radio Frequency
RHA	Radiation Hardness Assurance
SBD	Schottky Barrier Diode
SEB/GR	Single-Event Burnout/Gate Rupture
SEDR	Single-Event Dielectric Rupture
SEE	Single-Event Effect
SELC	Single-Event Leakage Current
Si	Silicon
SiC	Silicon Carbide
SOA	State Of the Art; Safe Operating Area
SWaP	Size, Weight, and Power
TCAD	Technology Computer-Aided Design
TID	Total Ionizing Dose
VDMOS	Vertical Double-diffused MOSFET
V_{DS}	Drain-Source Voltage
V_{GS}	Gate-Source Voltage
V_R	Reverse-bias Voltage
V_{TH}	Gate Threshold Voltage
WBG	Wide Bandgap
Xe	Xenon

Outline

- **Overview**
  - SiC and GaN material properties
  - Inherent radiation hardness from wide bandgaps (WBGs)
- **SiC Power Device Heavy-Ion Effects & Mechanisms**
  - SiC Diodes and MOSFETs
- **GaN Power Device Heavy-Ion Effects & Mechanisms**
  - GaN High Electron Mobility Transistors (HEMTs)
    - Focus on normally-off p-GaN HEMTs
- **Radiation Hardness Assurance Challenges**
  - Test methodology
  - Rate prediction and reliability uncertainty

Single-event burnout in a SiC Schottky Diode

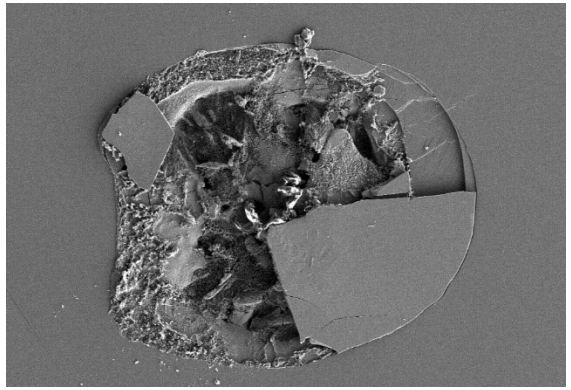
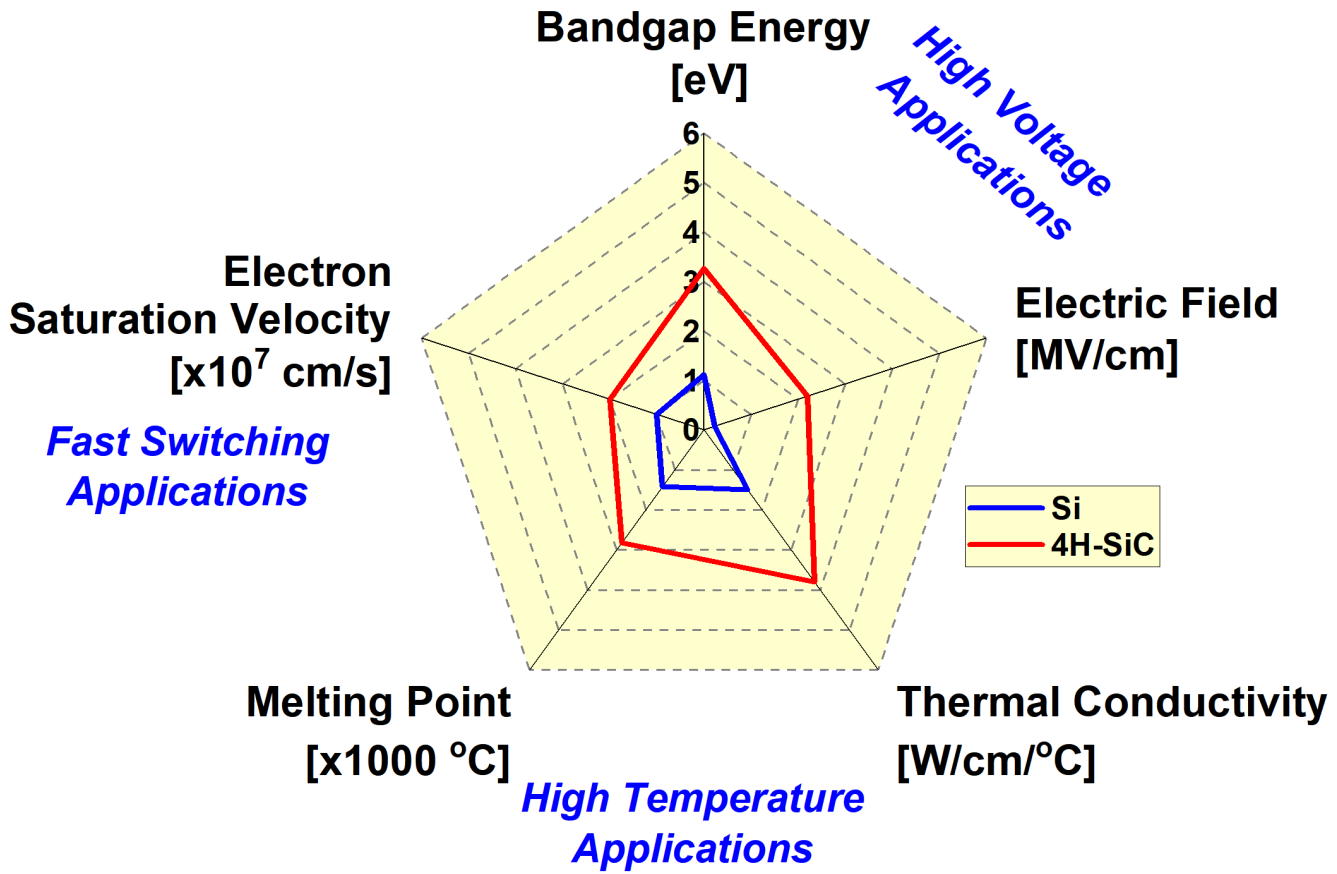


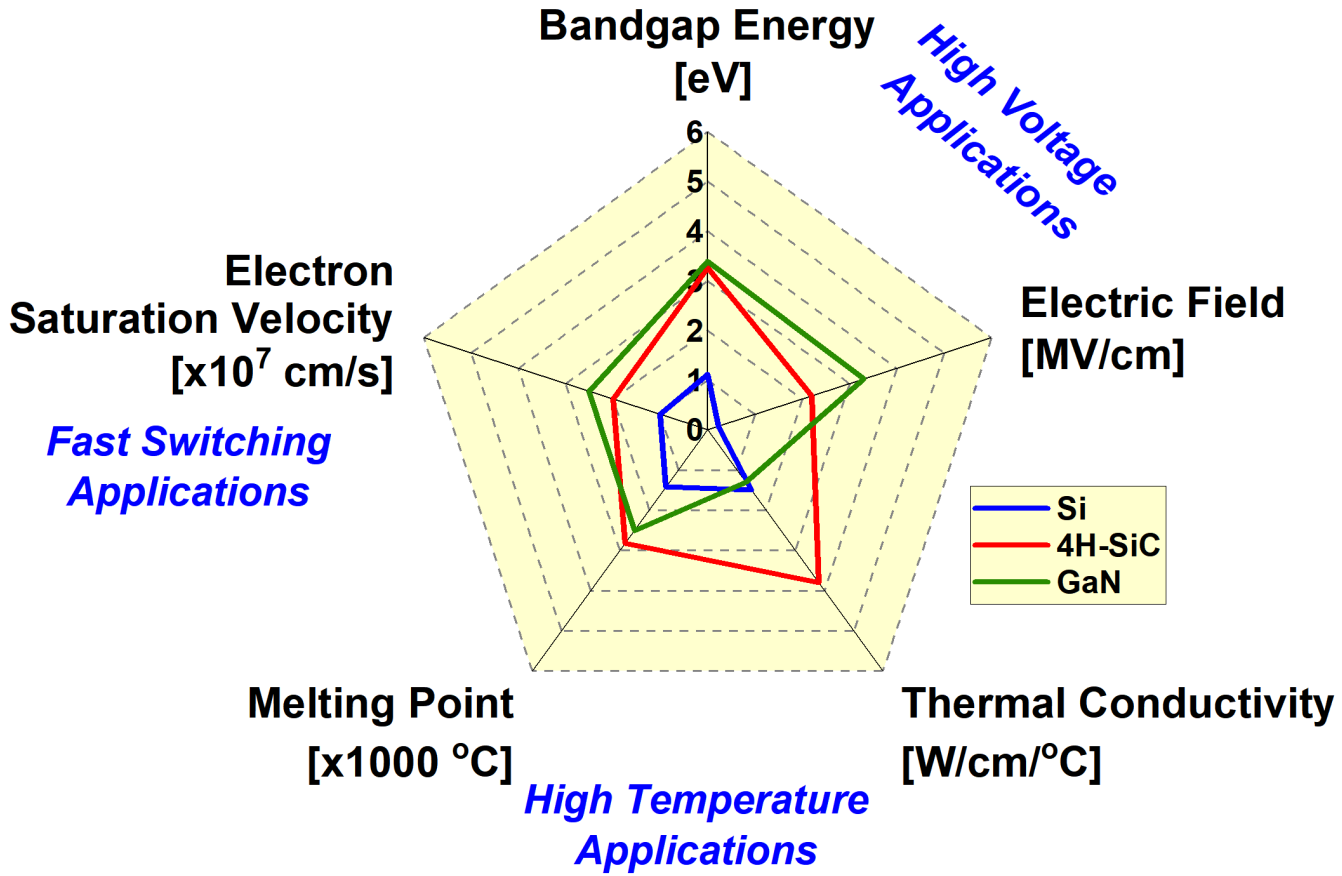
Image: A. Woodworth, NASA

SiC vs. Si Properties



SiC out-performs Si on 5 different parameters, lending itself to high-power, high-temperature, and fast-switching applications

GaN vs. SiC vs. Si Properties



To date, GaN's upper limit on voltage rating is dictated primarily by device reliability issues

Wide bandgap (WBG) Inherent Radiation Tolerance

- **“Inherent” radiation hardness of WBG semiconductors typically refers to their tolerance of total dose:**
  - Both the ionization energy and threshold energy for defect formation (atomic bond strength) exceed that for Si
  - Early WBG devices did not have gate oxides
  - Operation of WBG devices at high temperature may help alleviate dose effects

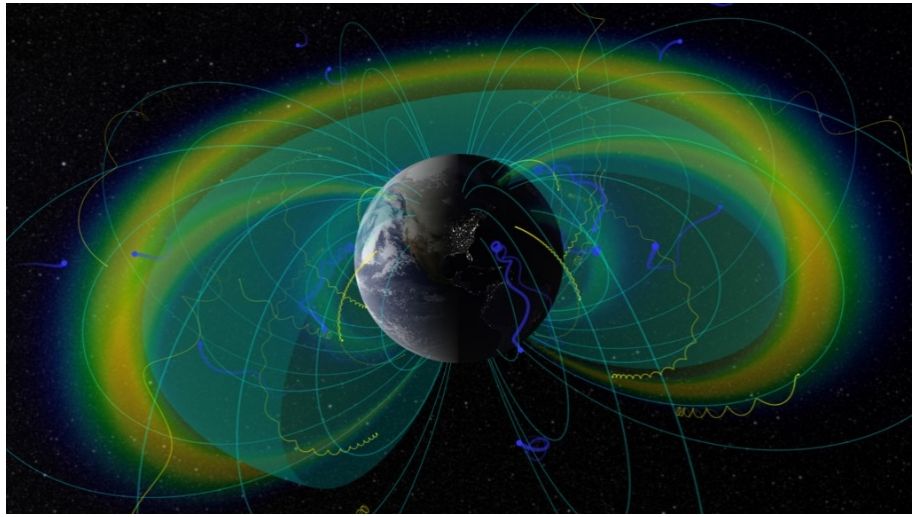


Image: NASA

WBG Achilles' Heel: Single-Event Effects (SEE)

SiC Diode

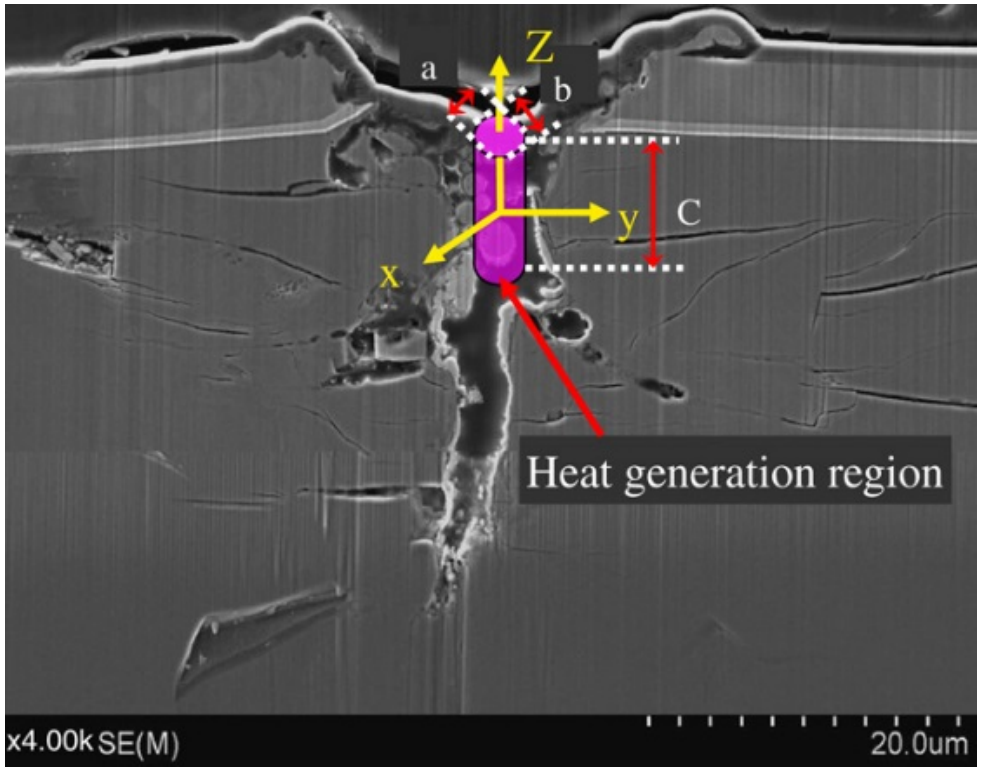


Image: Shoji, et al., © (2014) The Japan Society of Applied Physics, used with permission.

GaN HEMT

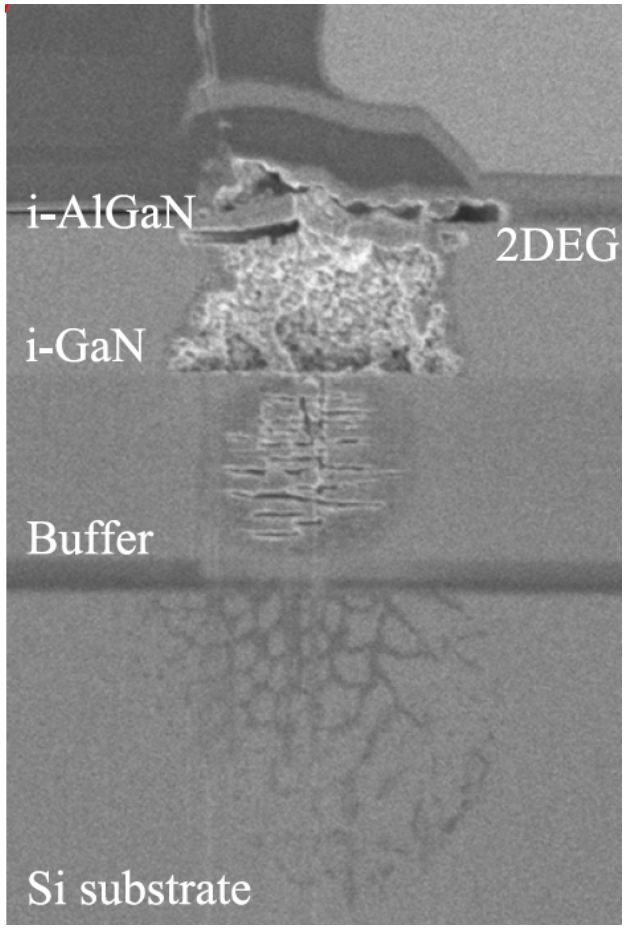
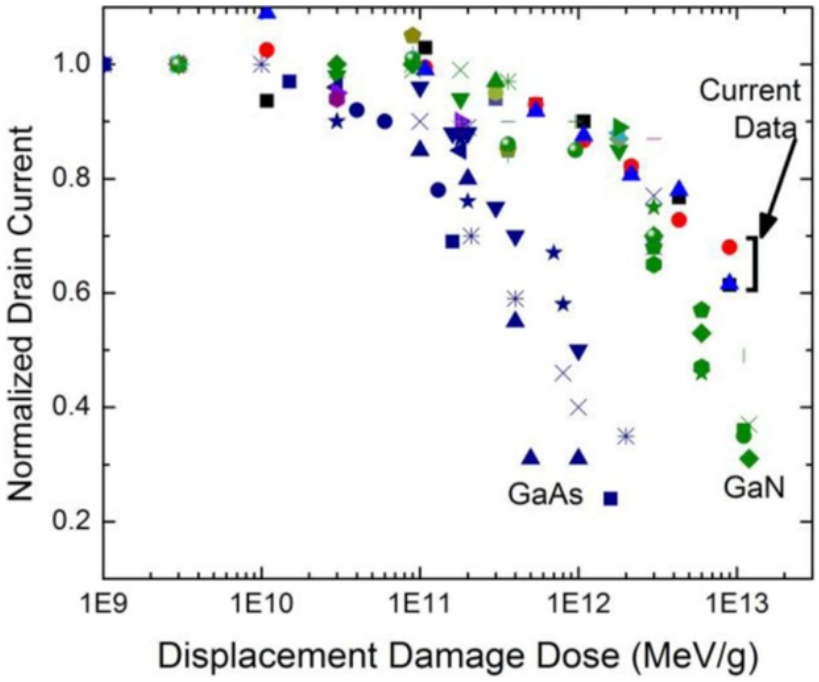


Image: Mizuta, et al., IEEE TNS 2018

Heavy-ion induced catastrophic single-event burnout in SiC and GaN power devices: Higher energy for charge ionization doesn't provide SEE immunity

Displacement Damage Dose (DDD) Effects: GaN HEMTs

GaN HEMTs out-perform GaAs HEMTs



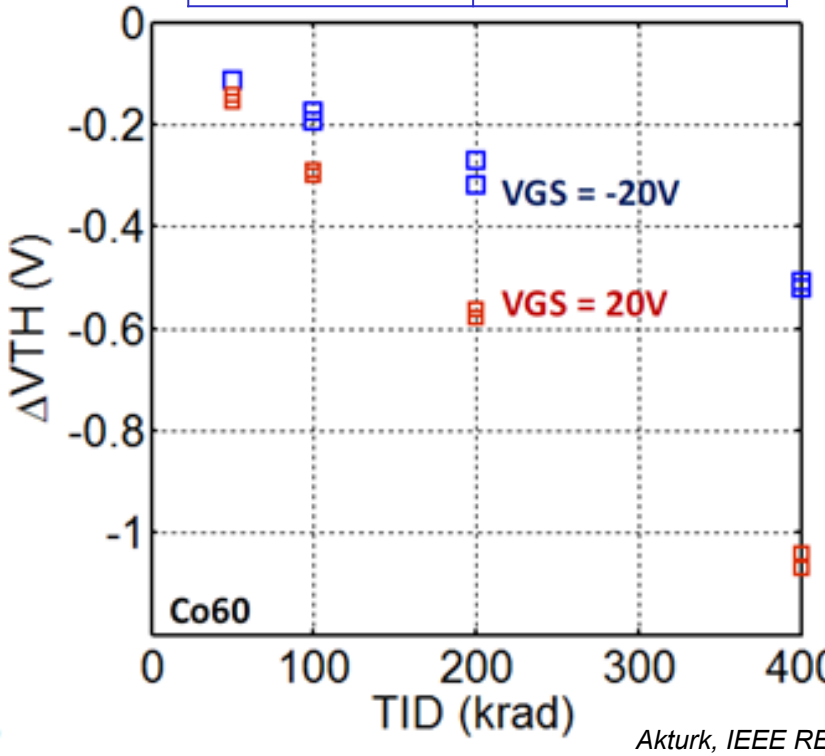
Weaver et al. ECS J. Solid State Sci. Technol. 2016. CC BY-NC-ND license.

- **Parametric degradation in GaN HEMTs occurs at DDD levels above those for typical space applications**
  - Weaver, *et al.*, 2015 show order-of-magnitude better performance of GaN vs. GaAs HEMTs
- **GaN HEMT DDD effects include**
  - Decreased drain current
  - Threshold voltage shift (typically positive)
  - Decreased mobility and transconductance
- **DDD susceptibility is greater when:**
  - **parts are biased during irradiation**
  - **parts have had prior hot-carrier stress**
    - see Chen, *et al., IEEE TNS* 2015

GaN device DDD test conditions are important

Total Ionizing Dose (TID) Effects: SiC MOSFETs

Orbit	~1-yr shielded TID [krad(Si)]
Jovian	300
GEO	150
Polar LEO	5
ISS LEO	1



Akturk, IEEE REDW, 2017

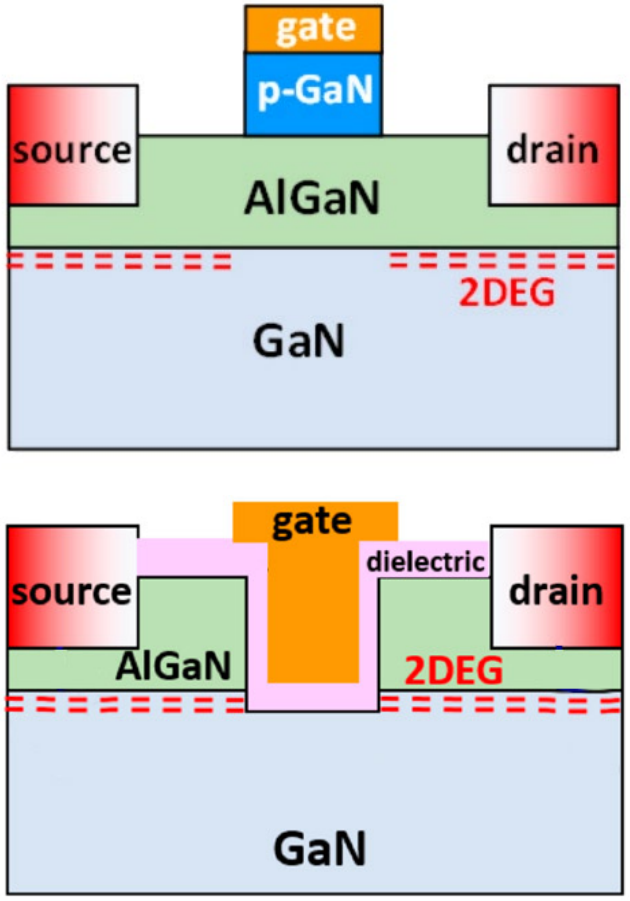
Despite thick oxides, SiC MOSFETs can be TID-robust:

- **Cree Gens 1 & 2 in spec up to 100 krad(Si)**
  - Above 300 krad(Si), significant gate-drain capacitance changes can strongly impact switching performance
- **Expect variability between manufacturers and processes**
  - Hole trapping depends strongly on NO anneal time and temperature
  - Interface state formation with radiation can vary
  - Substantial fundamental differences between radiation responses of Si and SiC MOSFETs found via electrically detected magnetic resonance (EDMR)

TID hardness is coincidental and may change

Total Ionizing Dose: GaN HEMTs

p-GaN and MISHEMT Gate Structures



Images modified from:
Roccaforte, Materials, 2019. CC BY license.

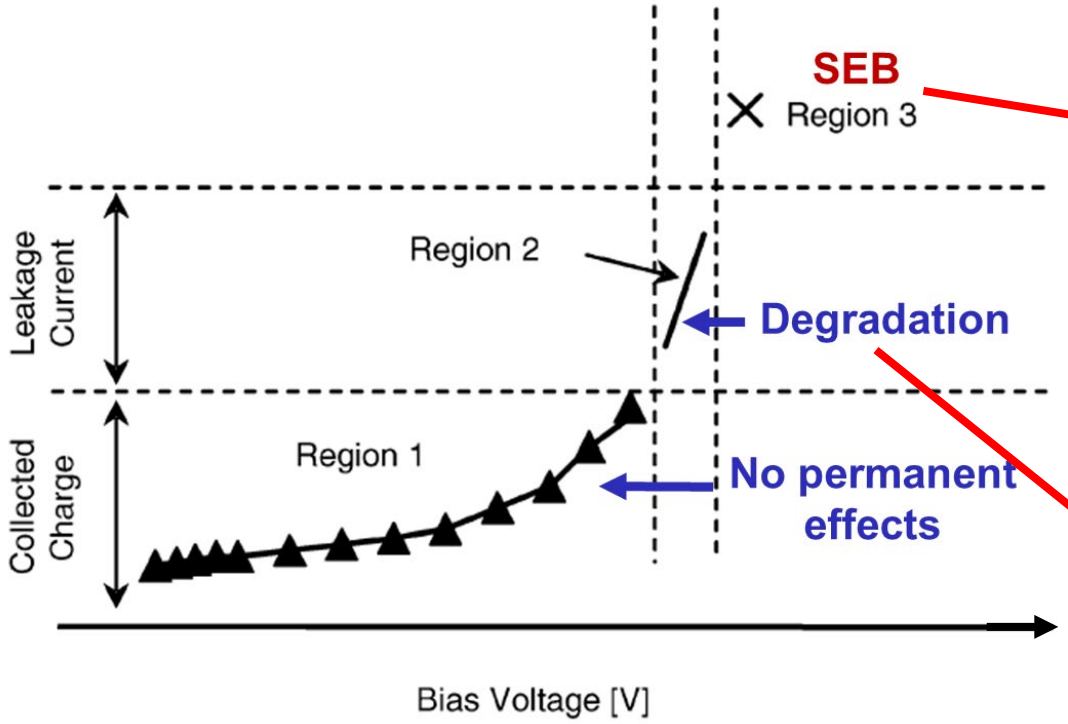
Many gate designs:

- **Schottky gate (normally on)**
  - Aktas, 2004 demonstrated 0.1 V threshold shift after **6 Mrad(Si)** γ irradiation
  - Harris, 2011 demonstrated no significant shift after **15 Mrad(Si)** proton irradiation
- **p-GaN gate (normally off)**
  - **500 krad(Si)** γ irradiation: < 18% Vth shift (Lidow, 2011)
- **Cascode design (normally off)**
  - Limited data (see Qi, 2020, *Nanotech & Prec Eng*)
  - Gate controlled by low-V n-type commercial Si MOSFET
- **MISHEMT (normally off)**
  - Oxide/insulator under recessed gate

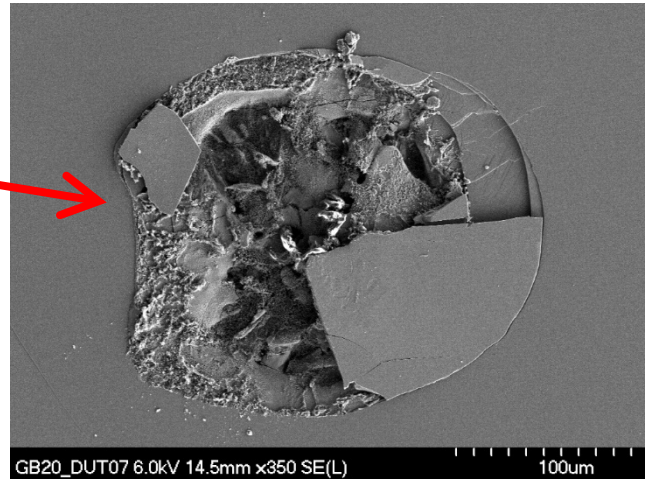
GaN HEMT TID effects may vary as a function of gate design

SILICON CARBIDE POWER DEVICE SINGLE-EVENT EFFECTS

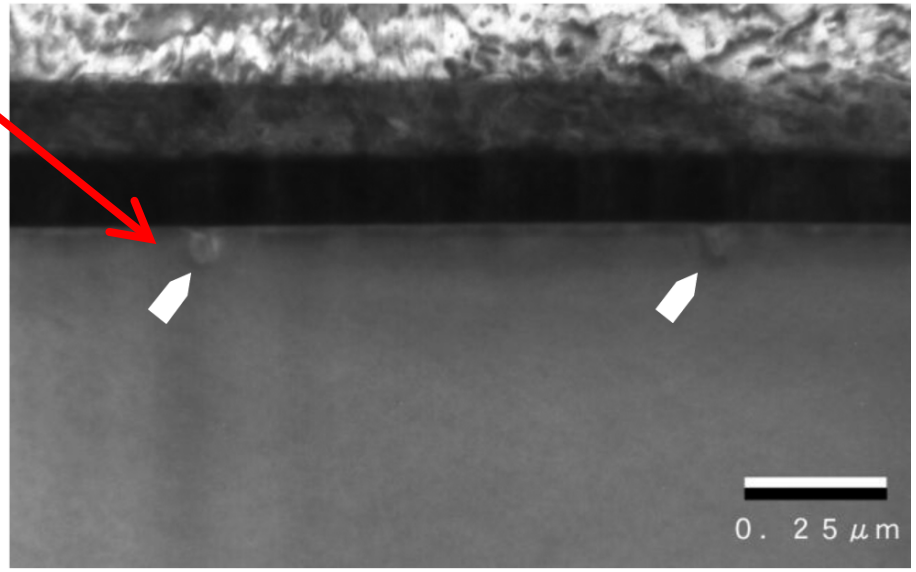
SiC Single-Event Effects: Diodes



After Kuboyama, IEEE TNS, 2006



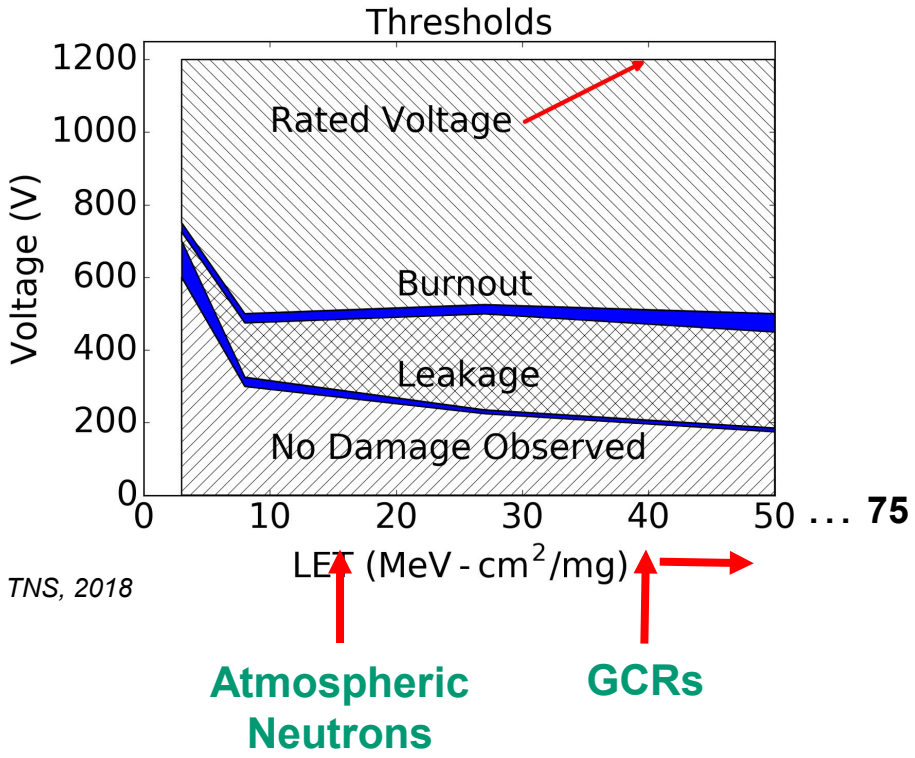
NASA GRC: A. Woodworth, 2015



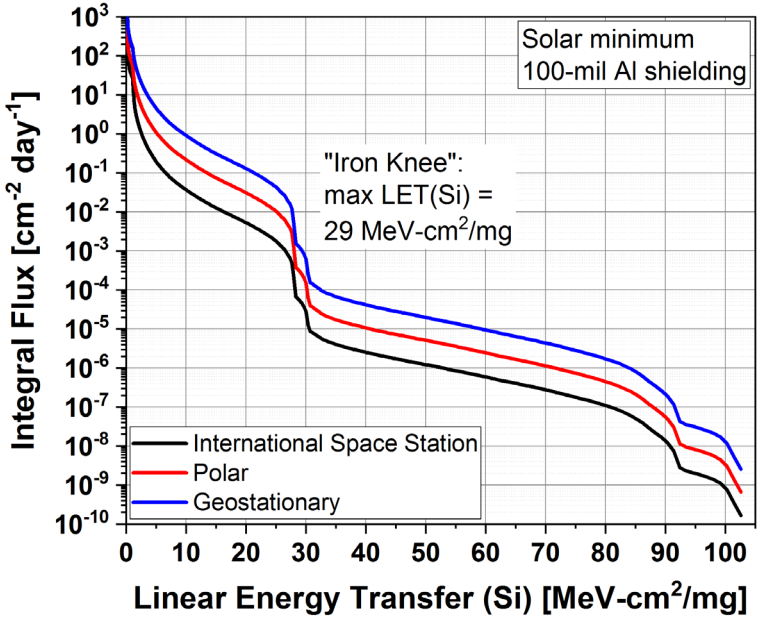
Kuboyama, IEEE TNS, 2006

- **SEEs in SiC Schottky diodes include:**
  - **Transient charge collection**
  - **Permanent increased leakage current**
  - **Catastrophic single-event burnout (SEB)**

SiC Schottky Diode SEE Thresholds



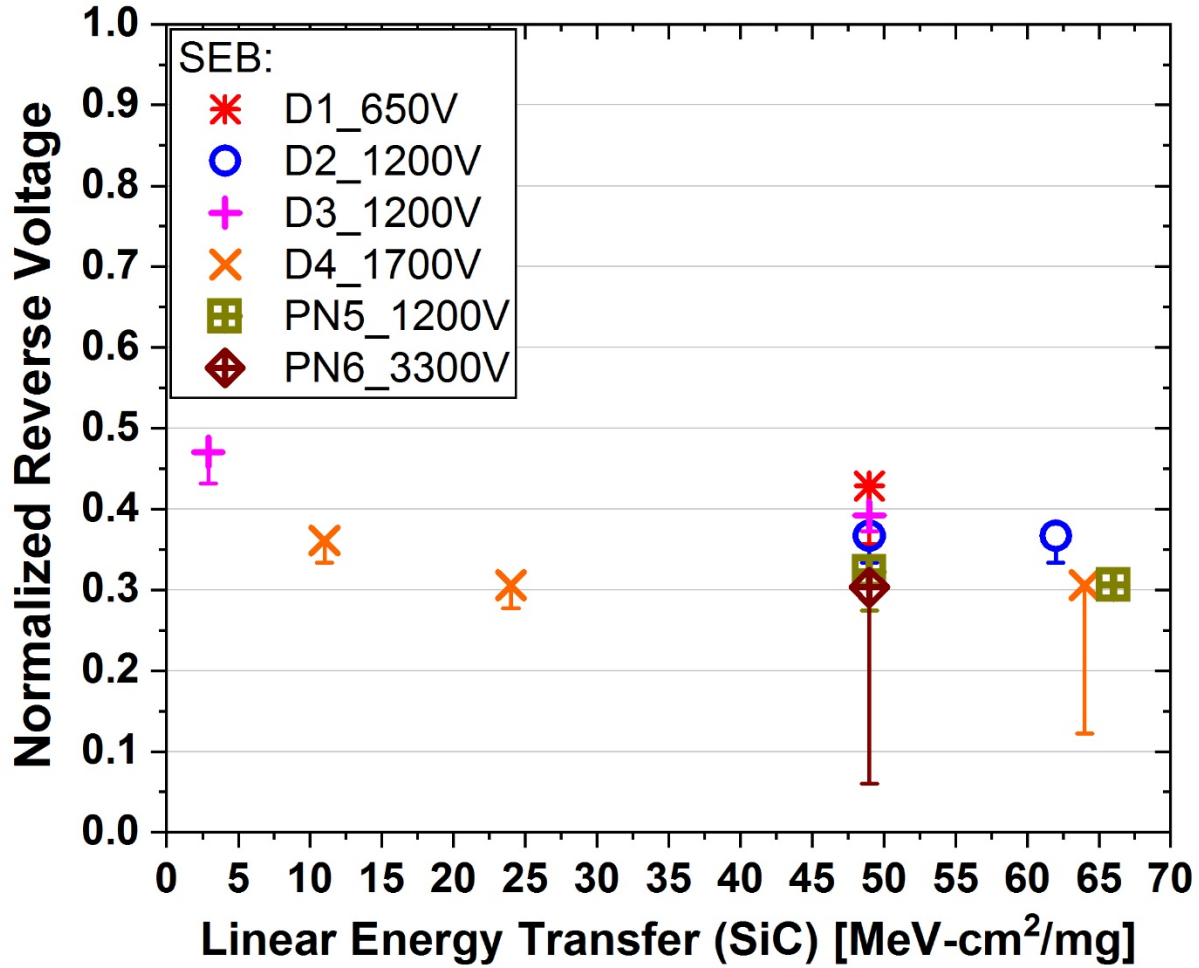
Witulski, IEEE TNS, 2018



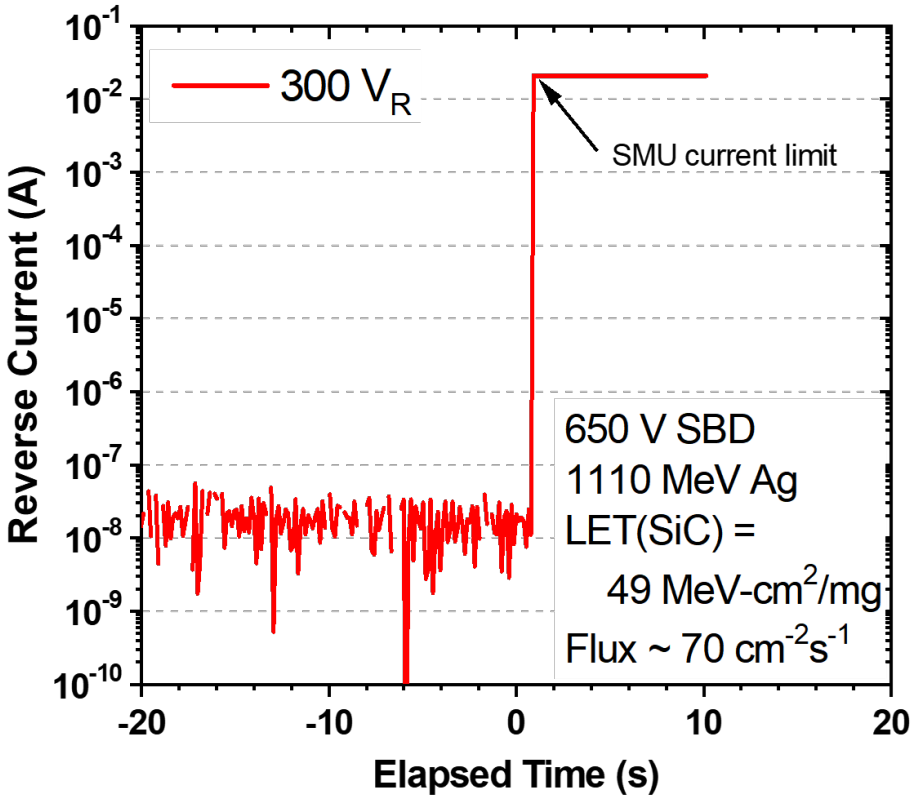
- **Onsets for ion-induced leakage current and single-event burnout saturate quickly with linear energy transfer (LET)**
  - Saturation occurs before the high-flux iron knee of the GCR spectrum

Risk-avoidant mission LET requirements for SEB vary by application: All fall within the saturation region of SEE sensitivity

SiC Diode Single-Event Burnout

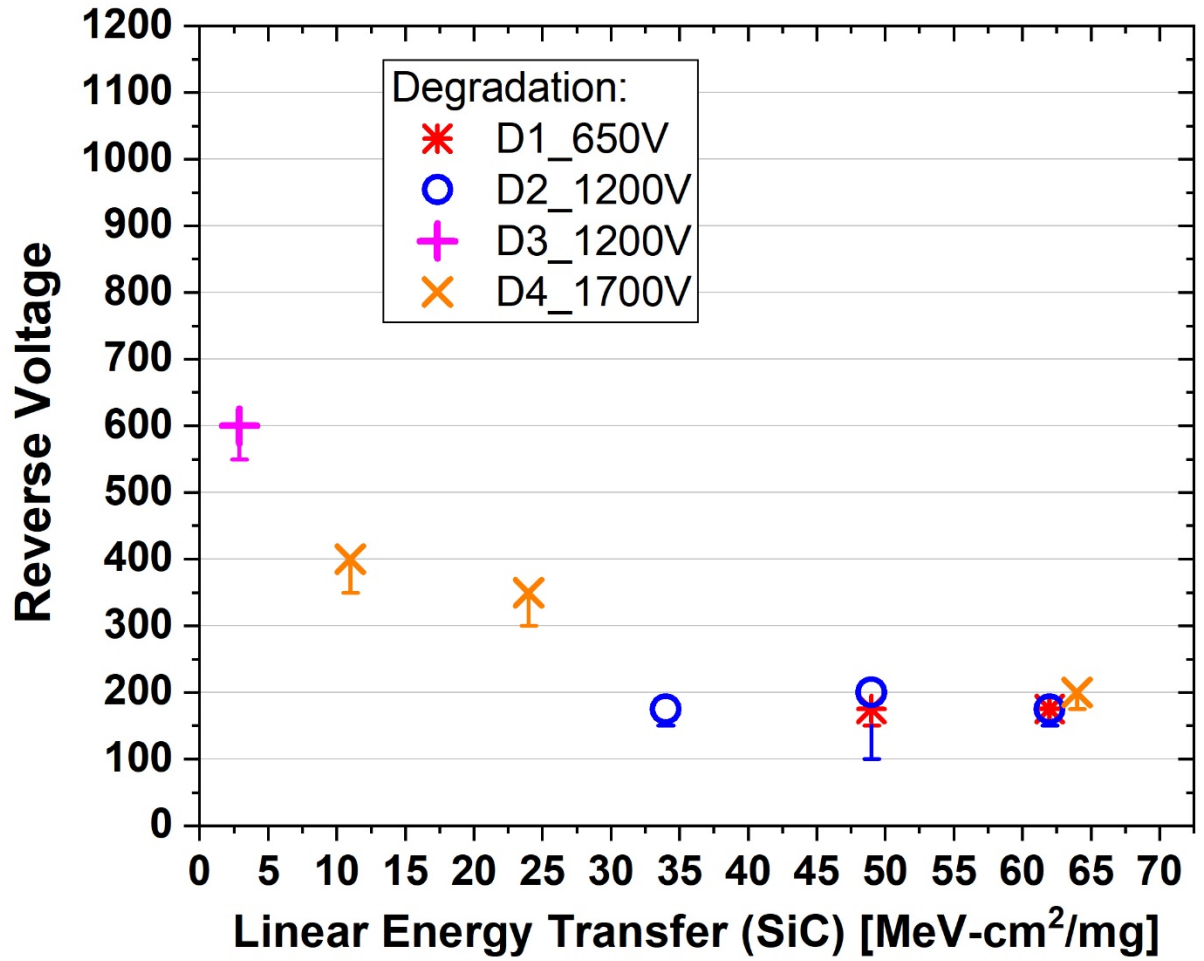


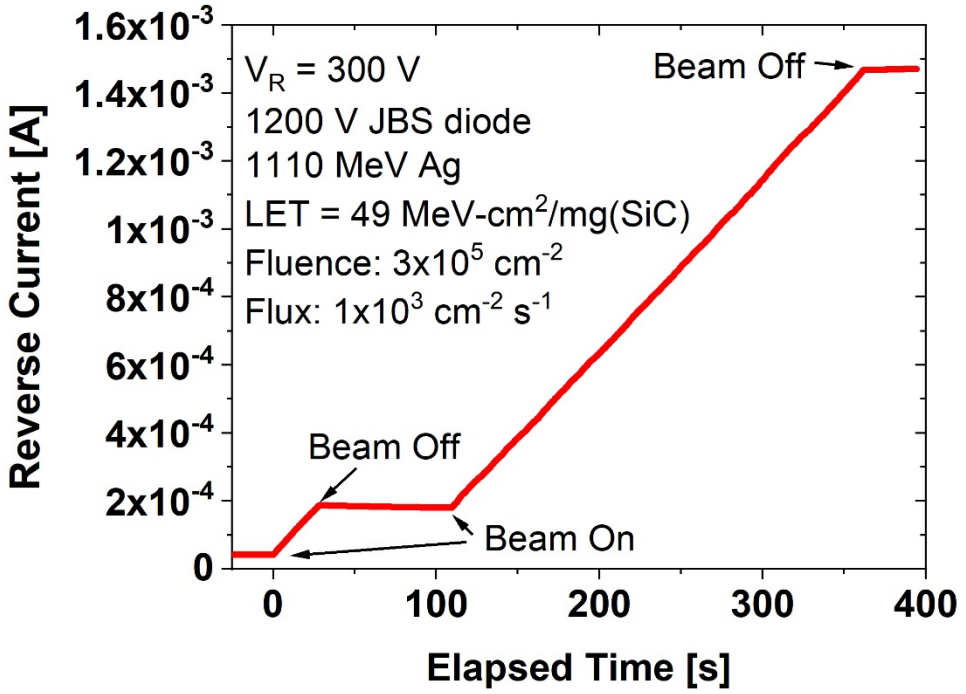
Lauenstein, IEEE IRPS, 2021



SEB is strongly electric field dependent:
650 V – 3300 V diodes fail at similar fraction of rated V_R

SiC Diode Single-Event Leakage Current (SELC)

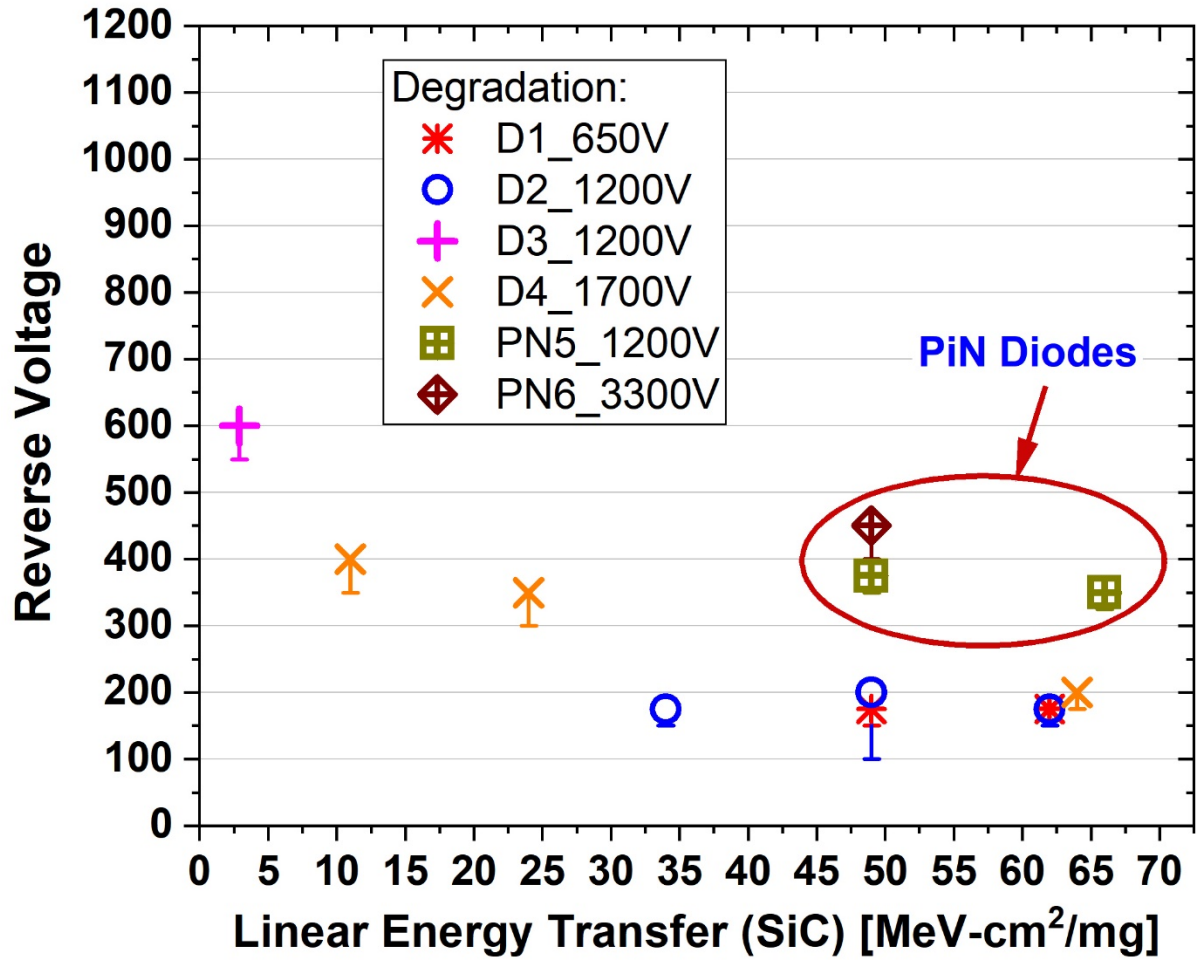




Lauenstein, IEEE IRPS, 2021

Electric field is not a primary factor for SELC:
Onset V_R for degradation is similar for 650 V – 1700 V Schottky diodes

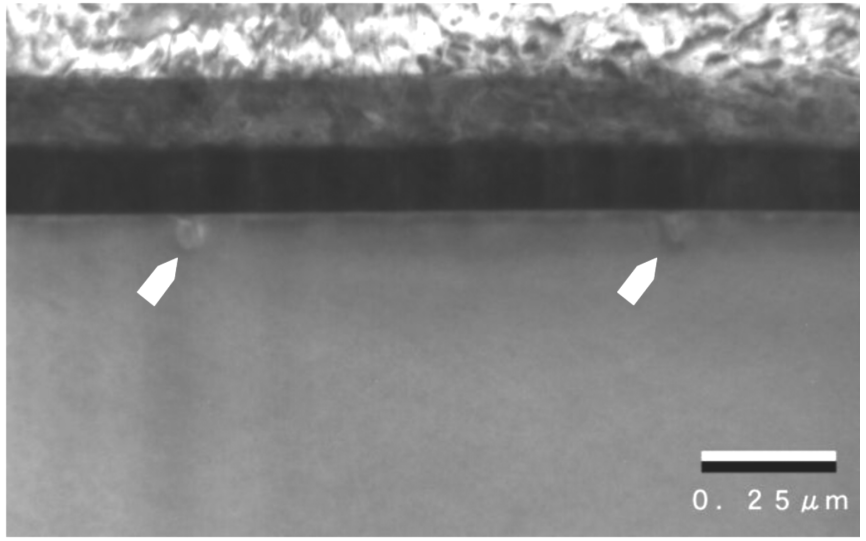
SiC Diode Single-Event Leakage Current (SELC)



Lauenstein, IEEE IRPS, 2021

PiN diodes have a higher threshold voltage for SELC, suggesting a role of the Schottky metal contact in initial degradation effects

SiC SELC Mechanisms



50 nm x 70 nm damage sites in SiC SBD: 3 MeV/u Xe while at 26% of rated V_R

Kuboyama, IEEE TNS, 2006

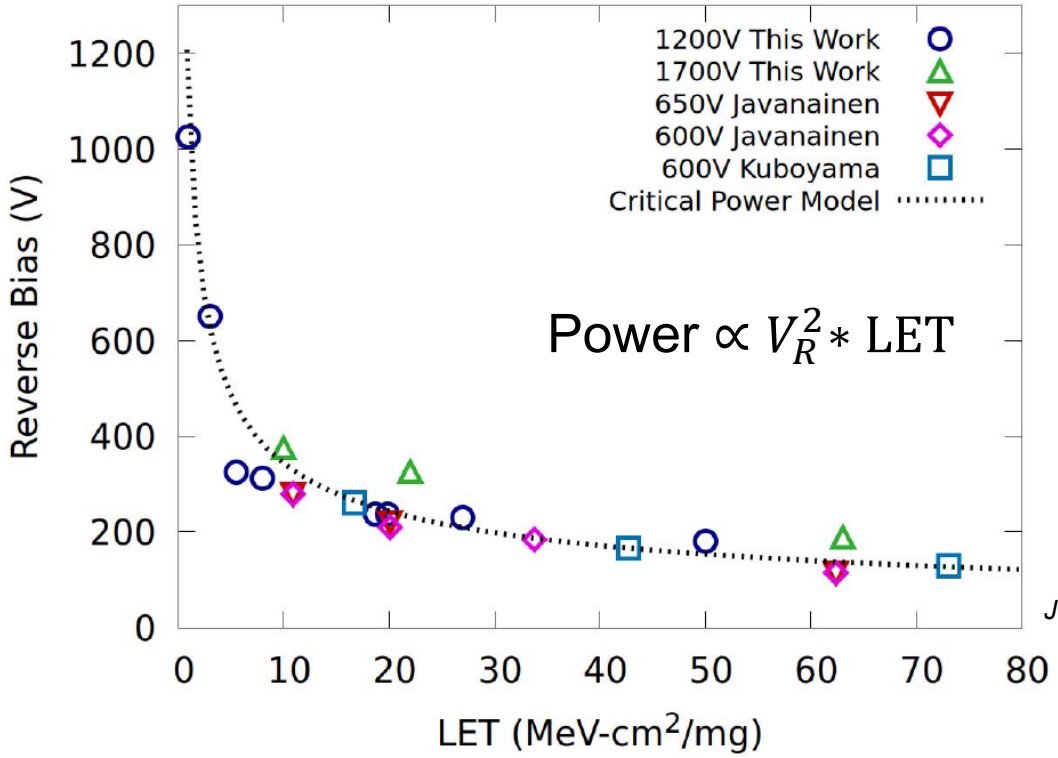
Kuboyama, *et al.*, 2006 findings:

- **SELC requires electric field**
  - **Displacement damage does not**
- **Non-ionizing energy loss (NIEL) factor**
  - **predicts much lower amount of leakage current per ion strike**
- **Result of Joule heating**
  - **Damage site diameter ≈ ion track width**

Individual ion strikes create areas of thermal damage that differ from displacement damage

SiC SELC Mechanisms

- **600 V – 1700 V SBD & JBS diodes require the same critical power density for onset of damage**

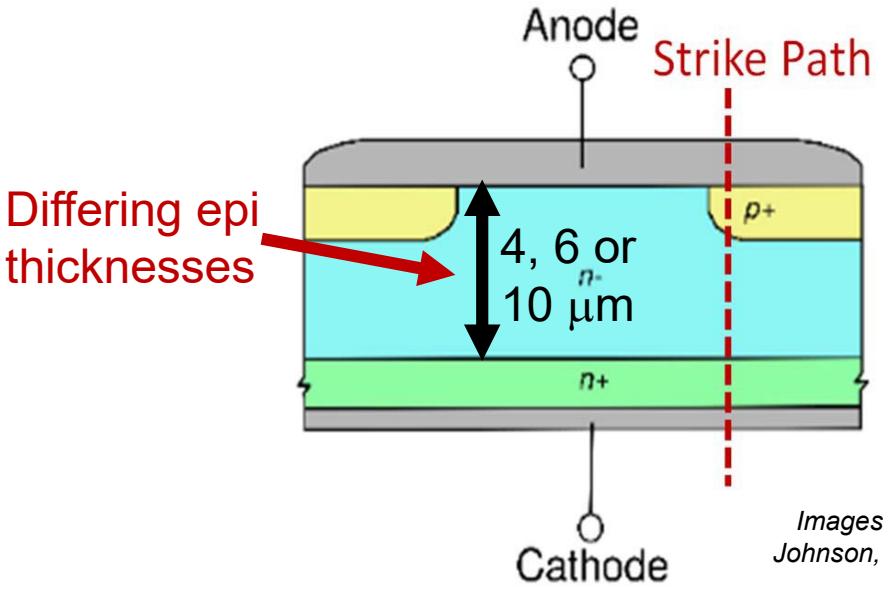


Johnson, IEEE TNS 2019

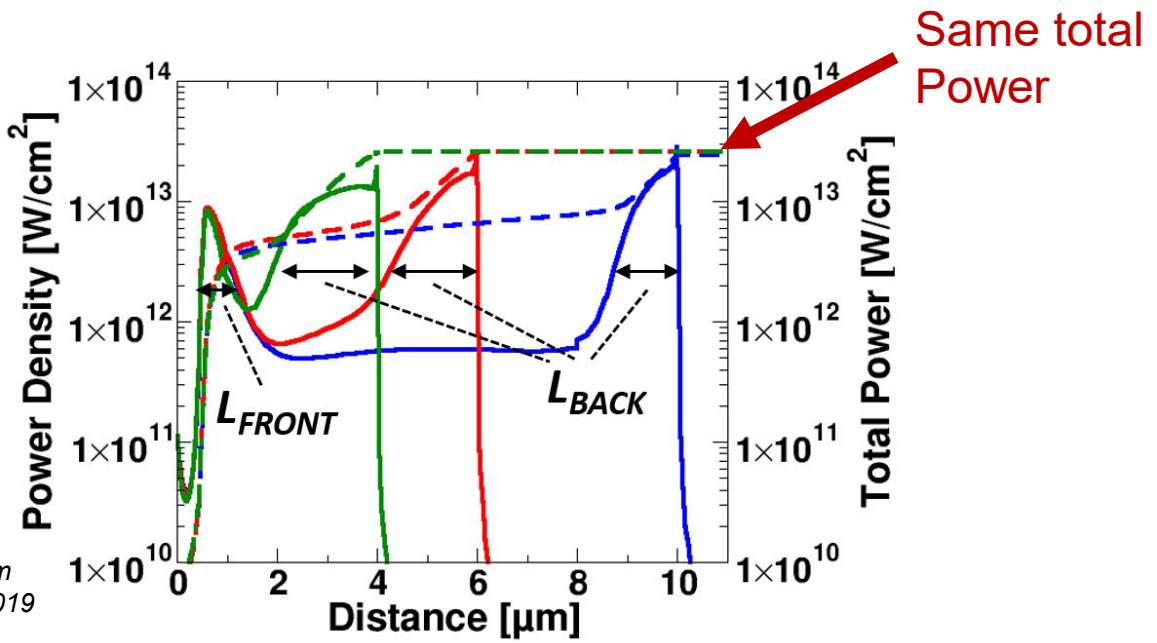
Degradation has minimal dependence on rated breakdown voltage

Weak Electric Field Dependence Explained

- $\vec{E}$-field maxima at the epi/sub. interface & near the Schottky contact due to ion strike
- Much of the epilayer thickness is not dissipating significant power
- Thus similar total power dissipation regardless of epi thickness & rated voltage



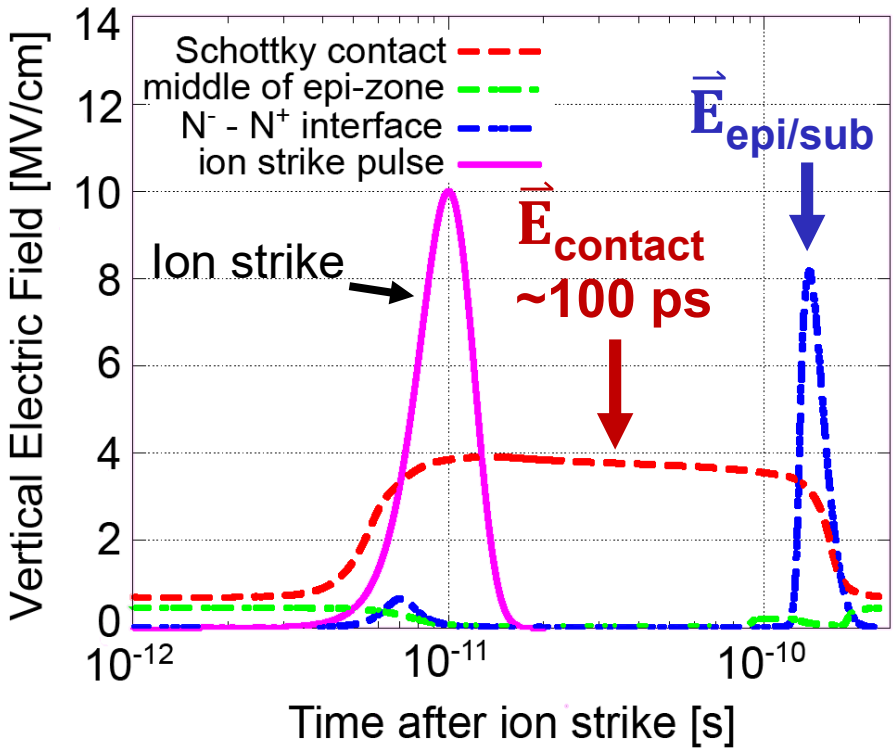
Images modified from Johnson, IEEE TNS 2019



Implication: Minimal SELC benefit from derating higher-voltage parts vs. using a part with lower breakdown rating!

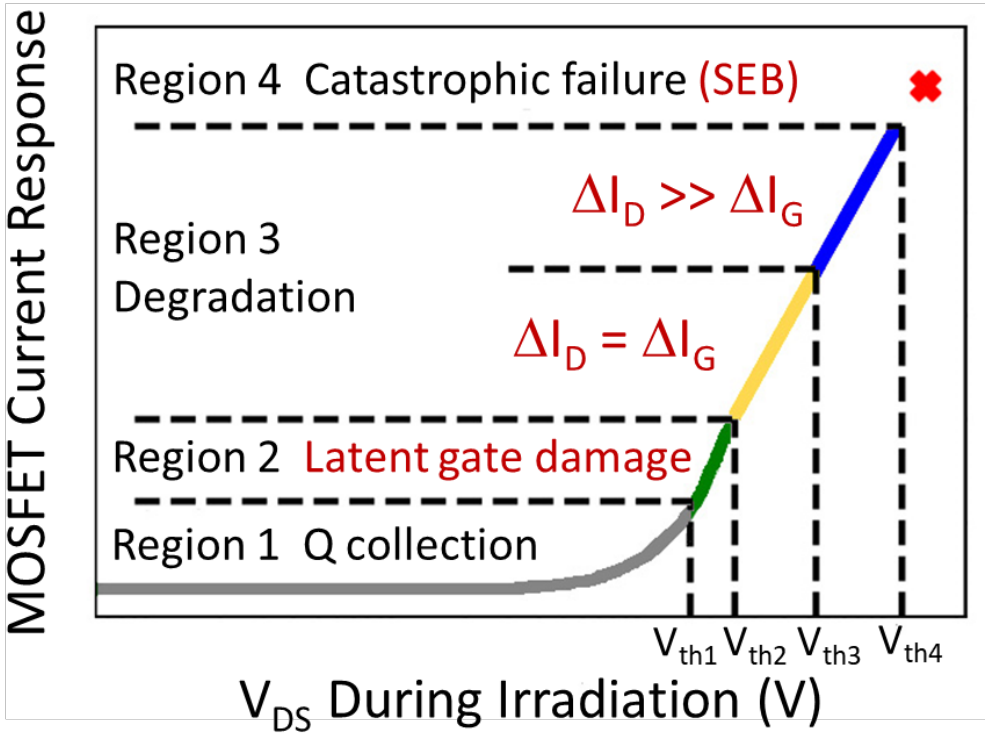
SEB: Source of High Power Density in Schottky Diodes

- **Key components for SEB in SiC Schottky diodes identified via TCAD:**
  - Duration of high $\vec{E}$-field at Schottky contact
  - Impact ionization then regenerative Schottky contact electron injection for thermal runaway at the contact interface
    - See Kuboyama, IEEE TNS, 2019



Witulski, IEEE TNS 2018

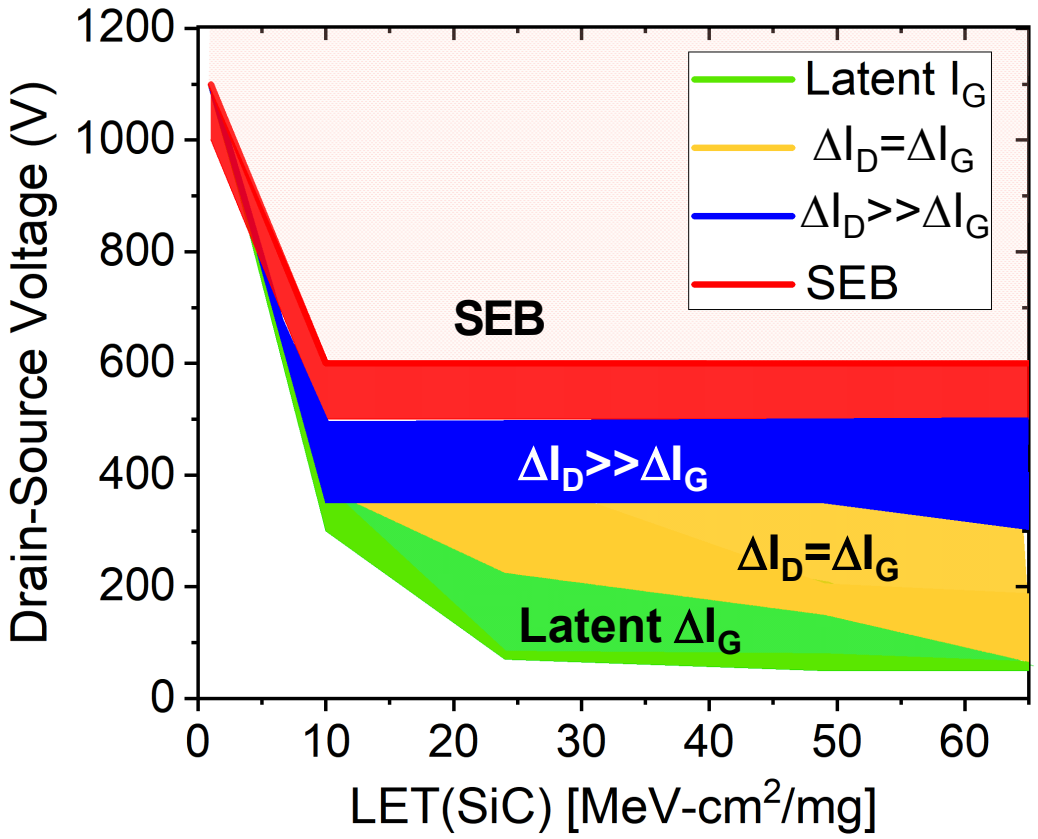
SiC Power MOSFET Single-Event Effects



After Martinella, IEEE TNS, 2020

- **SEEs in SiC MOSFETs include gate effects**
  - **Latent gate damage**
  - **Permanent increased leakage current**
    - Drain-Gate or Drain-Source leakage pathway
      - see Martinella, IEEE TNS 2020
- **Catastrophic single-event burnout (SEB)**
- **SiC JFETs have similar behavior except:**
  - Rare to have drain-source leakage
    - Drain-gate leakage is main degradation pathway
  - No latent gate damage (no gate oxide)

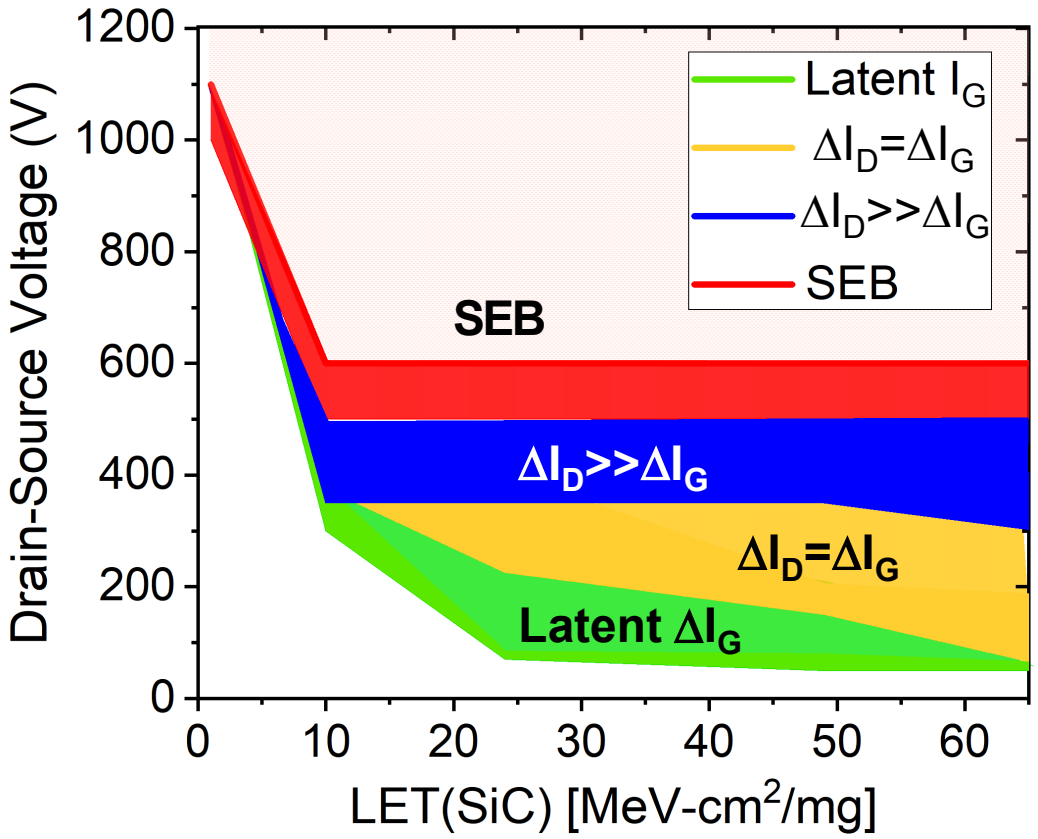
SiC Power MOSFET Single-Event Effects



see also Martinella, Microelectron Reliab, 2021

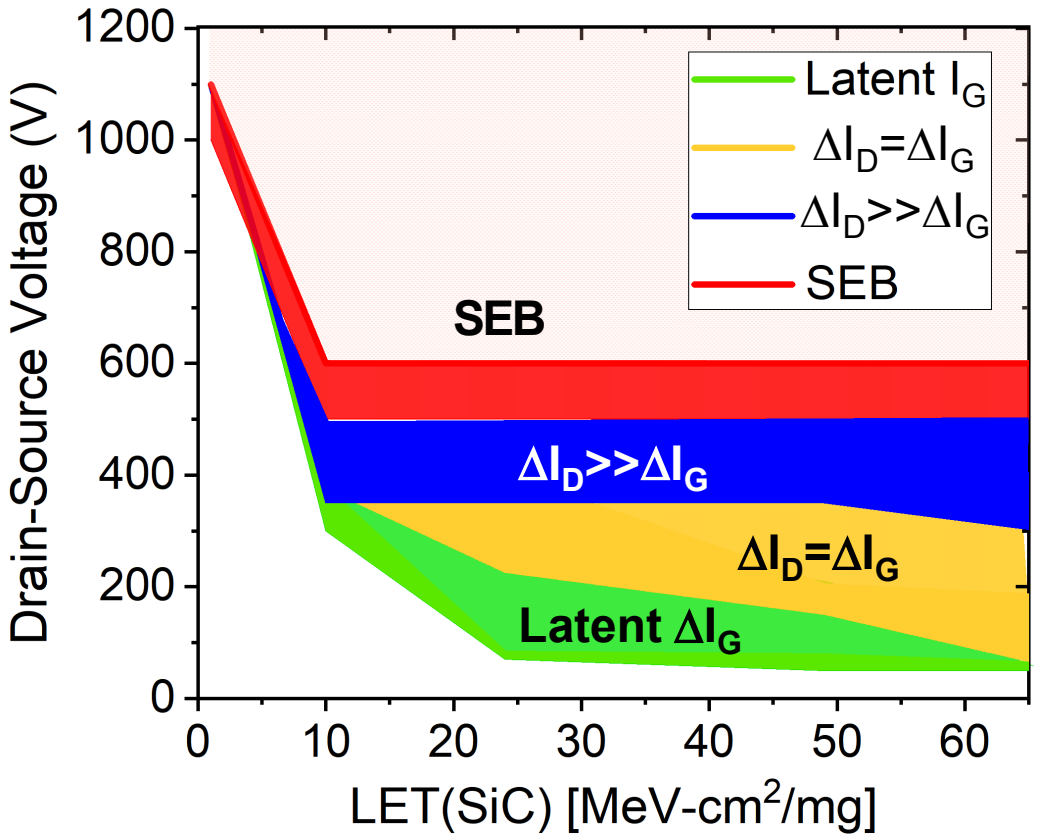
- **Typical 1200 V MOSFET SEE thresholds:**
  - **SEB and drain-source SELC saturate at low LET, similar to diode effects**
  - **Latent gate damage occurs at very low V_{DS}**
  - **At lowest LETs, SEB dominates**

SiC Power MOSFET Latent Gate Damage

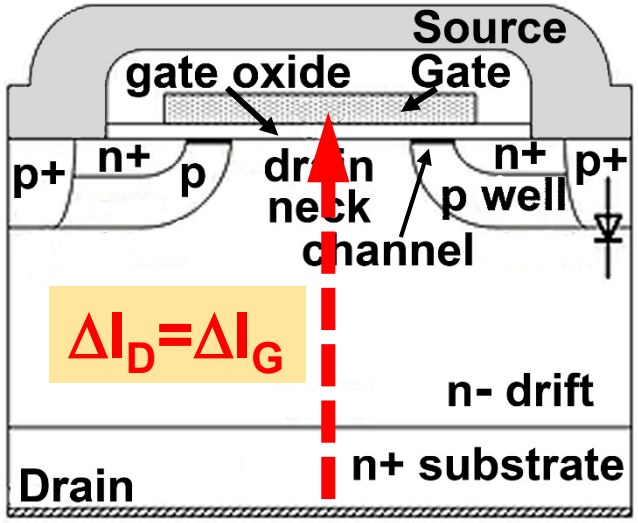


- **Latent gate damage (green):**
  - **Reduced with lower LET/lighter ions**
  - **At high LETs, onset at ~50 V to 75 V!**
- **Mechanism:** (Busatto, 2020 Microelectron Reliab)
  - **Ion strike causes high $\vec{E}$ox**
    - high hole trapping in oxide
    - shift of SiC electric field across oxide
  - **High $\vec{E}$ox results in fast current injection**
    - Poole-Frenkel like rapid emission of holes from oxide traps
    - Fowler-Nordheim tunneling of holes across SiC/SiO_2 interface energy barrier

SiC Power MOSFET SELC

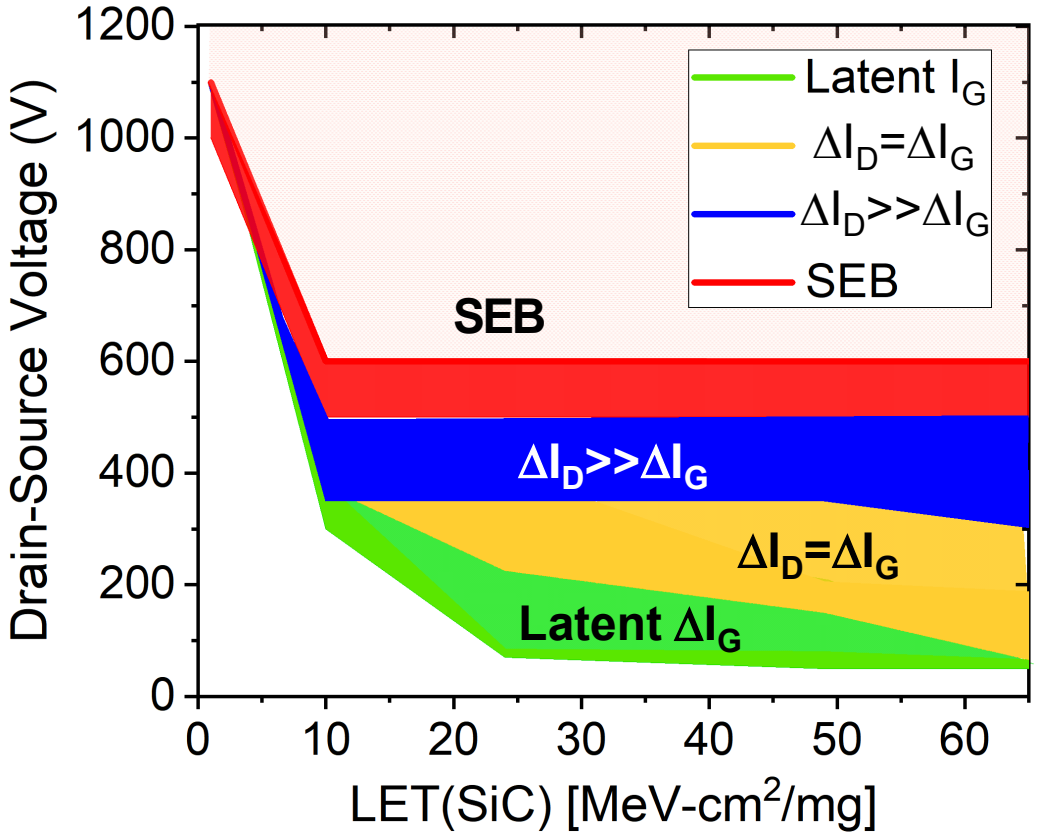


- **Drain-Gate SELC (yellow region):**
  - **Leakage thru oxide over drain "neck" region** (Martinella, 2020 IEEE TNS)
  - **Not all MOSFETs have drain-gate SELC**
    - Design techniques may eliminate this effect



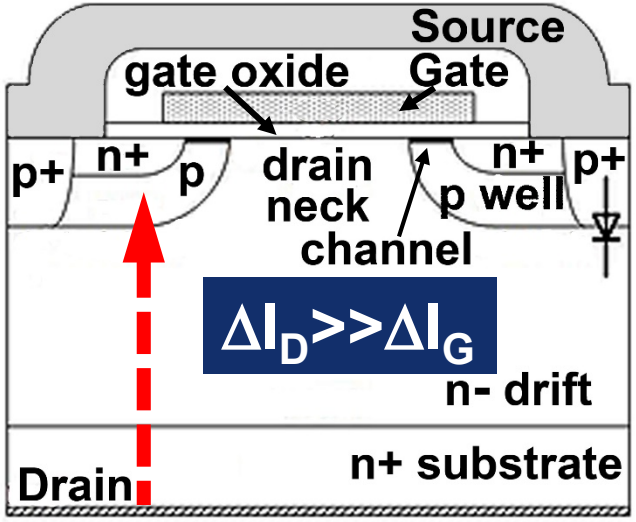
MOSFET image: Li, Micromachines, 2019. CC BY 4 license

SiC Power MOSFET SELC



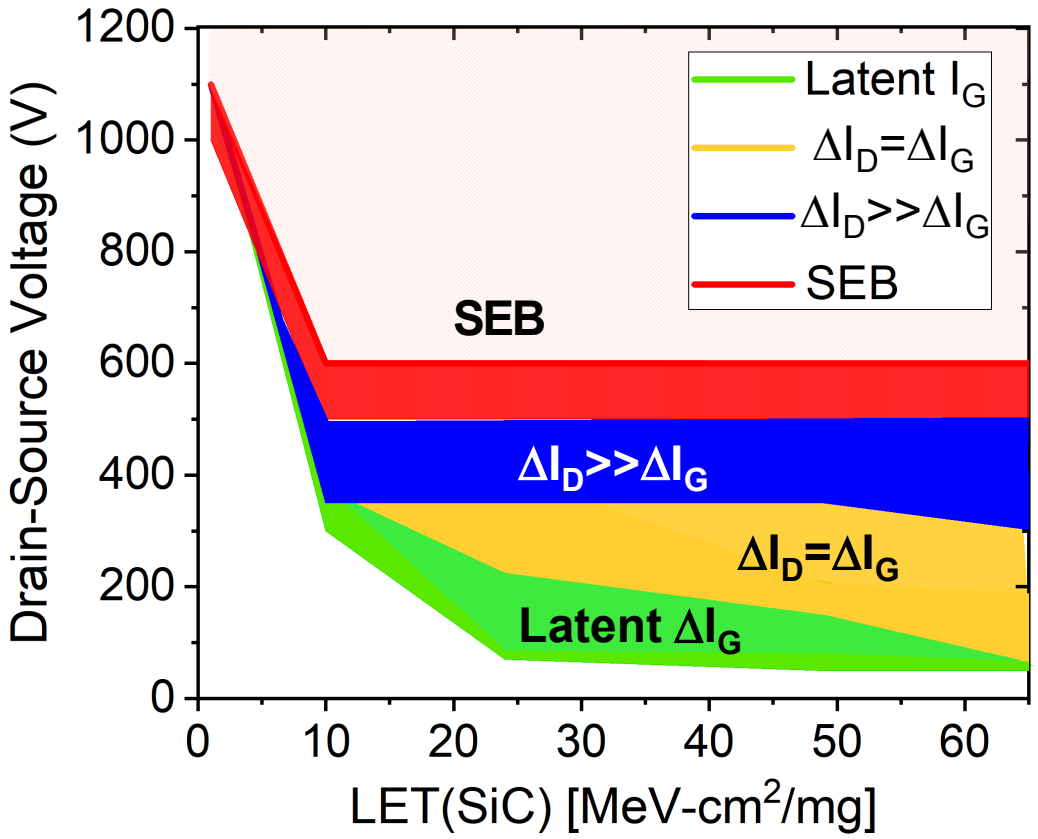
see also Martinella, Microelect Reliab, 2021

- **Drain-Source SELC (blue region):**
  - **Sensitive region is p-n junction (body-drain)** (Martinella, 2020 IEEE TNS)
  - **Least influenced by LET or electric field**
    - Onset ~400 V for SiC MOSFETs rated 900 V to 3300 V
    - Similar to SELC in diodes



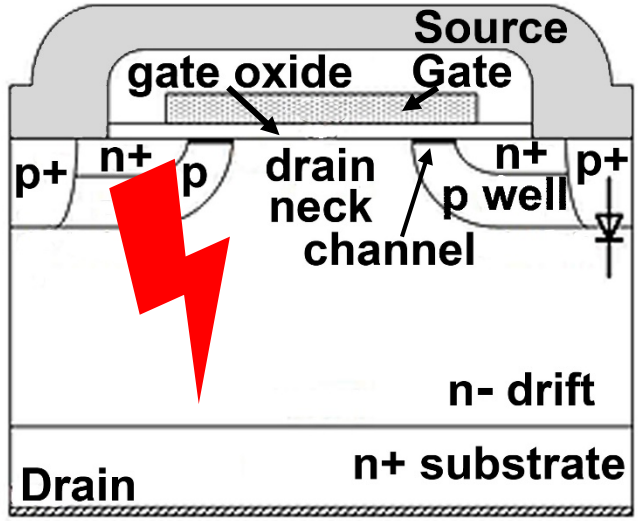
MOSFET image: Li, Micromachines, 2019. CC BY 4 license

SiC Power MOSFET SEB



see also Martinella, Microelect Reliab, 2021

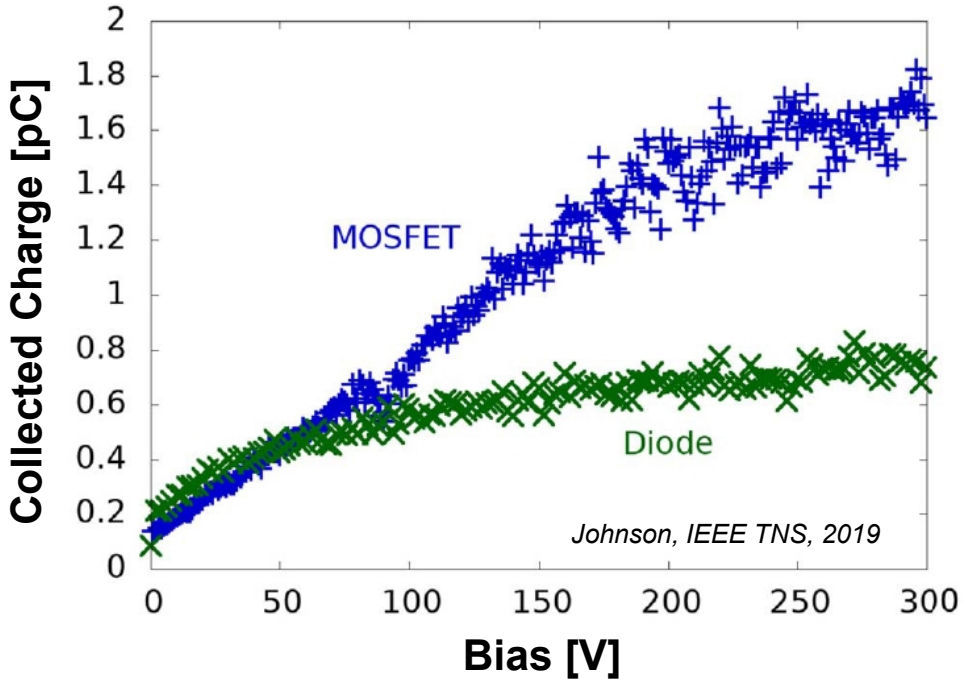
- **SEB (red region)**
  - **Max cross section at ~50% of rated V_{DS}**
  - **Susceptible at very low LET**
    - Proton/neutron risk



MOSFET image: Li, Micromachines, 2019. CC BY 4 license

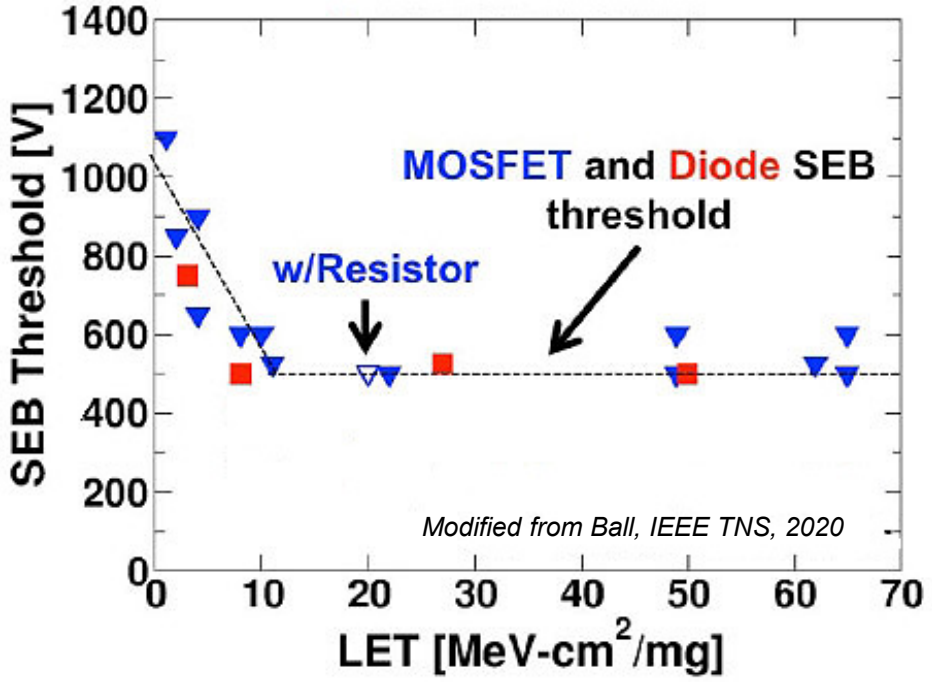
SiC MOSFET SEB: Minimal Parasitic BJT Involvement

Evidence of BJT Turn-On



- Pulsed laser tests of matched MOSFET & diode show MOSFET charge amplification
  - Johnson, IEEE TNS, 2019
- TCAD simulations show run-away current
  - Witulski, IEEE TNS, 2018

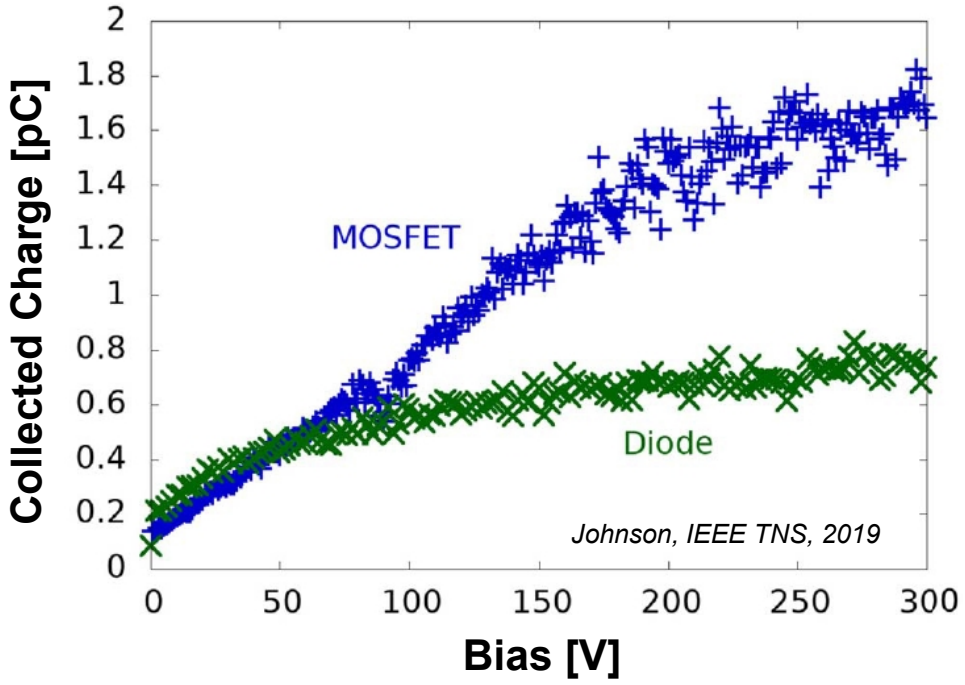
Data Do Not Support BJT Involvement



- SEB voltage in MOSFET = Diode
- SEB protective mode testing fails
  - Ball, IEEE TNS, 2020
- Removal of MOSFET n+ source implant yielded similar simulated max lattice temperature
  - Shoji, Microelectronics Reliability, 2015

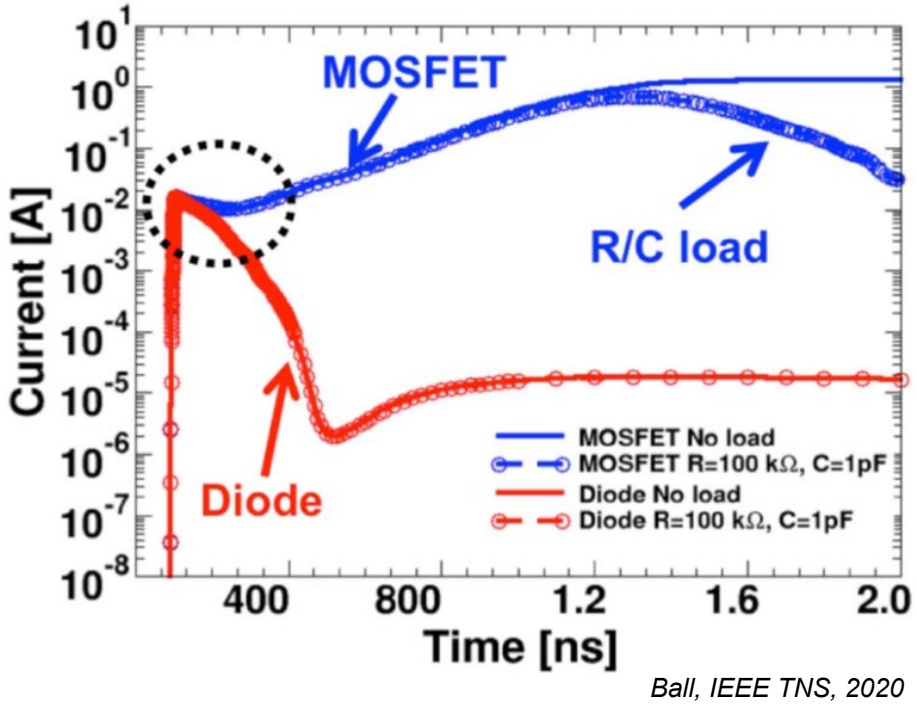
SiC MOSFET SEB: Minimal Parasitic BJT Involvement

Evidence of BJT Turn-On



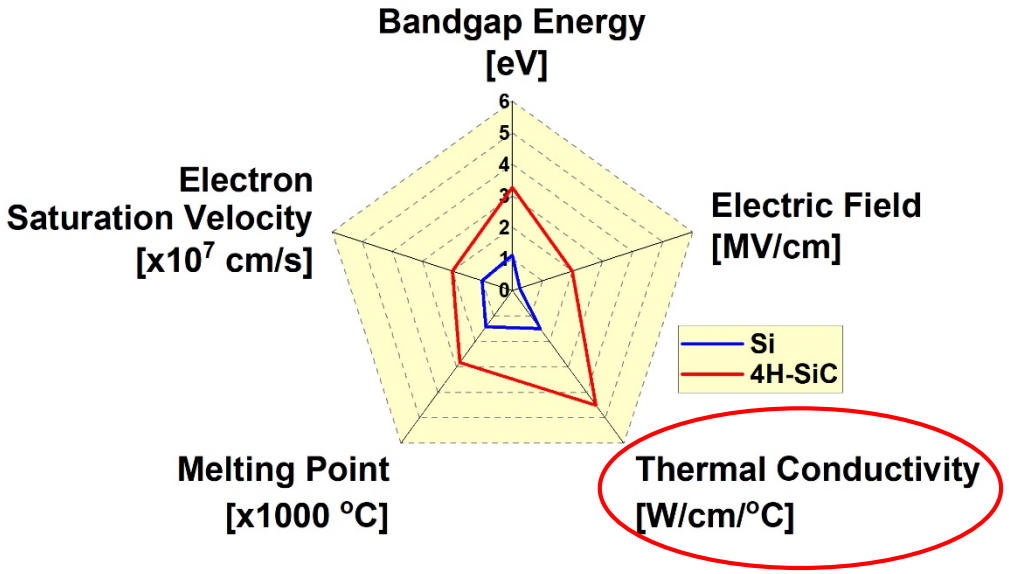
- Pulsed laser tests of matched MOSFET & diode show MOSFET charge amplification
  - Johnson, IEEE TNS, 2019
- TCAD simulations show run-away current
  - Witulski, IEEE TNS, 2018

TCAD Explanations



- MOSFET & diode similar only in first ~100 ps
- SEB protection circuitry too slow
  - Ball, IEEE TNS, 2020
- Note TCAD sims of increased substrate resistance showed decreased max temperature
  - Abbate, IEEE TNS, 2015

SiC Properties Revisited: Thermal Conductivity



- **High thermal conductivity, but not instantaneous**
  - Heat removal via acoustic phonons
  - **≥ ns to start conducting heat away**
    - See Akturk, IEEE TNS, 2018

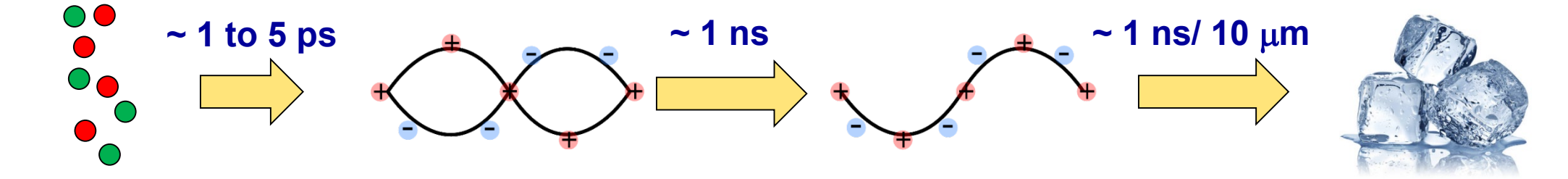
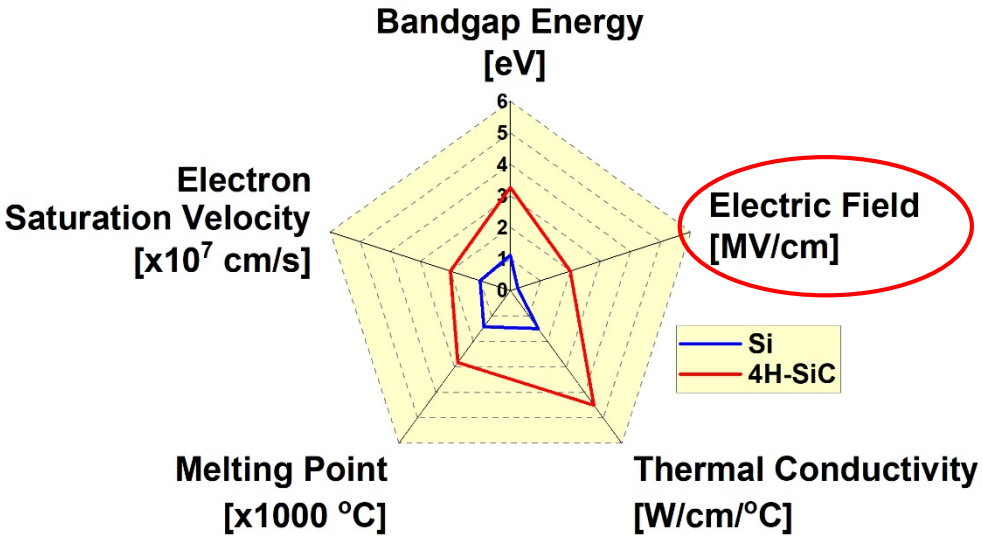


Image: Creative Commons, M. Griffith, 2017

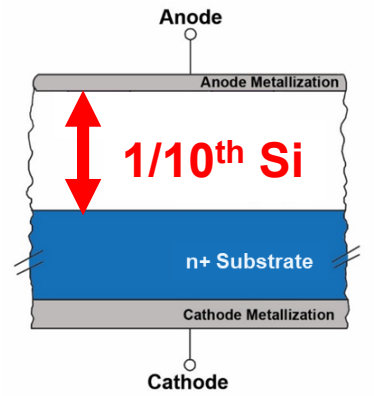
SiC Properties Revisited: Electric Field



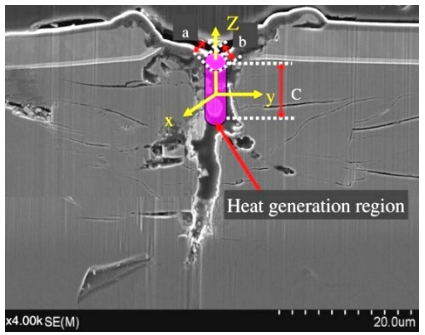
- **Peak $\vec{E}_{SiC}$ > 10x peak $\vec{E}_{Si}$ means 100x higher heat generation density**
  - More rapid rise in temperature (T)
  - ΔT = time × power / heat capacity (C)
    - C ∝ heated volume
  - **SiC sublimation in picoseconds**
    - See Shoji, JJAP 2014 & Akturk, IEEE TNS 2018

$$\text{Power} = \frac{V^2}{R}$$

Joule's law



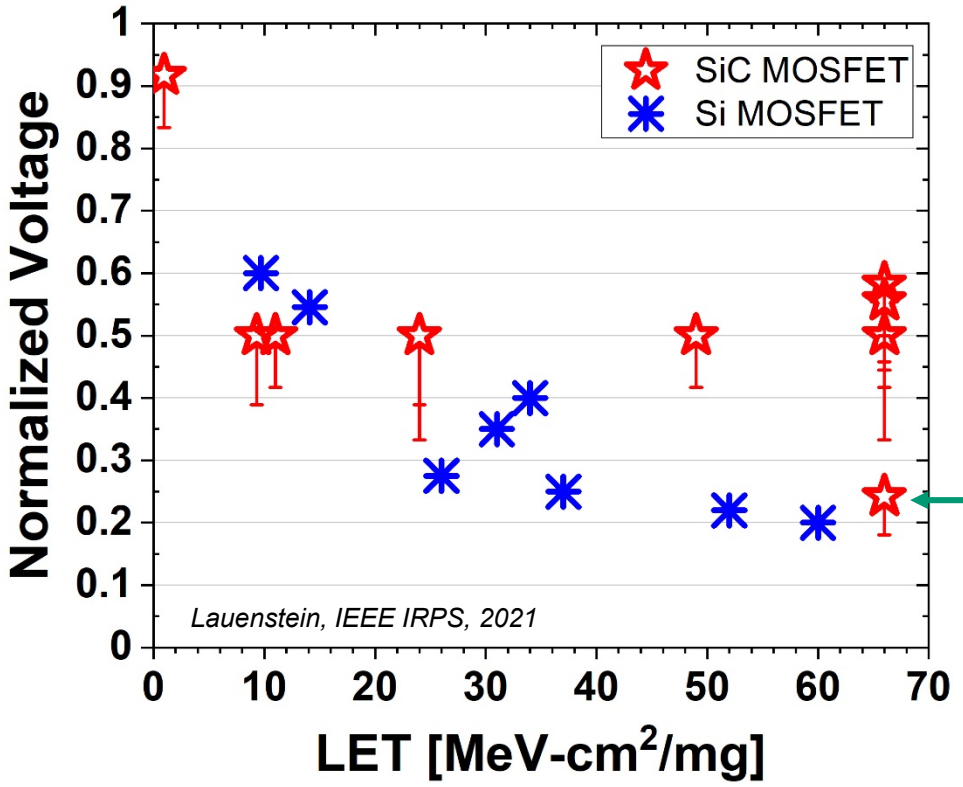
SiC epi thickness



SEB

Image: Shoji, et al., © (2014) The Japan Society of Applied Physics, used with permission.

Silicon Carbide vs. Unhardened Silicon: Power MOSFET SEB Susceptibility



SiC MOSFETs: 900 V to 3300 V

Si MOSFETs: 50 V to 200 V

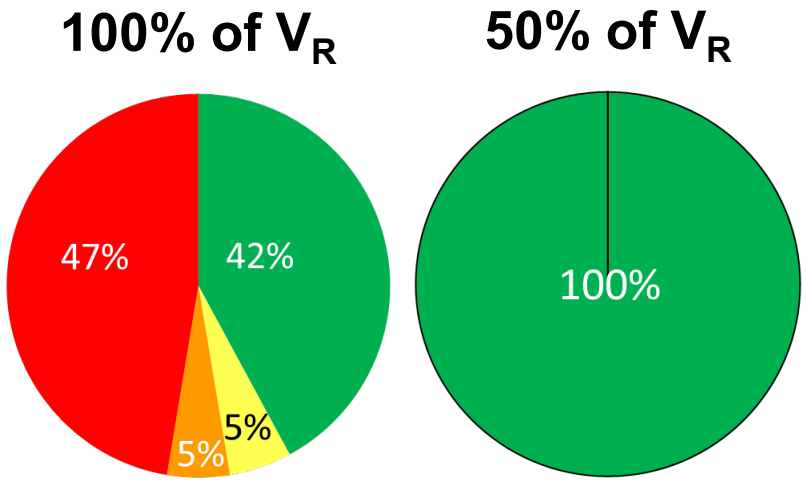
3300 V

SiC MOSFETs are generally less susceptible to SEB than unhardened, commercial silicon MOSFETs **

**** Not shown: SiC MOSFETs are more susceptible to permanent, non-catastrophic damage effects.**

Silicon Carbide vs. Silicon: Schottky Diode SEB Susceptibility

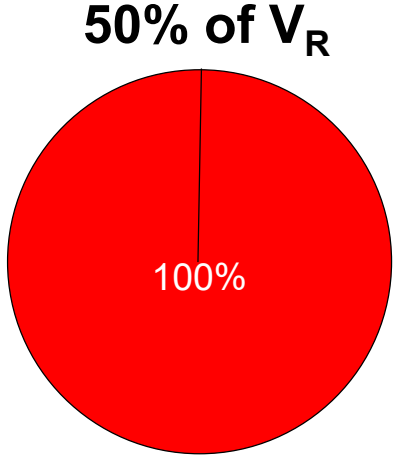
Silicon



No SEB at 50% of V_R
(LET = 59 MeV-cm^2/mg(Si))

Plots: Casey, IEEE NSREC, 2015

Silicon Carbide



SEB at ~ 50% V_R
(LET << 59 MeV-cm^2/mg(SiC))

Data from: Lauenstein, MRQW, 2018

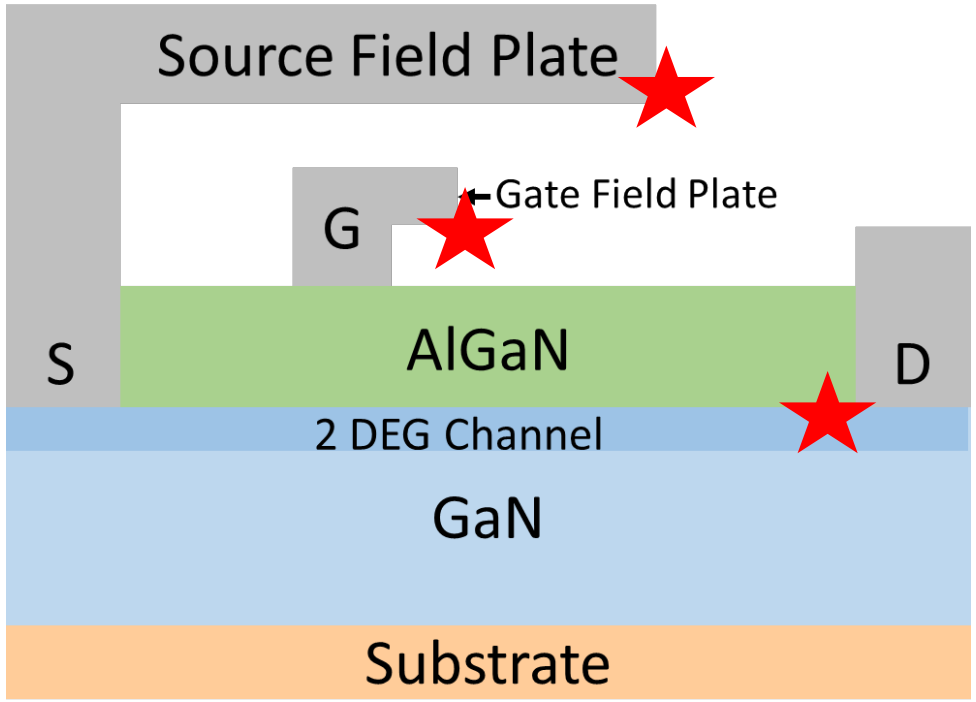
- **SiC Shottky diode susceptibility to SEB occurs at < 50% of avalanche V_R**
- **Si Schottky diodes pass at this derating level, with almost half passing at 100%**

To date, no tested commercial SiC diodes pass above ~50% of rated V_R at mission LET requirement levels

GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) RADIATION EFFECTS

GaN HEMT Single-Event Effects

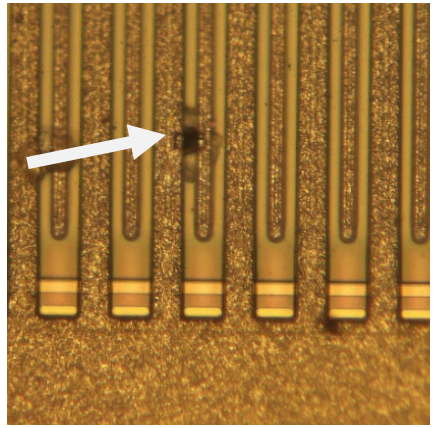
- **Power GaN HEMT structure**
  - Lateral device
  - Insulators under field plates
  - Possible gate oxide/insulator
  - No p-n junction - cannot avalanche
  - Breakdown voltage >> rated voltage
- **SEEs include:**
  - Leakage current degradation
  - Single-event burnout
  - Single-event dielectric rupture (SEDR)



GaN HEMT SEE Failure Thresholds

- **SEE data vary:**
  - Multiple HEMT designs
  - Lot-lot variability
  - Generational variability
- **Guaranteed SEE-free HEMTs exist**
  - Max 300 V

SEB/DR mark on gate contact

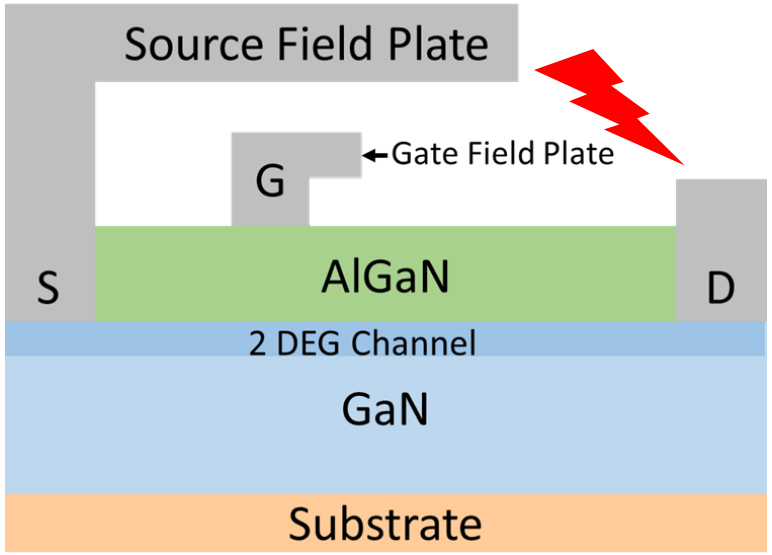


Images: NASA JPL, courtesy of L. Scheick

- **Susceptibility tends to increase with voltage rating, with exceptions**
  - Expect 40 V parts to pass at 40 V
  - 100 V & 200 V parts:
    - some only degradation;
    - others SEB susceptibility
  - Expect SEB in ~ 600 V p-gate parts ~50% of rating at LET ~ 40 MeV-cm^2/mg(Si)

GaN HEMT SEE thresholds vary;
Guaranteed SEE-free parts are available

GaN HEMT Dielectric Rupture



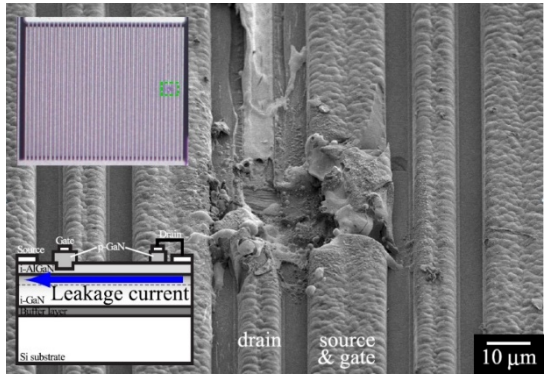


Image: Mizuta, et al., IEEE TNS 2018

- **SEDR: Source-Drain Shorting**
  - Worst-case angle parallel to channel
    - Also occurs at normal incidence
  - Simulations suggest ion strike at edge of field plate necessary at normal incidence
    - see Zerarka, IEEE TNS 2017
  - Low cross section for failure
    - Supports simulation findings

Field plate design will likely affect SEDR susceptibility

GaN HEMT Single-Event Burnout

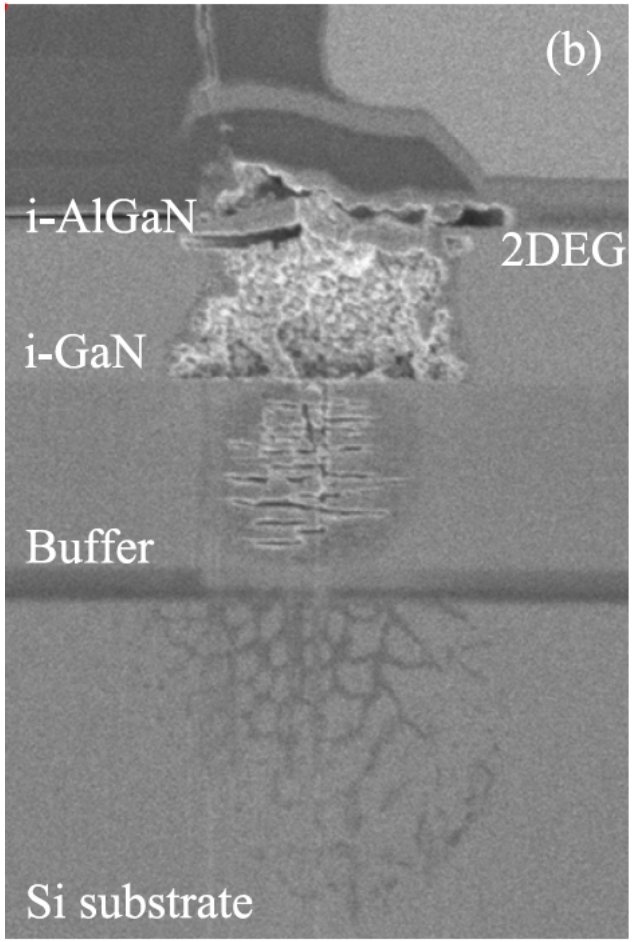
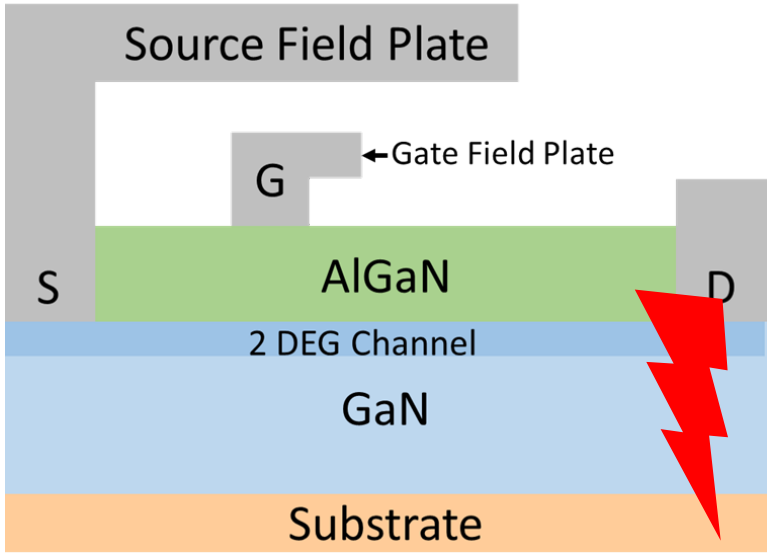


Image: Mizuta, et al., IEEE TNS 2018



- **SEB: Drain-substrate**
  - Requires ion range into substrate
    - see Zerarka, IEEE TNS 2017
  - Higher threshold V than for SEDR (for same part type) but higher cross section too

GaN HEMTs can have multiple catastrophic SEE failure modes

GaN HEMT Single-Event Leakage Current

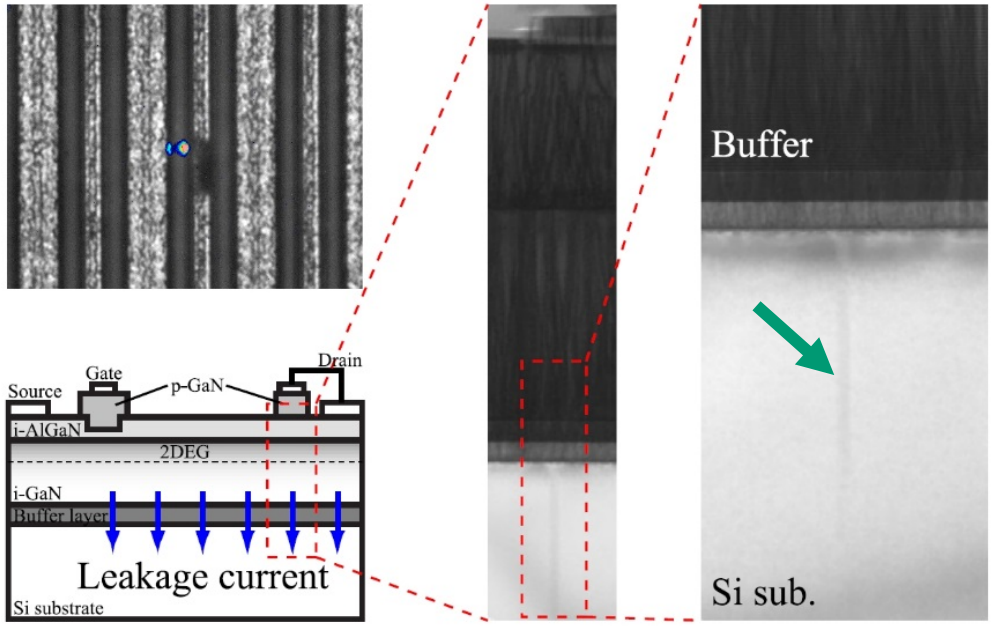
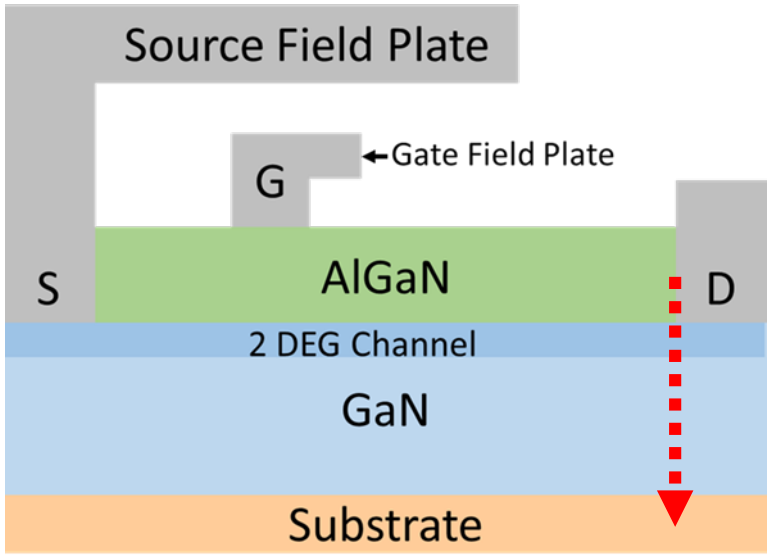


Image: Mizuta, et al., IEEE TNS 2018

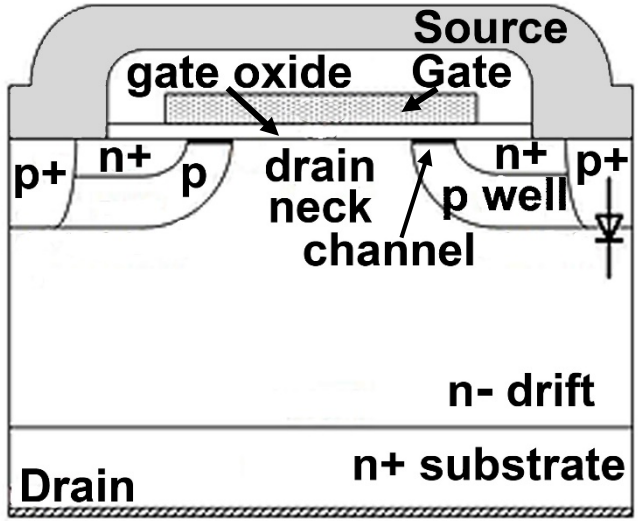


- **Drain-substrate non-catastrophic leakage current degradation**
  - Large drain SETs correlated with leakage current increase
    - see Abbate, Microelectron Reliab, 2015
- **Drain-Gate leakage current degradation reported in normally-on GaN HEMTs**
    - see ex/ Kuboyama, IEEE TNS 2011

RADIATION HARDNESS ASSURANCE CHALLENGES

Heavy-Ion Test Methodology for Silicon Power MOSFETs

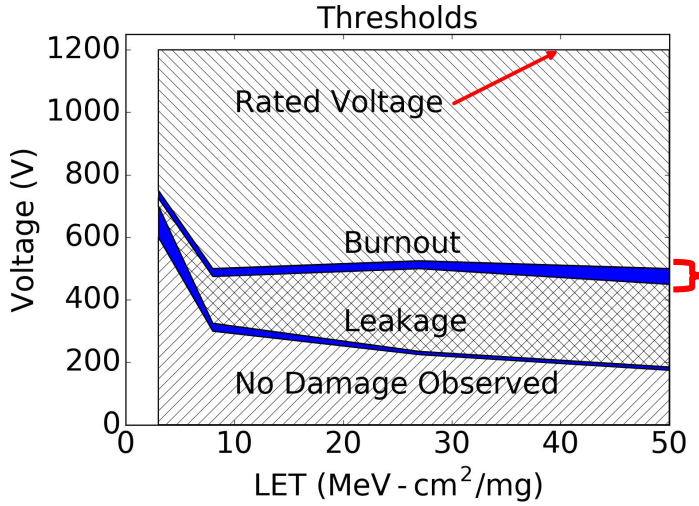
- **Worst-case ion beam conditions for VDMOS (and the JESD57 standard)**
  - Normal incidence
  - Ion Bragg peak at epi/substrate interface
- **Rationale**
  - Allows more accurate comparison of SEE tolerance between device offerings
  - Eliminates bond-wire shadowing effects
  - Safe-operating area accurate for all lighter ions
- **Test Goals**
  - Define safe operating area, and/or
    - Increment V_{DS} between beam runs, until failure
  - Obtain SEB cross-section curves



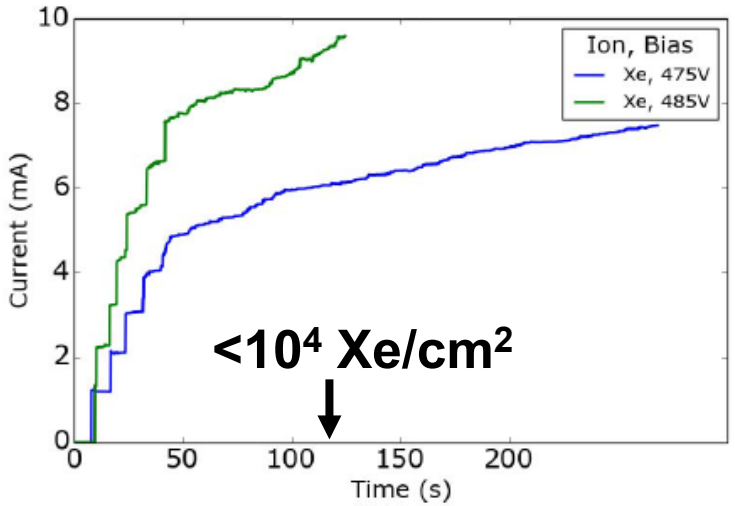
Li, Micromachines, 2019. CC BY 4 license

Silicon power MOSFET test methods are based on decades of test data and research into the mechanisms of failure in VDMOS

Silicon Carbide SEB Test Challenges



Witulski, IEEE TNS, 2018



Witulski, IEEE TNS, 2018

- **Ion-induced leakage current (I_R) can impact SEB susceptibility if SEB does not occur early in the beam exposure**
- **Achievement of test method fluence levels may not be possible, and may provide misleading data**

Difficult to obtain accurate SEB safe operating area

RHA Guidance: SiC Testing Recommendations

- **Ion beam selection:**
  - **Thinner epilayer means lower-energy ions can penetrate into the substrate**
  - **In addition to mission requirement conditions, consider lighter ion/lower LET tests to:**
    - Aid on-orbit risk assessments
    - Reveal differences between parts
- **Test fluence:**
  - **Dictated by test goals and degradation response of the device**
  - **Non-catastrophic damage can *increase* the threshold voltage of SEB**
    - Identification of the threshold voltage yielding the maximum cross section will be identified instead
  - **Rate of degradation of leakage current is not dependent on prior history**
    - Until the rate is no longer constant
- **Temperature:**
  - **Unestablished effects on SEB**
    - Impact ionization is hole-driven unlike in silicon
  - **Some data suggest non-catastrophic degradation rate increases with temperature**

RHA Guidance: GaN HEMT Test Recommendations

- **Ion beam selection**
  - **Safe operating areas (SOAs) can be identified**
    - Valid for the tested lot only
    - Part-part variability reduces confidence – larger sample sizes advised
    - Effects are LET-dependent; range should penetrate into the substrate
- **Sample and test setup considerations**
  - **Lot-specific heavy-ion testing is necessary until consistency becomes routine**
    - Each wafer is often one “lot”
  - **Packaging is designed for minimal inductance and maximum heat extraction**
    - Consider impact of decapsulation, wire-bonding, and restricted die access
  - **Susceptibility may depend on test circuit design and methods**
    - Voltage stress introduces defects: do not exceed rated voltage on the drain during post-rad characterizations
    - Gate structures have limited voltage ratings – minimize systematic transients
- **Temperature Effects are not established**

RHA Guidance: Risk Assessment

- **(Unvalidated) failure rate prediction methods developed for Si and SiC power devices may provide an upper bound**
  - Allow additional margin for uncertainty of SiC SEB voltage threshold
  - Consider that steradian window of vulnerability may change with voltage
    - see Javanainen, IEEE TNS, 2017
    - For risk-tolerant applications, margin and unpowered redundancy is advised
- **Non-catastrophic damage has unknown longer-term effects**
  - Extent of damage is part-to-part variable
  - Consider application temperature and functional lifetime requirements
    - For risk-tolerant applications, margin and unpowered redundancy is advised
  - Life tests of damaged parts may reveal higher-likelihood failure modes - sample size will limit discovery of rarer modes


NEPP
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