2.5/3D HI Packaging – Foundation and Future Vision

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NEPP

Package Type by Mission

Package Type Sampling of Recent and Future JPL Missions

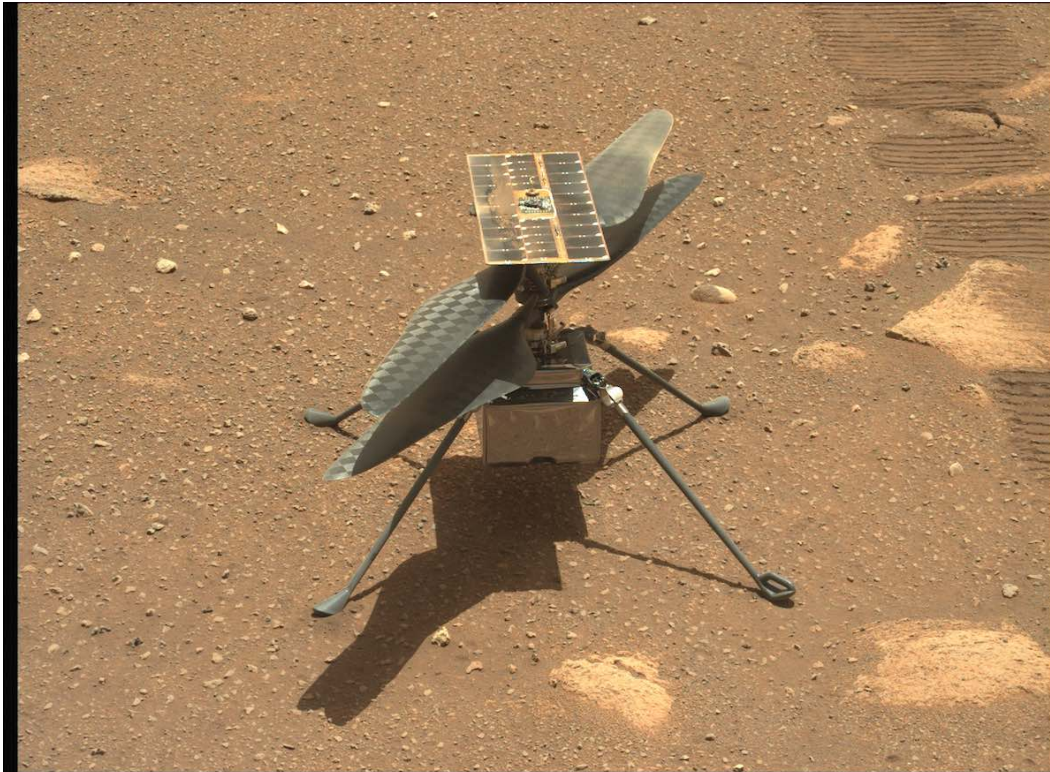
600
500
400
300
200
100
0

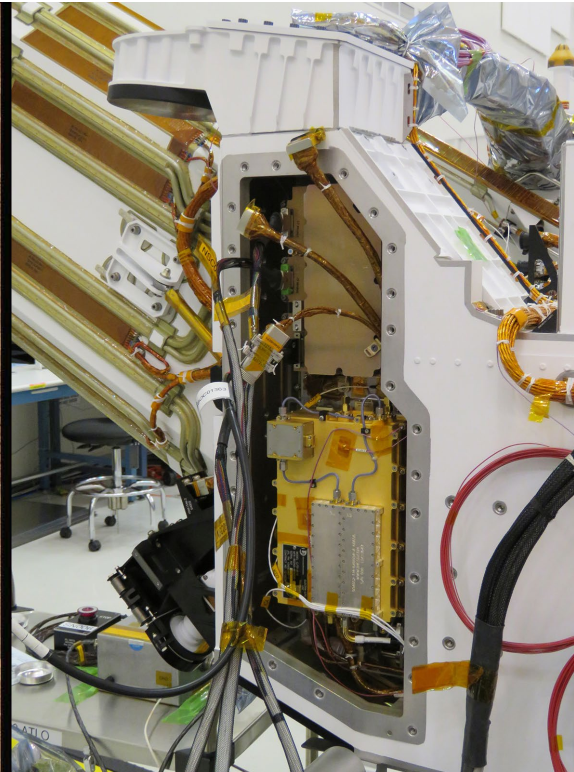
Mars 2020
Europa Clipper
MSL
NISAR
OCO2
Psyche
OCO-3
SWOT
ECOSTRESS
WFIRST-CGI
SPHEREx
GRACE FO
InSight

CGA DIP QFN QFP SOIC TSOP

- Heritage space grade DIP packages are still very common
  - Often > 10% of total
- Large heritage CGA devices are also very common
- QFPs are heritage and there are many heritage space parts using them.
  - Very common and very easily to handle for trained techs
- QFN usage is very limited but starting to increase on recent missions
  - QFNs are still coming up the manufacturing learning curve.
  - They require very good process control/design rules.
- TSOP usage dominated by memory devices
- One die per package almost exclusively

COTS PoP Packaging in Space





Snapdragon 801 PoP
28nm SoC + LPDDR3

- COTS packaging technologies are capable of meeting flight environmental requirements as-is in some cases
- Board level quality issues can dominate
- Support from Part manufacturer key to understanding infusion issues and providing technical support

Frequency, Hz	Flight Acceptance Level	Qualification/ Protoflight Level
20	0.01 g^2/Hz	0.02 g^2/Hz
20 - 40	+ 6 dB/oct	+ 6 dB/oct
40 - 450	0.04 g^2/Hz	0.08 g^2/Hz
450 - 2000	- 6 dB/oct	- 6 dB/oct
2000	0.002 g^2/Hz	0.004 g^2/Hz
Overall	5.6 Grms	7.9 Grms

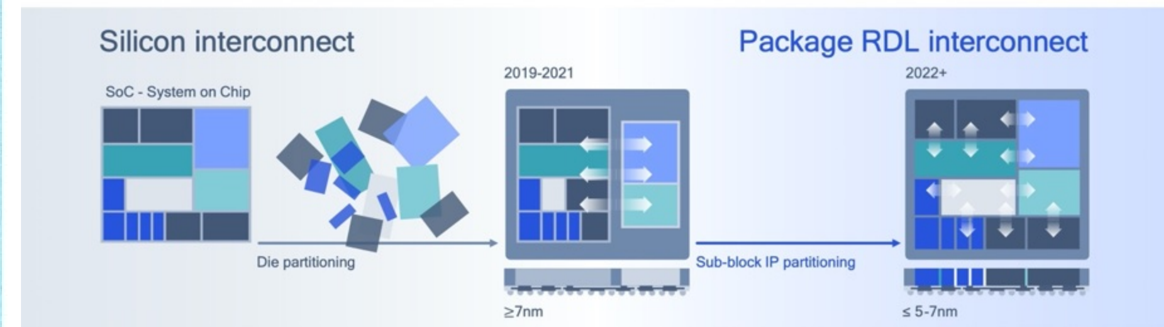
Mobile Phone Packaging Technology

1. Apple A11/DRAM (InFO PoP)
2. Samsung Flash (Stacked die)
3. Qualcomm MDM9655 BBP/Memory (stacked die)
4. Qualcomm WTR5975 TRx (WLP)
5. Skyworks GSM PA (SiP)
6. Skyworks 3G/4GPAD (SiP)
7. Broadcom 3G/4GPAD (SiP)
8. Skyworks Diversity Rx Module (SiP)
9. Skyworks Diversity Rx Module (SiP)
10. Qualcomm Envelope Tracker (SiP)
11. USI WLAN/BT Module (SiP)
12. Qualcomm PMD9655 Power Manager (WLP)
13. Power Manager (WLP)
14. Audio Codec (WLP)
15. Audio Amplifier (WLP)
16. Audio Amplifier (WLP)
17. Audio Amplifier (WLP)
18. Broadcom Wireless Charger (WLP)
19. TI Battery Charger (WLP)
20. NXP Display Controller (WLP)
21. NXP NFC Controller (WLP)
22. Bosch MEMS Accel/Gyro (SiP)

Figure 7: Apple iPhone X main board (source: Prismark Partners)

Next-generation SoC design in the 5G era

Integrates with all package technologies



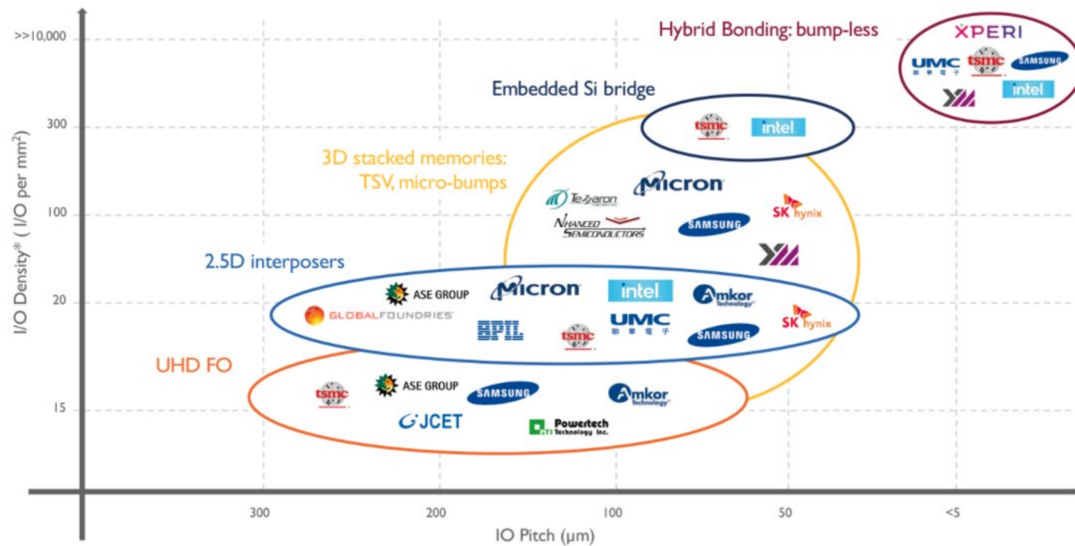
New architectures | New methodologies | New tools

https://eri-summit.darpa.mil

- Wafer Level, System in Package (SiP) or PoP are used exclusively
- Continued innovation to meet performance and cost goals
- Mobile is also a fundamental packaging driver

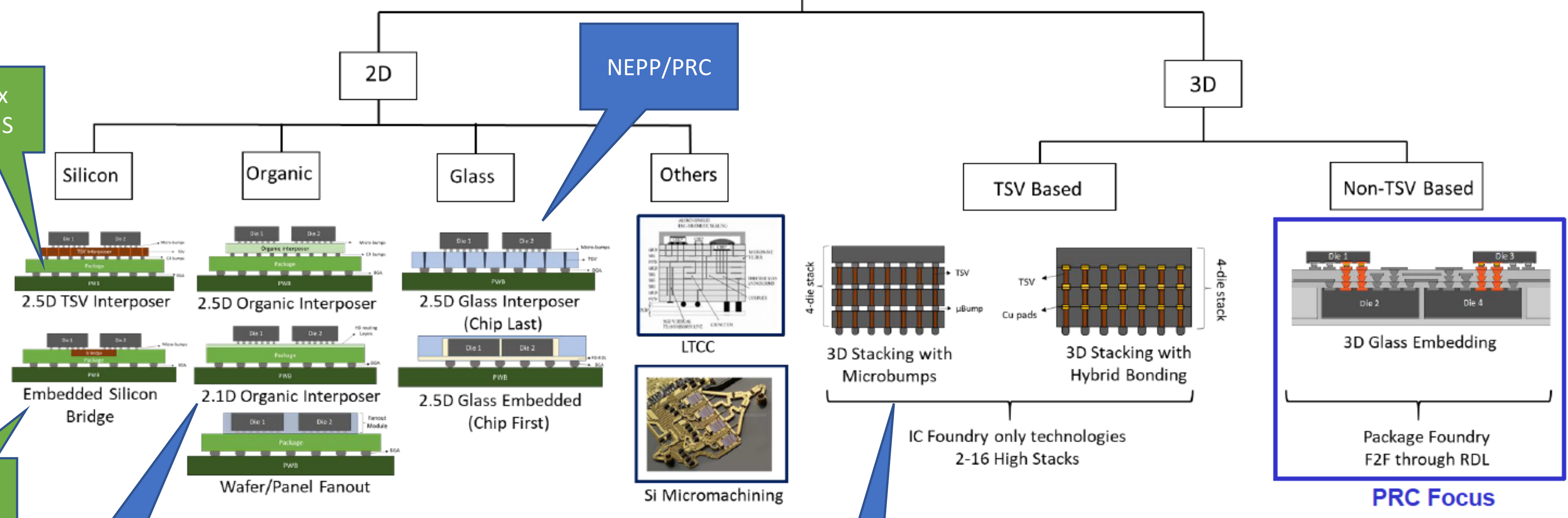
High Performance HI COTS Packaging Roadmap

http://www.yole.fr/Reports.aspx



- Packaging scaling factors:
  - Pitch:
    - Stacked die ubump
    - FC bump pitch
    - BGA Ball
    - I/O
  - I/O density
- Each new generation requires a new space qualification
  - New materials, processes, physics of failure
- High volume, large financial requirements to be competitive

NEPP HI Roadmap



- Combination of COTS evaluation along with custom technology evaluation
- Future collaborative path as several options
- Package foundry concept becomes option for space missions w/ PRC collaboration

NEPP/PRC Collaboration

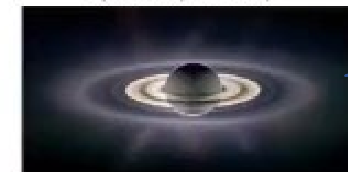
PRC – Application & System Driven Center

QC, AI & HPC (Neuromorphic ..)

Automotive (EV & Self Driving)

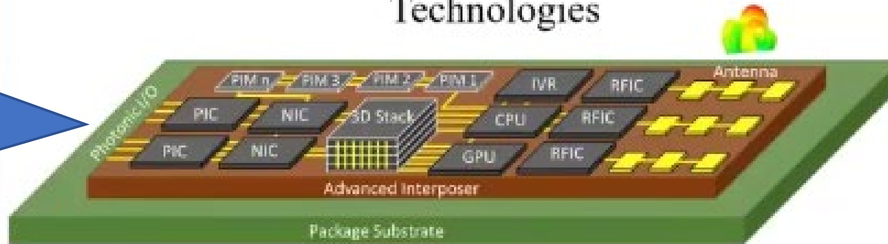
Wireless (5G/6G & Beyond)

Space (Harsh)



Mission & Extreme Environments

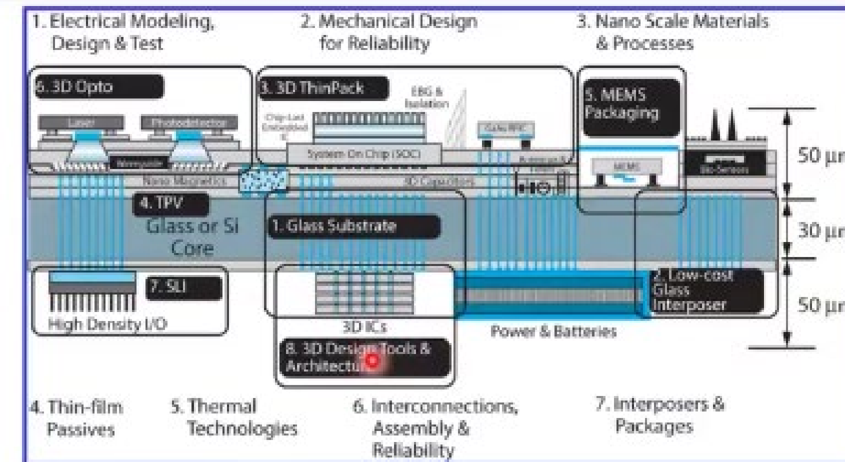
Computing, Communication, Sensing & Control Technologies



S. Ravichandran & M. Swaminathan, Heterogeneous Integration for AI Applications: Status & Future Needs, Microwave Magazine (to be published)

Packaging as the central unifier of technology efforts.

Opens the door for photonic packaging collaboration



Rao Tummala, McGraw Hill, 2019

Depth and breadth of PRC research and capabilities

❑ Advanced Packaging being used to enable Microelectronics Systems!

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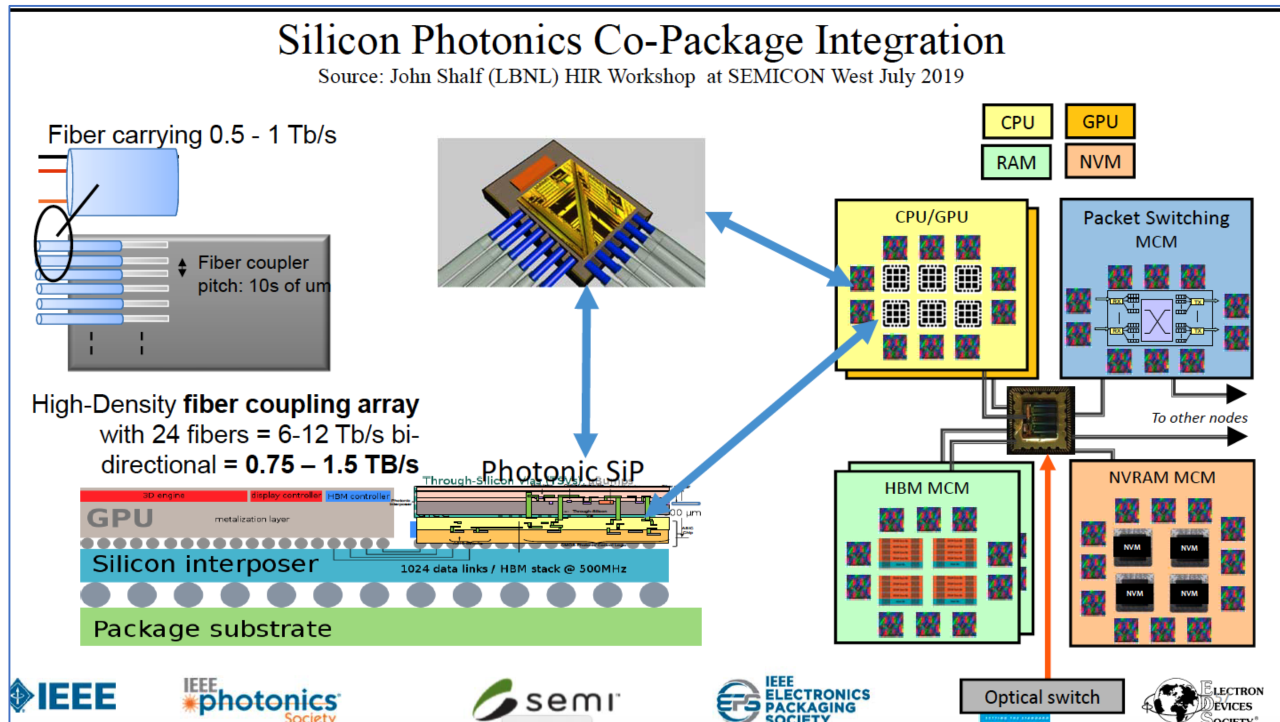
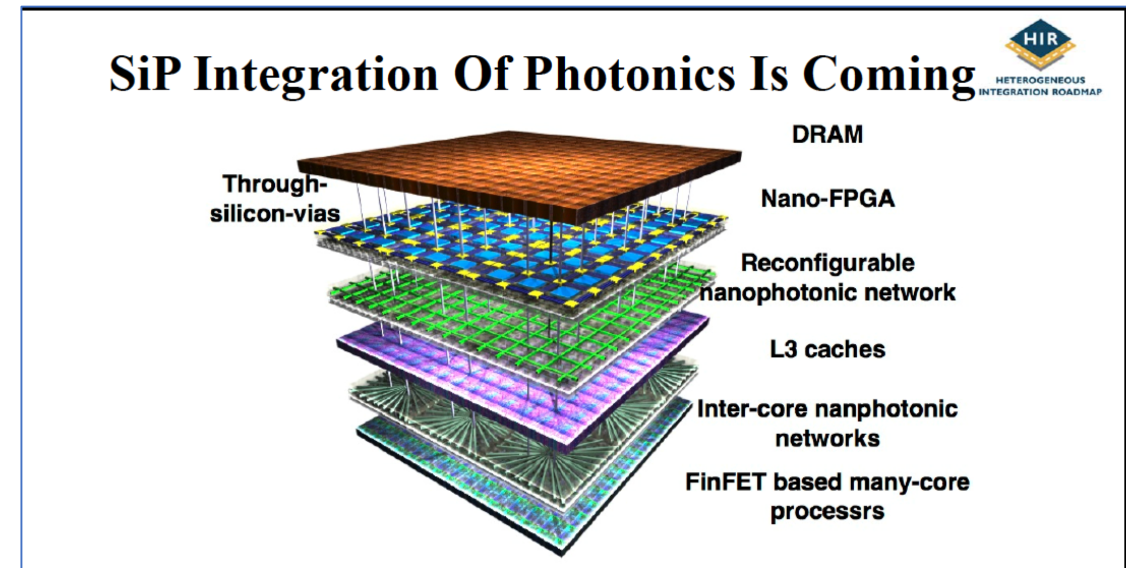
SiP with Electro-Photonics Technologies



https://eps.ieee.org



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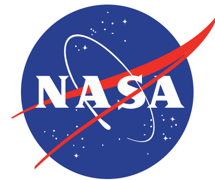
Game Changing Technology Opportunities for NASA/JPL missions

Integrated Photonics can have profound impact both in the flight computers as well as science instruments

NEPP HI Packaging Roadmap

- **GT PRC**
  - Glass Interposer and 3D Glass embedding for SWaP enhanced space SiP
    - Support and evolve Packaging Foundry concept for NASA/JPL missions
  - Industry partner outreach for characterization of shared technology for space environments
    - Extreme environment physics from COLDTech/Ocean Worlds Life Detection
- **EPICA - Electronic-Photonic Integrated Circuits for Aerospace**
  - GT/VU/UCF NSF funding IUCRC for integrated photonics and electronics in communication and sensing applications
- **COTS Packaging Technology**
  - Opportunistic characterization in support of mission interest and standards development
  - Failure mode identification and scaling analysis

NEPP



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