2.5/3D Packaging Technology Challenges for Space Components

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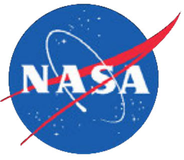

Presentation Overview

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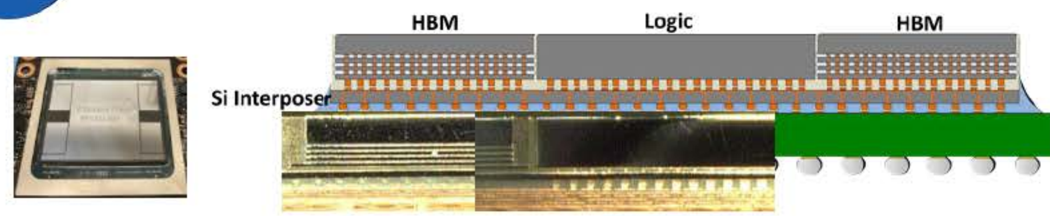
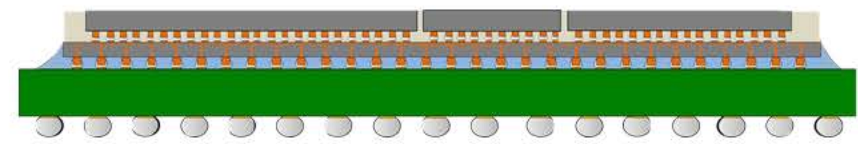
- 2.5/3D packaging process and materials are more sophisticated than in the traditional flip chip packaging technology.
  - The industry mainstream SoA 2.5/3D package assembly process, materials, and business model are not currently compatible with low-volume production for mil/space components.
  - Future mil-spec may have challenges in reflecting the potential materials and screening issues unique to 2.5/3D packaging.
- This talk will introduce some of the challenges and NEPP's approaches to address them.

Introduction

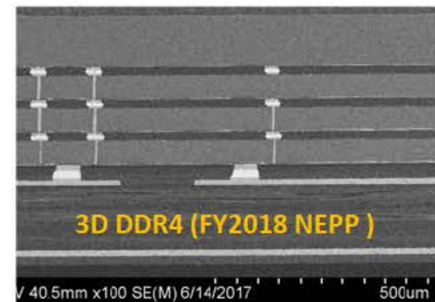


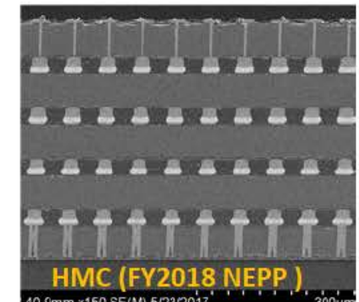


- 2.5/3D packaging
  - Uses interposer and/or stacked dies.
    - Short signal length. High bandwidth between dies (high I/O density).
  - Interposer to overcome the feature size limitation of organic substrate when integrating dies
    - Organic substrate cannot provide small enough feature sizes (line width/space, bump pitch, via diameter/pitch).
      - *EMIB and fan-outs are developed for the same reason.*

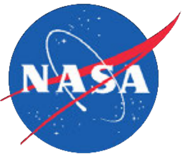
**Dies can be integrated on organic substrate, if high I/O density is not required.*

  - Technology drivers :
    - High bandwidth between the processor and the HBM.
    - Integration of dies and chiplets with diverse IPs.
    - Improvement of yield by integrating smaller segments of die (Virtex 7).
- 2.5/3D Packaging Technology Challenges
  - In the following slides, some of the challenges in 2.5D/3D packaging technology relevant to space applications will be discussed.
    - Die attach process and materials
    - Package assembly processes and their implications for low-volume production.

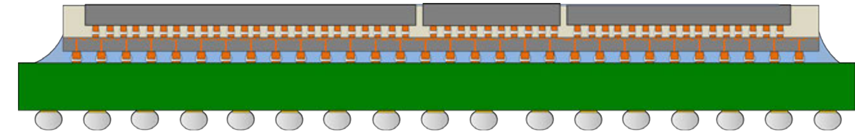




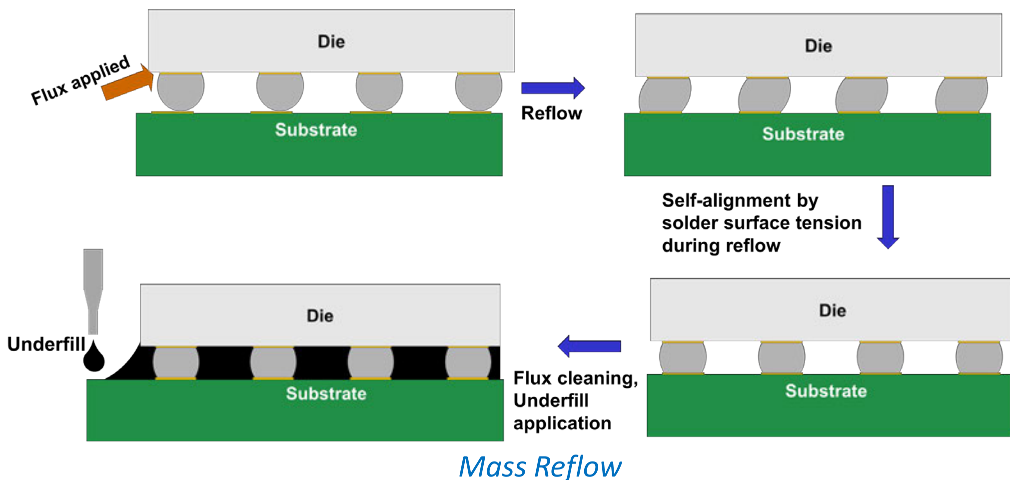
	Organic Substrate	Si Interposer
Trace Line Width (µm)	9~15	~0.5
Trace Line spacing (µm)	12~15	~0.5
Via Diameter (µm)	50~65	0.4~2
Via pitch (µm)	100~125	<40
Core/TSV/TGV via diameter (µm)	300	~10
Core/TSV/TGV via pitch (µm)	1000	~40
Bump pad pitch (µm)	120~150	~40
IO density (IO/mm/layer)	<50	> 1000



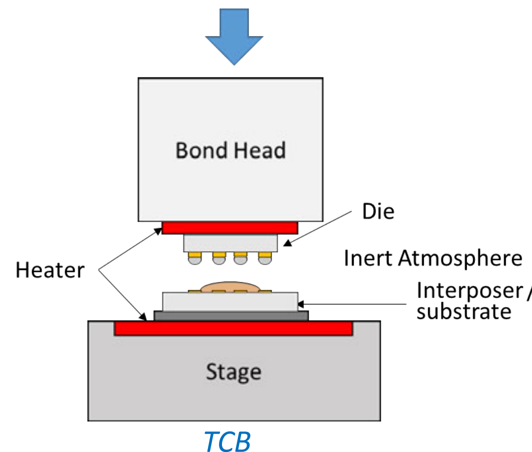
Die Attach Process



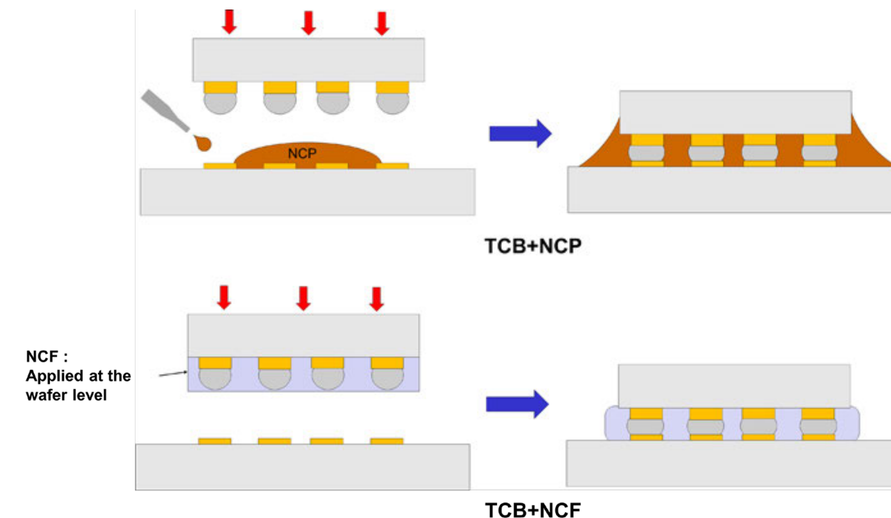
- Conventional mass reflow (MR) process
  - For conventional flip chip packages.
  - Major variables : Reflow profile (Time-temperature profile)
  - Low ramp rate (<1°C/sec average). Reflow process takes a few minutes.
  - Capillary underfills are applied after die attach.
- Thermocompression/Thermal-compression bonding (TCB) process :
  - Preferred for bump pitch below 100µm. Necessary as bump pitch approaches 50µm.
  - Can meet the finer die placement accuracy for microbumps (≤2µm capable). Can accommodate thinned dies that would warp.
  - High ramp rate (~100°C/sec). Process completes within a few seconds.
  - Variables : Stage temperature, bond head time-temperature profile (ramp, contact, peak, release, cool), contact & bond force, bond head displacement, dwell time
  - Use of non-conductive paste (NCP)/ non-conductive film (NCF) instead of underfill for fine-pitch bumps
    - NCP/NCF is applied before TCB.
    - NCP/NCF cures within seconds during TCB process.
      - Properties of NCP/NCF changes during TCB in real-time during bonding.
    - Use of NCP/NCF can create unique defects and packaging challenges



Mass Reflow



TCB



NCP / NCF Packaging Challenges (1)

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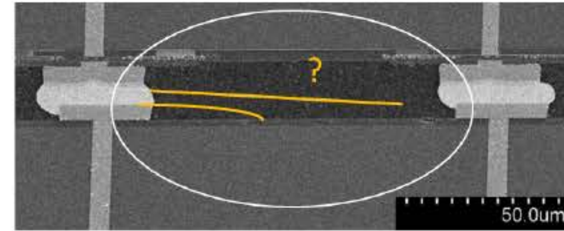
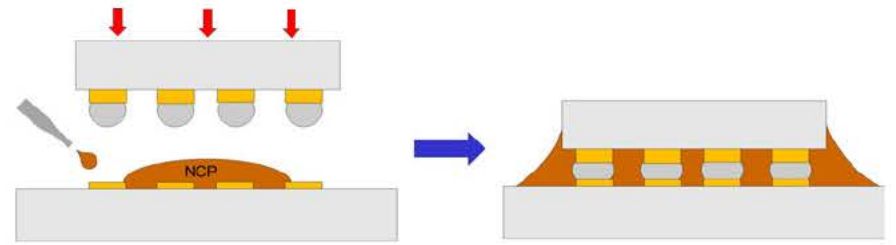
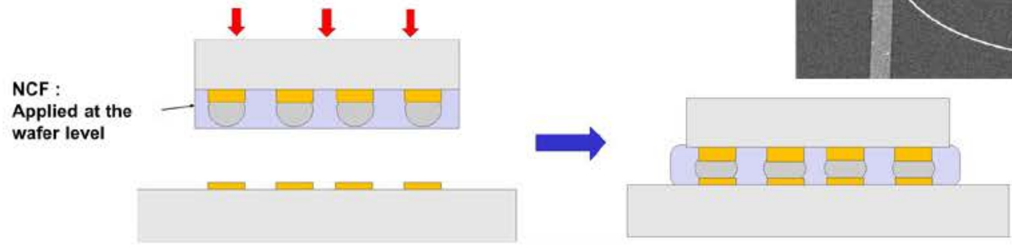
- Why use non-conductive paste (NCP)/ non-conductive film (NCF) instead of capillary underfill (CUF)
  - Fine pitch microbumps make flux cleaning and underfill flow not easily feasible.
    - Flux residue can hinder CUF flow between bumps, creating voids. Underfill void can reduce solder joint reliability.
      - ** MIL-PRF-38535 does not have a specific accept/reject criteria for underfill voids. (Having underfill void does not violate the spec).*
      - *- But microbumps are Pb-free. Your customer or auditor: "Are you sure you won't have the whisker issue?"*





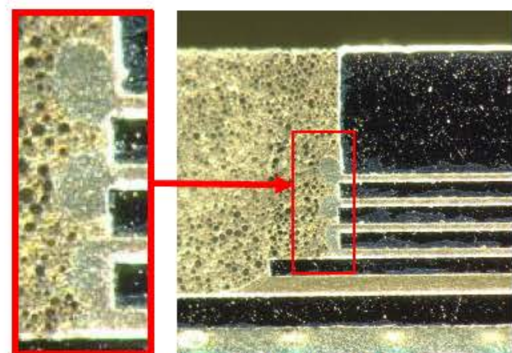
TCB+NCP



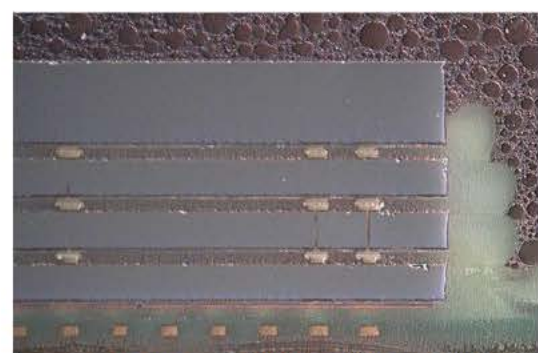
TCB+NCF

- NCP
  - Typically has fluxing capability
  - Fillet length is longer and more difficult to control than NCF.
  - Pre-applied prior to TCB process.
  - Die proximity limit
    - Die proximity for short signal length/high bandwidth

- NCF
  - Typically has fluxing capability
  - Fillet length is short. Dies can be put very close to each other.
  - Applied at the wafer level. Comes with die. B-stage material.
  - Die with NCF will have a shelf life. :
    - *Need a clever die distribution network or new material & process*

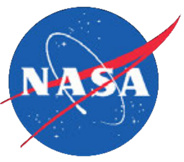


HBM in a Nvidia CoWoS package



3D DDR4 with NCF (FY2018 NEPP task)

- Fluxing capability
  - Materials may not meet outgassing requirement.
    - If the quantity of material is only in the range of 10s of mg max, how critical is the outgassing? (providing that long-term outgassing doesn't hurt the reliability.)



NCP / NCF Packaging Challenges (2)

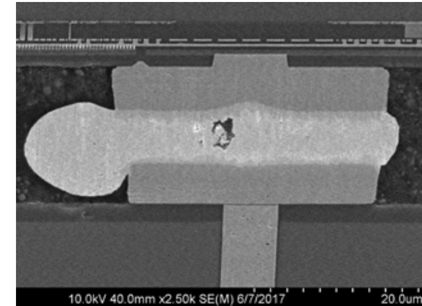
- Solder bumps can have defects that do not exist in the MR+CUF process

  Ex) Entrapment of NCP, NCF, or filler. Solder voiding.

  - It would difficult to consistently produce defect-free packages for typical low-volume manufacture.
    - Multiple dies with different bump geometry, die size, low-k, etc in the same package.
    - Large number of bumps.
  - <u>Screening challenge</u>
    - Defects are too small to see in non-destructive inspection tools (x-ray or CSAM).
    - The failure condition will depend on bump pitch, die size, type of defect.
      - Depending on the stack-up above/below the defect, the defect can be benign.
    - These defects may pass the screening tests in the current mil-prf-38535 but potentially cause early failure.

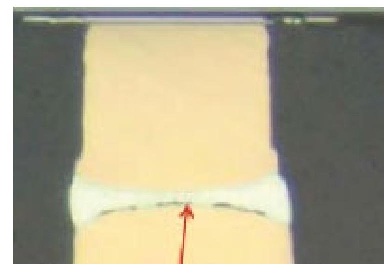
      ex) TM 1010, condition C 10 cycles minimum. TM1010 condition B 15cyc minimum.

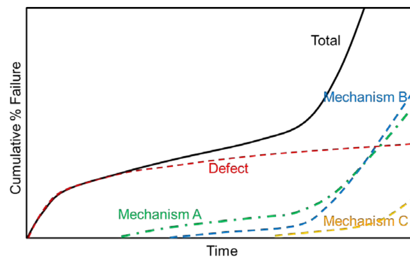
      - The screening tests in the current 38535 may not be effective in screening out the early failure by these defects.

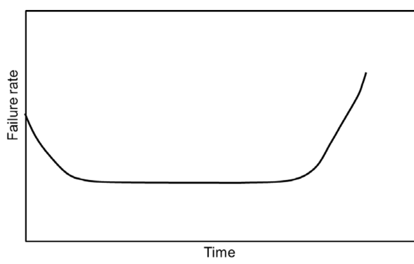


Benign defect in a 3D DDR4 (FY18 NEPP task)

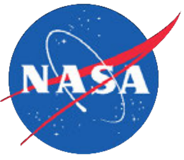
Y.M. Cheung, Dewen Tian, Giuseppe Y. Mak, and Ming Li, EMAP 2013





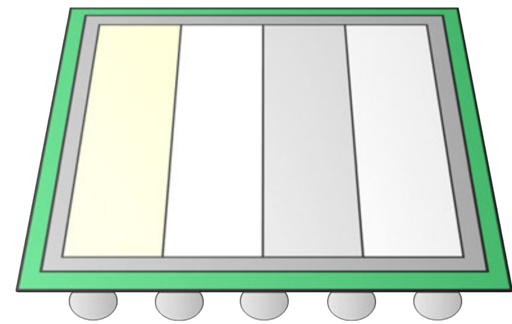


Lei Yang, Dewen Tian, YM Cheung, and Ming Li, EPTC 2015



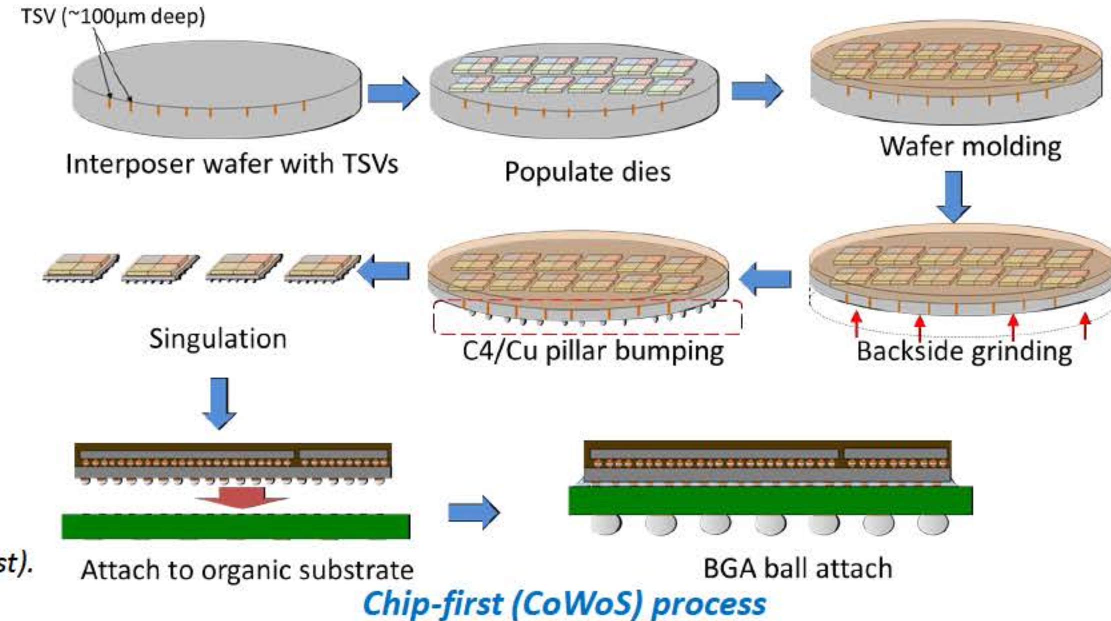
Is the TCB +NCP/NCF process absolutely unavoidable for small pitch ?

- Virtex-7 (V7) packaging
  - V7 was the first commercially available 2.5D package product.
  - A Xilinx presentation and paper imply that V7 used CUF (and possibly MR).
    - 45µm pitch microbump, 300µm thick 7x12mm dies, 100µm thick interposer
    - Optimization of routing layers and backside passivation
      - *Ivo Bolsens "2.5D ICs: Just a Stepping Stone or a Long Term Alternative to 3D? (https://www.xilinx.com/publications/about/3-D_Architectures.pdf)*
      - *Raghunandan Chaware; Kumar Nagarajan; Suresh Ramalingam, "Assembly and Reliability Challenges in 3D Integration of 28nm FPGA Die on a Large High Density 65nm Passive Interposer", 2012 ECTC*
  - *With "enough" engineering, MR+CUF is feasible for 2.5/3D devices.* *..(Dies may have to be thick enough)*



Package Assembly Processes

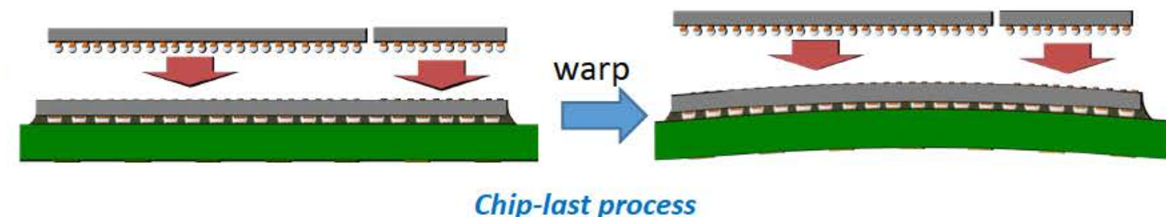
- Known good die
  - The current industry practice is to integrate known good dies.
    - Integrating multiple dies : ‘weakest link’ situation (if one die fails, all fails).
  - There is no standardized definition of known good die.
    - There will be a SAE working group
    - Using KGD defined by die suppliers and performing a robust electrical test at the package level can be another option.
- Package assembly process : Chip-first vs Chip-last
- Chip-first
  - The current mainstream process
  - Provided by big companies, such as TSMC.
    - TSMC CoWoS: Attaches dies to unfinished interposer wafer
      - Handing thinned interposer wafer is difficult
    - *Amkor CoW attaches dies to a finished&bumped interposer wafer (Categorized as chip-last).*
  - May not be suitable for low-volume manufacturers.
    - In-house : High investment cost to develop the capability
    - Contract out : Small quantity order to big companies
      - New business model needs to be developed to accommodate low volume production.



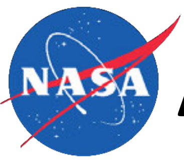
Chip-first (CoWoS) process

- Chip-last
  - Potentially more suitable for low-volume manufacturer
  - Yield challenges from interposer handling and warping
    - Requires engineering know-how for warpage control

ex) Amkor CoS.



Chip-last process



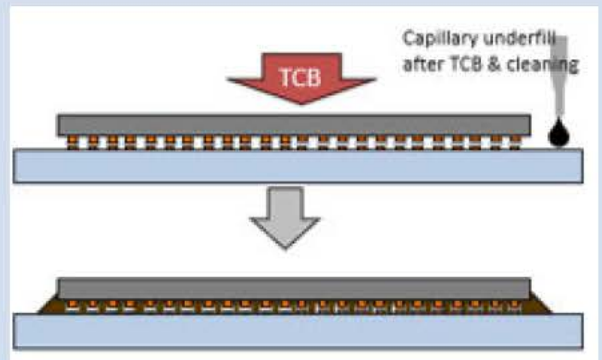
Advanced Substrate Technologies for Low-volume 2.5/3D Packaging

- Role of Si interposer : to overcome feature size (I/O density) limitation of organic substrate.
- If substrate can provide high enough I/O density, interposer is not needed.
  - Can reduce the yield issue from warping.
  - Glass (GaTech consortium – current NEPP task)
    - Glass substrate can provide high enough IO density
      - *IO density can be comparable to currently available SoA commercial 2.5/3D products.*
    - Potential additional advantages in optoelectronic/photonic and RF applications.
  - Organic substrate suppliers
    - Shinko i-THOP *Calls this technology "2.1D or 2.3D " to differentiate from the existing 2D technology.*
    - Kyocera is also making efforts
  - Other benefits : low cost and easy supply chain management

	HTCC Substrate	Organic Substrate	Glass Substrate	Si Interposer
Trace Line Width (µm)	100~125	9~15	1.5~5	~0.5
Trace Line spacing (µm)	100~125	12~15	2~5	~0.5
Via Diameter (µm)	125~200	50~65	2	0.4~2
Via pitch (µm)	250~640	100~125	20	<40
Core/TSV/TGV via diameter (µm)		300	>25	~10
Core/TSV/TGV via pitch (µm)		1000	>50	~40
Bump pad pitch (µm)	~250	120~150	20~40	~40
IO density (IO/mm/layer)		<50	100~500	> 1000

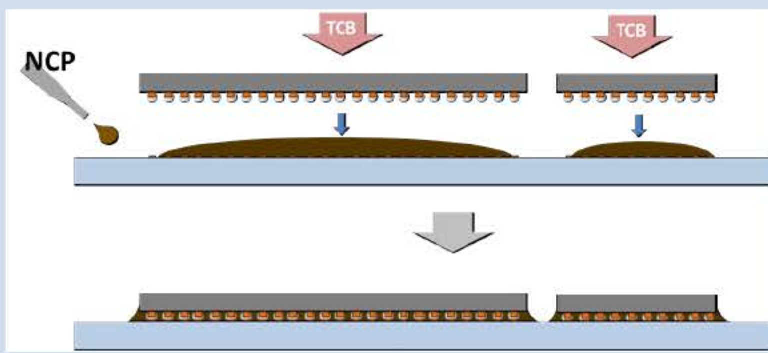
NEPP Glass 2.5D Package Study with Georgia Tech Packaging Research Center

Phase 1 (Current): Baseline Reliability for 50µm TCB Bumps without NCP/NCF Process Defects



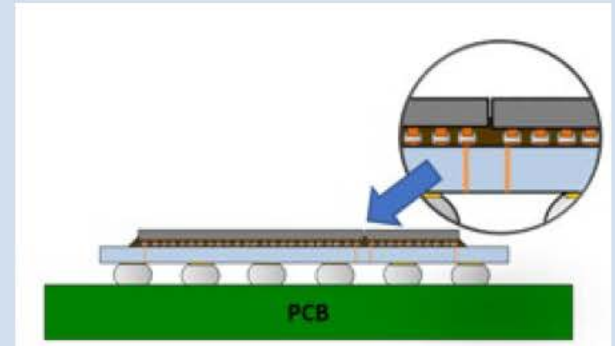
- 50µm pitch TCB bumps at periphery of the die
- CUF instead of NCP
  - Since the bumps are only at the periphery, it's feasible to clean the flux.
- Thermomechanical modeling.
- Thermomechanical reliability tests in MIL-PRF-38535 and JESD47
- NCP + TCB process optimization for the phase 2 task in parallel

Phase 2 : 40~80µm Bumps With NCP TCB



- 40~80µm pitch bumps. Full array.
- NCP + TCB
- Multiple dies
- Thermomechanical modeling
- Thermomechanical reliability tests in MIL-PRF-38535 and JESD47
- Effects of TCB+NCP process defects
- Process know-how on defect and fillet control

Phase 3: Effect of package warping and TGV reliability.



- Glass substrates are thin. When attached to PCB, the substrate will warp during thermal cycling.
- Effect of the actual stack up needs to be understood.

- **Georgia Tech team**
  - Profs. Suresh K. Sitaraman, Vanessa Smet, and Swaminathan Madhavan
  - Drs. Mohan Kathaperumal and Jack K. Moon
  - Trilochan Rambhatla and Amiri Savage

Long Term Goals and Phase 1 Test Vehicle Status

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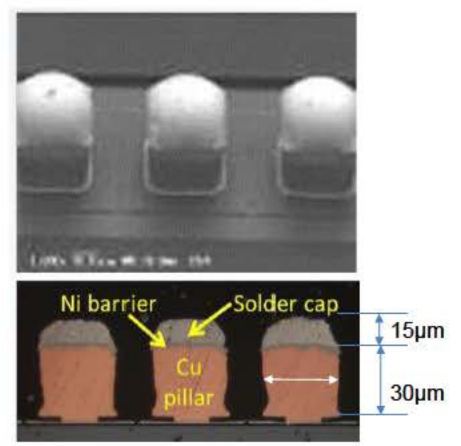
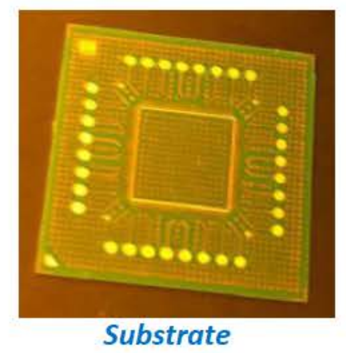
- Long term goal
  - Design principle/rules
    - How to optimize between die-level and board-level reliability?
      Ex) Low glass CTE : good for die-level. High glass CTE : good for board level. Die size? Glass thickness?
  - Package assembly challenges around TCB process
    - Reliability issues associated with TCB process.
    - Effect of defects, geometry, warpage, and materials.
    - Assembly process know-how for defect control and yield.
    - Screening condition for bump/package defect.
      - Is it possible to develop a predictive model for defect causing failure?
      - Should there be pass/fail criteria based on bump geometry and geometry?
      - Effect of board-level assembly reflow on TCB bump defects
- Phase 1 test vehicle
  - To establish baseline reliability data for 50µm bumps without NCP/NCF process defects
  - Develop analytic model for reliability
  - Sample production in progress

Die Size	7.3 mm x 7.3 mm
Die Thickness	725 µm
Pad pitch	50 µm
Bump	ϕ25µm Cu with solder cap
Bump height	Cu30µm+SnAg15µm
Substrate size	20 mm x 20 mm
Glass Core Thickness	200~300 µm
Glass CTE	3.8 ppm/C
Underfill	CUF

Solder resist	~15 µm	SR-FA
Copper pattern	~8 µm	Copper
Dielectric	~15 µm	ABF GX-92
Glass Core	200~300 µm	Low CTE glass
Dielectric	~15 µm	ABF GX-92
Copper pattern	~8 µm	Copper
Solder resist	~15 µm	SR-FA





Substrate

Initial Analysis Results

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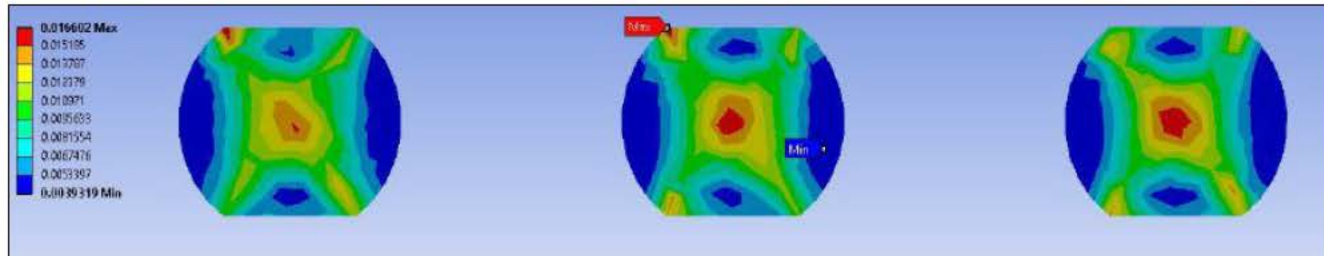
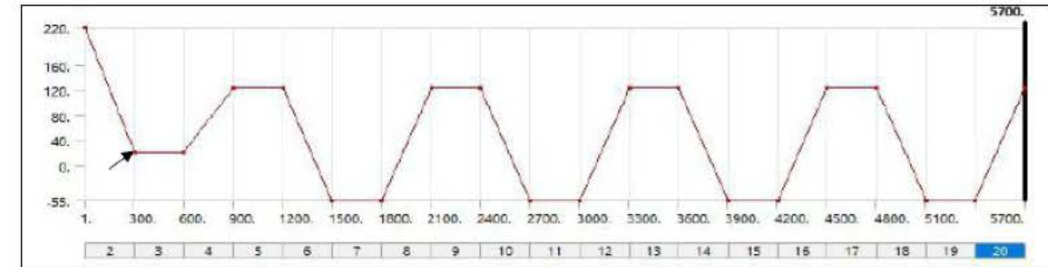
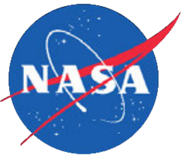
- Both elastic and viscoplastic behavior of solder joints were included in the model
- Hysteresis of solder joint stabilizes after 4th cycle in -55 /125°C cycle
- Underfill effect is not included yet.
- The mean predicted life is greater than 1800 cyc in TM1010 condition C, without underfill.
    - This is initial result. Does not reflect the exact bump geometry.
    - Underfill will be included.
    - Long term property change and degradation associated with thermal aging may need additional study.





Temp Range	Considered Strain Region	$\Delta\varepsilon_p$	α	C	N_f
-55 to 125 °C	Absolute max occurs at the corner	0.0166	0.93	21.9	2266
-55 to 125 °C	Area- averaged strain at corner	0.0159	0.93	21.9	2373
-65 to 150°C	Absolute max occurs at the corner	0.0199	0.93	21.9	1816
-65 to 150°C	Area- averaged strain at corner	0.0186	0.93	21.9	2001

Trilochan Rambhatla,
Prof. Suresh Sitaraman,
Georgia Tech



Summary

- 2.5/3D packaging requires different packaging materials and process than the traditional flip chip packaging.
- There are challenges for space component industry regarding the materials and process
  - Materials issue
    - Die shelf life for dies with NCF
    - Potential outgassing of NCP/NCF
  - The current screening condition may not be applicable for 2.5/3D devices
  - Process issue
    - Chip-first : Currently not suitable for low-volume production
    - Chip-last : Potentially suitable for low-volume production, but has potential yield challenge
- Advanced substrate technology, such as glass substrate, can potentially enable low-volume space component manufacturers to easily produce 2.5/3D packages.
- NEPP is working with GeogiaTech Packaging Research Center consortium to study glass substrate package for 2.5/3D packaging.
  - Samples for the 1st phase study are being produced. Analysis is also being performed.