

M2020/NEPP TCL Evaluation

for Electronics Packaging

TCL= Thermal Cycle Life

by

Reza Ghaffarian, Ph.D.

NASA-JPL-CalTech

(818) 354-2059

Reza.Ghaffarian@JPL.NASA.gov



Copyright 2021California Institute of Technology Government sponsorship acknowledged

NEPP Electronics Technology Workshop (ETW 2021) June 14-17, 2021, NASA GSFC- Virtual

http://nepp.nasa.gov



Outline

Electronics Packaging Technologies Evaluation

- > NEPP : Standard COTS and Advanced New BGAs/CGAs
 - > Generic/standard thermal cycle life (TCL) Evaluation
- > M2020 : Standard and Advanced
 - > Standard TCL, but short
 - > Standard TCL environmental control, but long
 - > Specific Martian environment short and mostly long
- M2020/NEPP link via Standard TCL especially instrument/Technology demonstration, knowledge for specific

> M2020/NEPP TCL Standard Environment

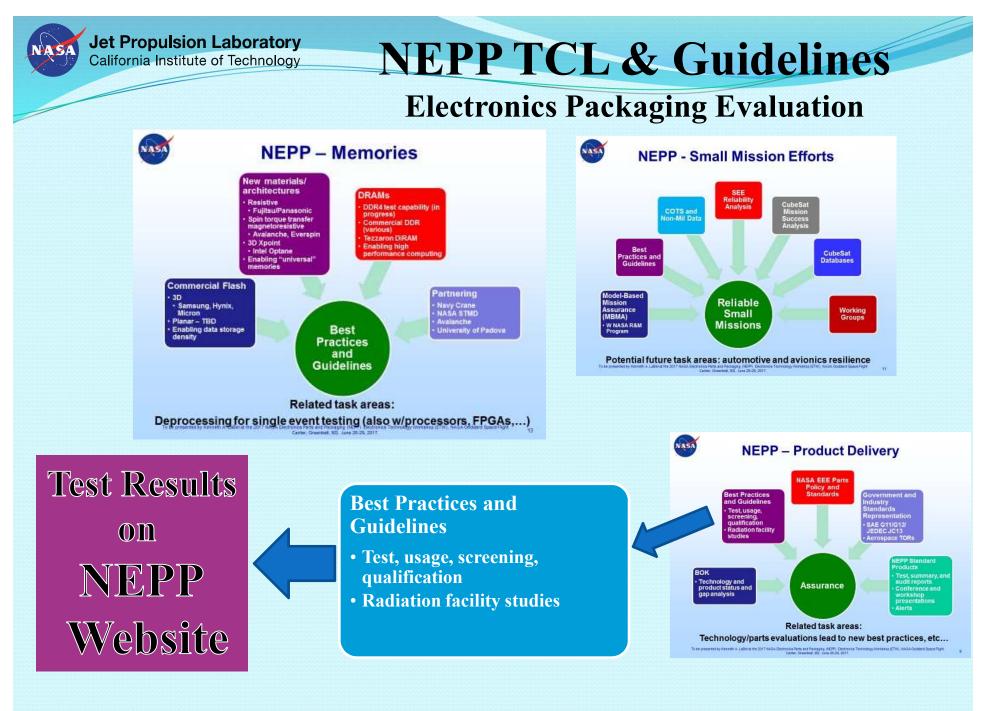
- Technology demonstration Control Environment
- > 3D Stack design/part developed under NEPP task
- > Built 5 partially populated assemblies for M2020 funded by project
- > Subject to TC standard environmental requirement
- > TC results for single- and double-sided assemblies
- Fully populated assemblies under NEPP task

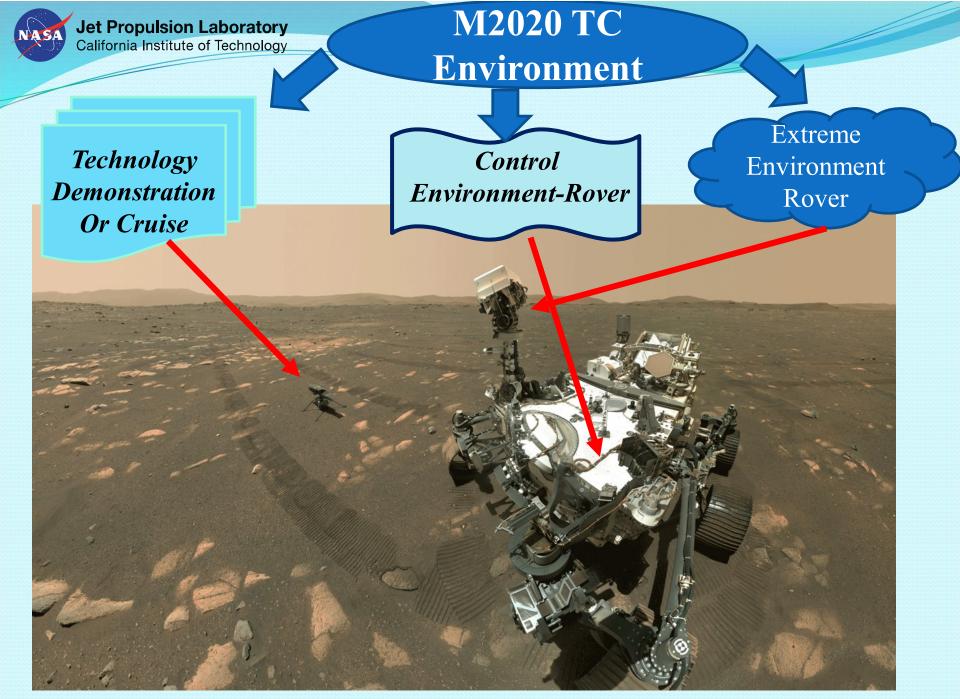
Unique Martian Environment

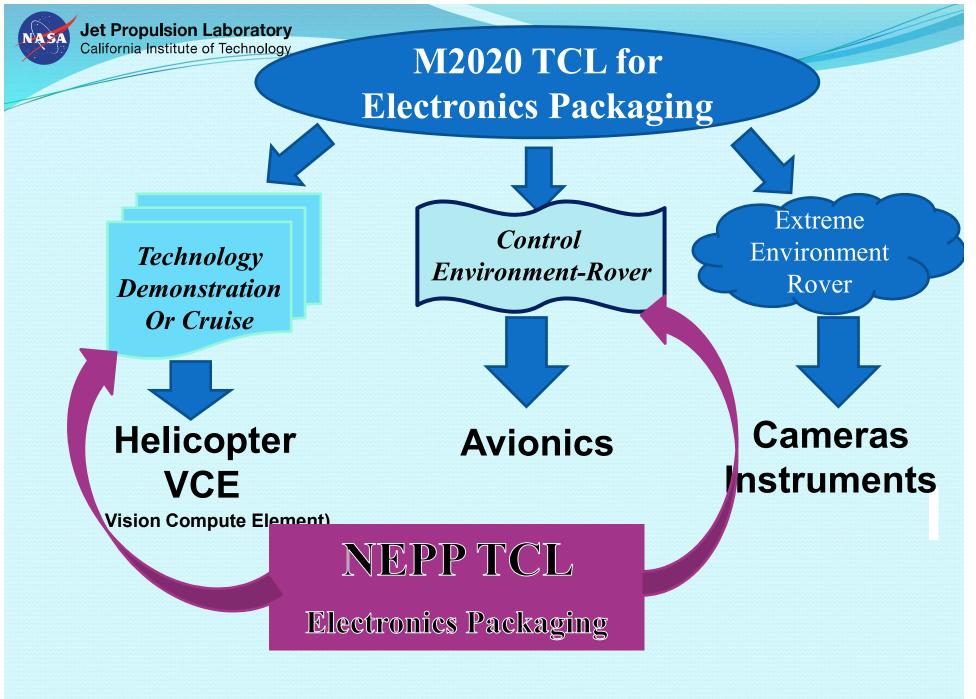
- > PGA, first attempt & physics of failure (PoF) under extreme cold TC
- > Pin height increase and PoF under extreme cold TC
- > Author's proposed robust approaches via bonding & test verification

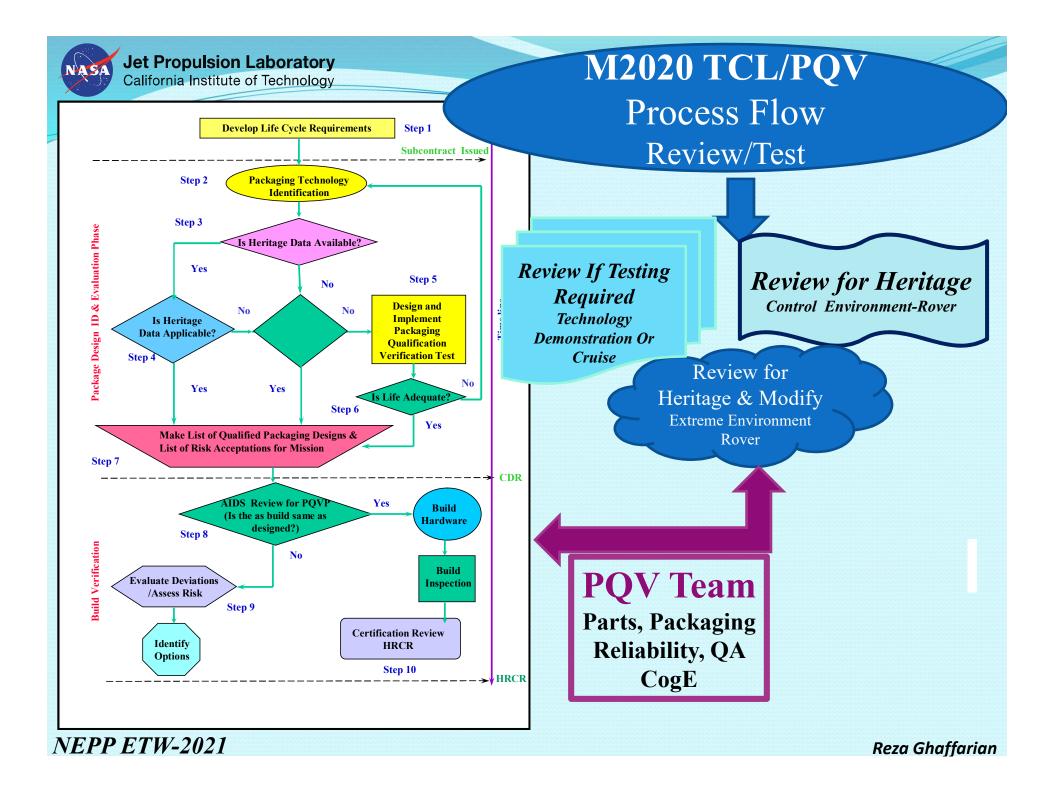
➤ Summary

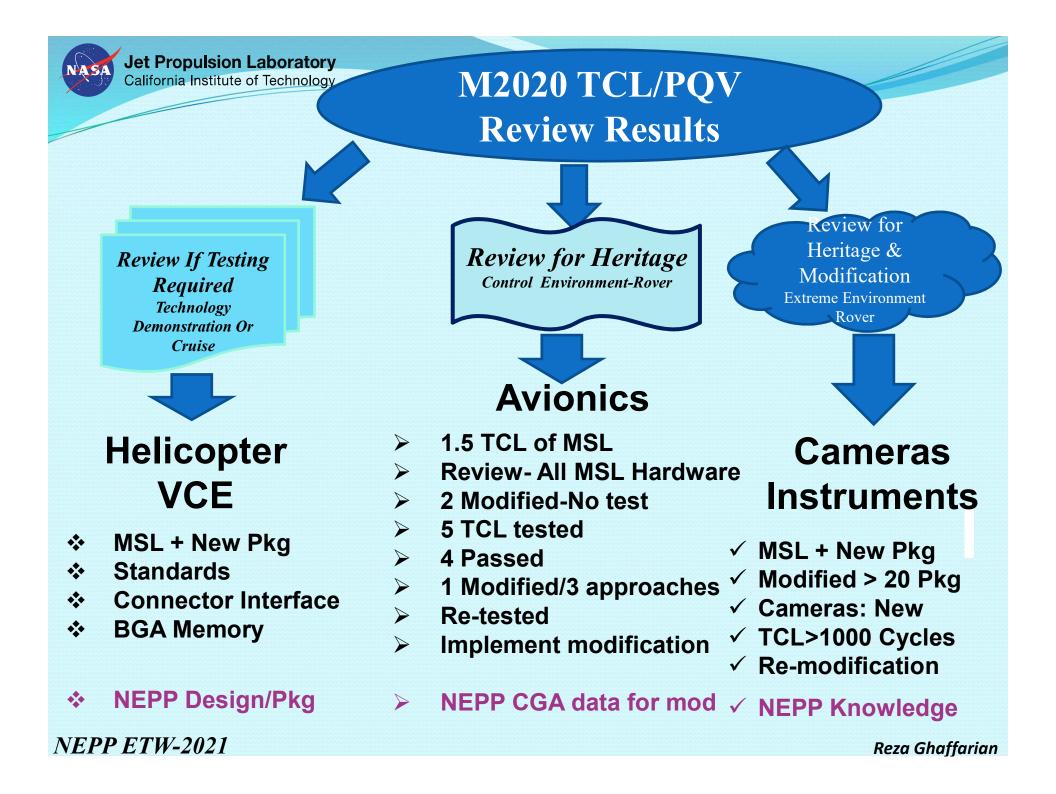
NEPP ETW-2021

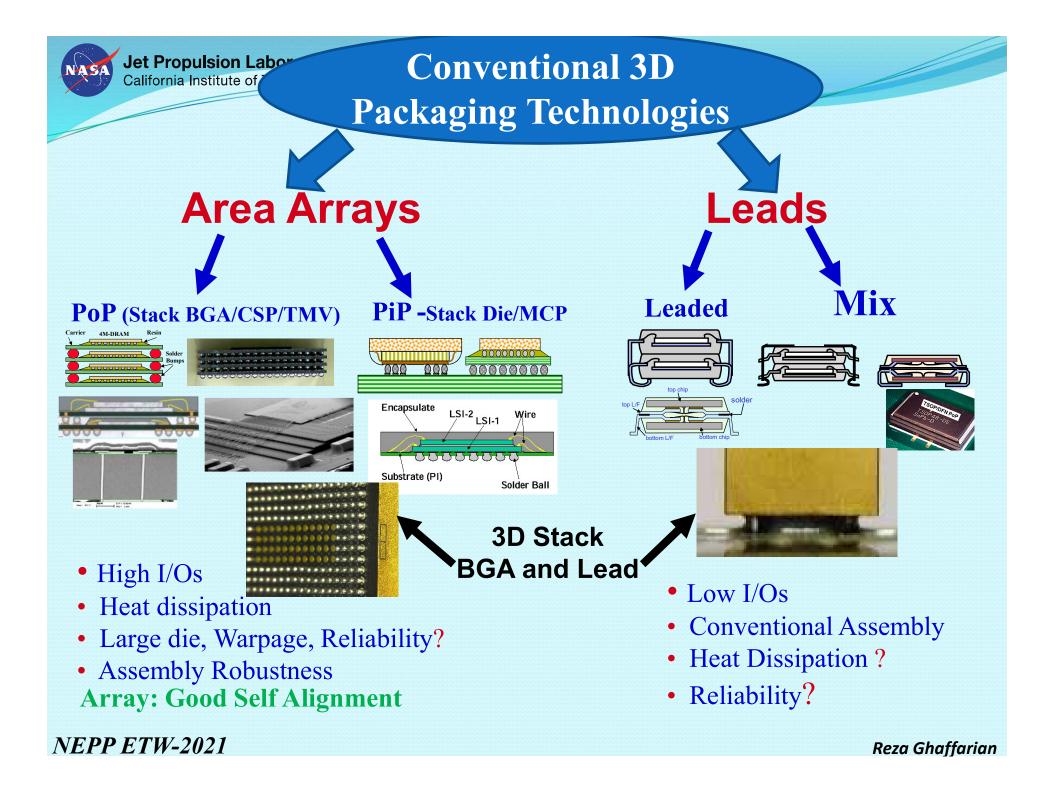














3D Stack BGA M2020 & NEPP

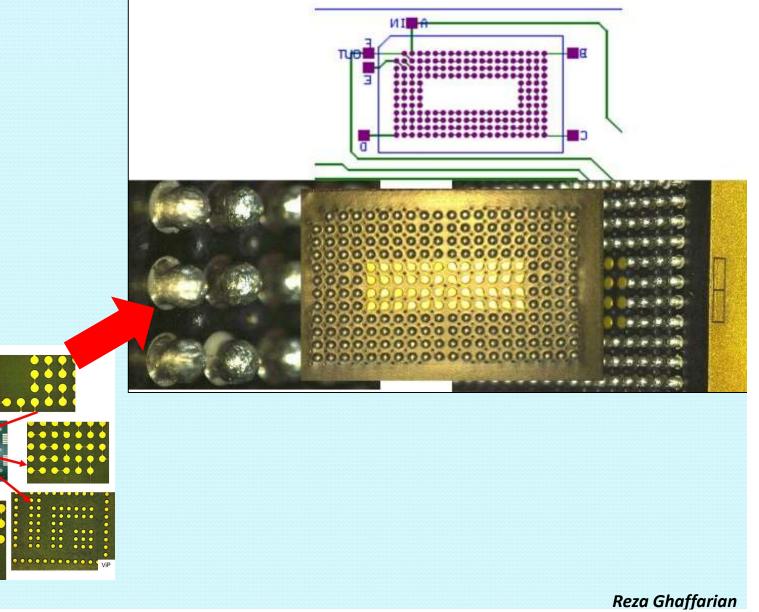
- PCB designed under NEPP
- Test matrix covered 3D Stack & BGA daisy-chain
- M2020 VCE required TCL evaluation
 - Funded to build 5 assemblies, one double-sided
 - HASL surface finish, SnPb Solder Paste
 - Thermal cycle, $TC = (-55^{\circ}C/100^{\circ}C)$
- NEPP for additional build/TC/Failure Evaluation

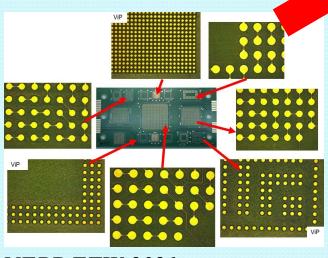


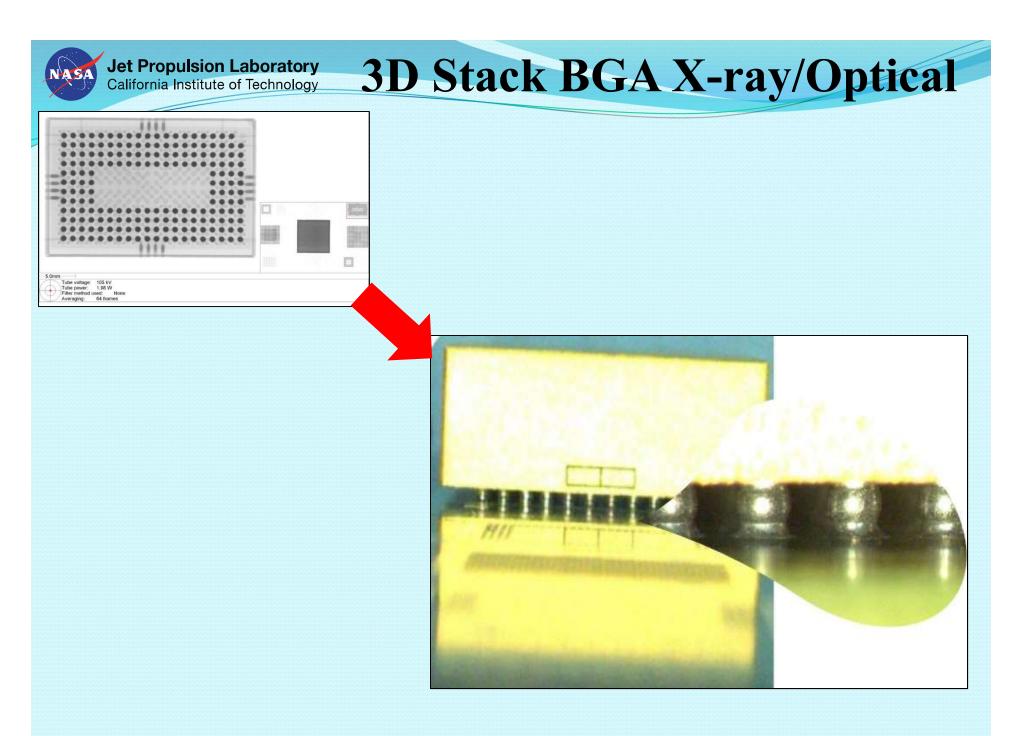
NEPP ETW-2021

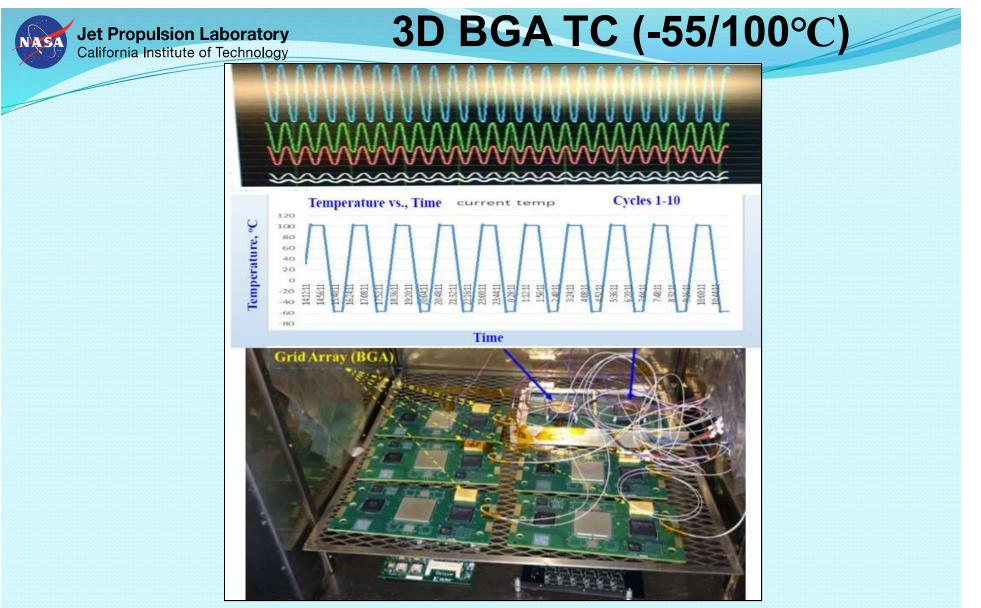










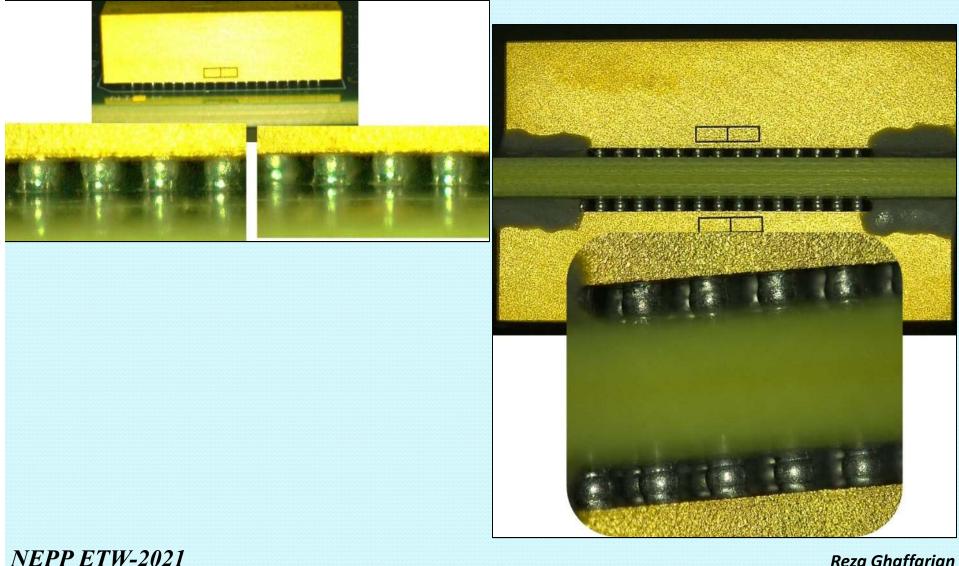


Representative of thermal cycle test profile (-55°C to +100°C) (top bottom), daisy-chain resistance changes with cycling (top rows), and single zone thermal cycle chamber (bottom). Chamber is fully loaded with five 3D stack BGA Assemblies, one double sided, which is shown by yellow arrows. NEPP ETW-2021

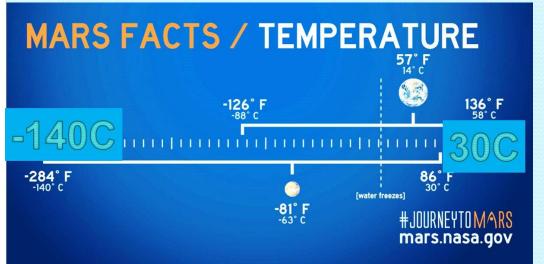


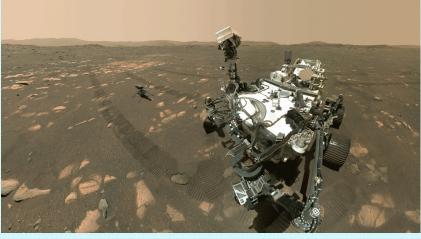
3D BGA Stack

200TCs (-55/100°C), Single- & Double-Sides

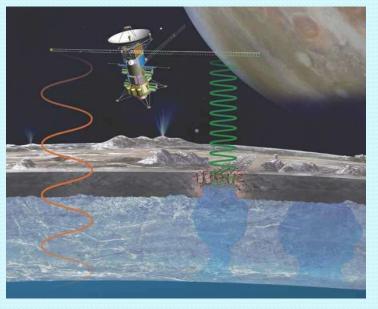


Jet Propulsion Laboratory California Institute of Technology M2020 Camera Cryogenic TC/Long Exposures

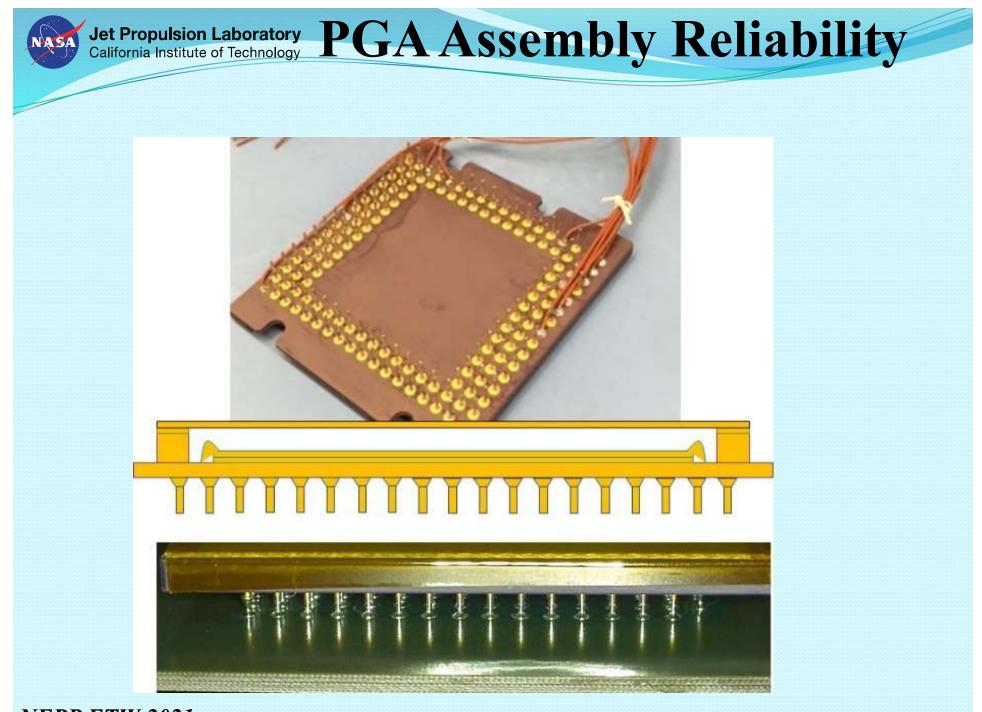




Jupiter-Europa ~-240°C

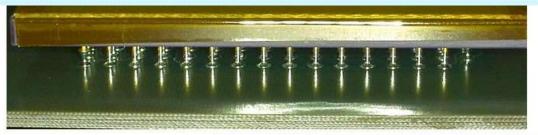


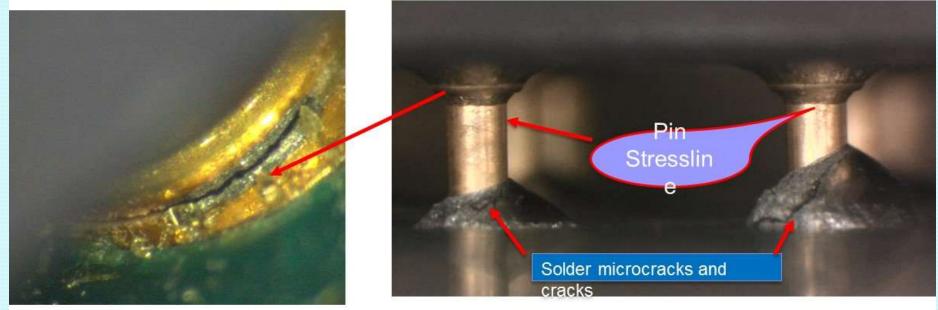
NEPP ETW-2021





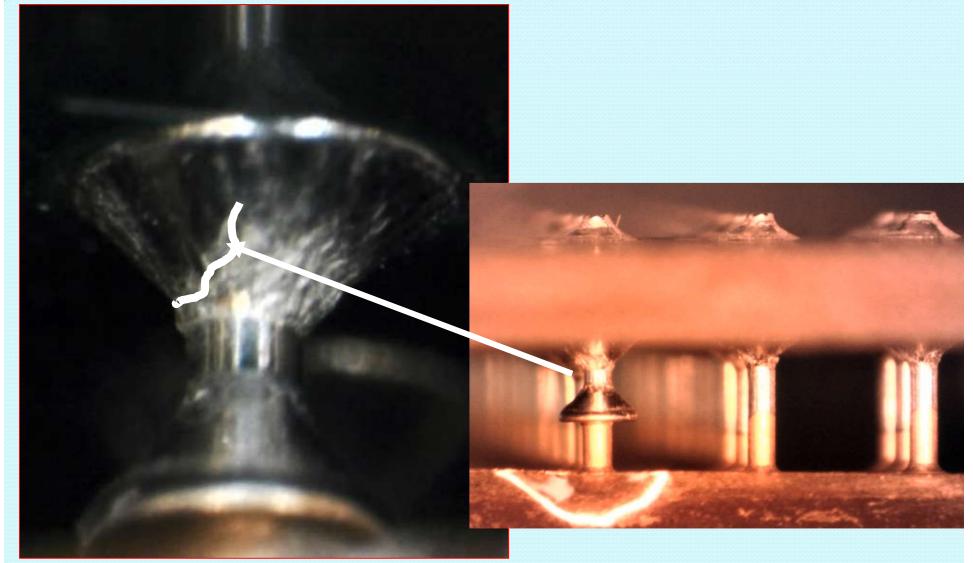
> $-135C/70^{\circ}C$, $\Delta T=205$ > PGA Pin Height = 50 mils



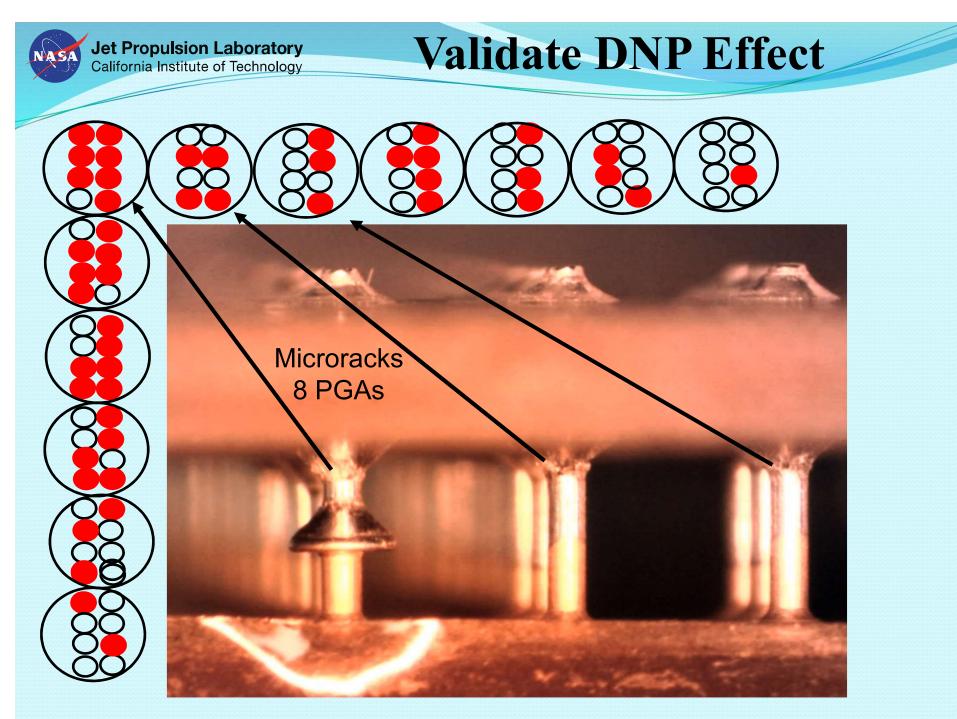


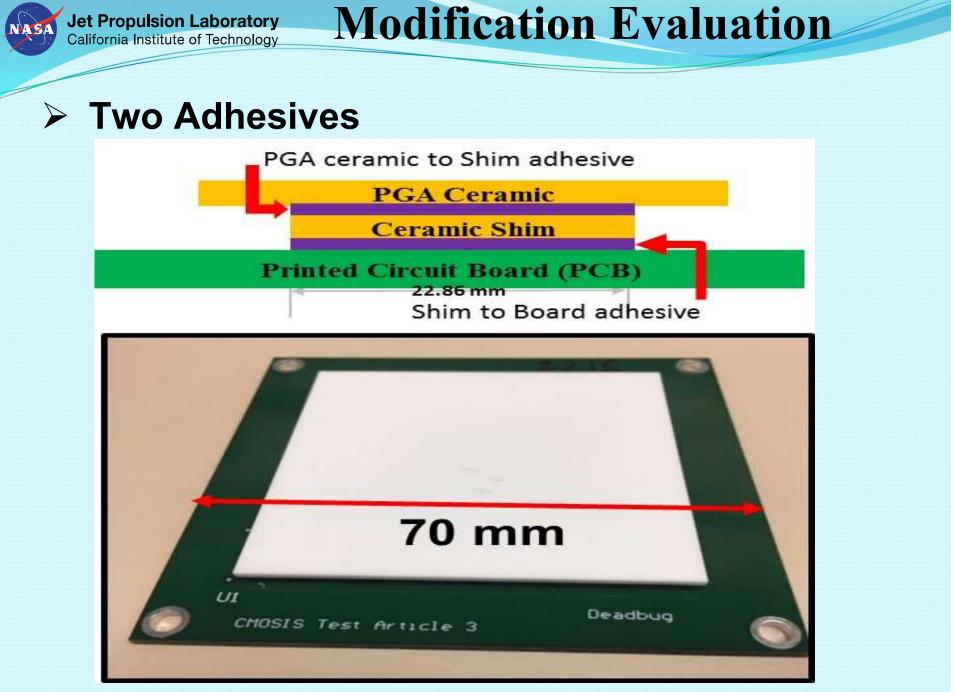
NEPP ETW-2021

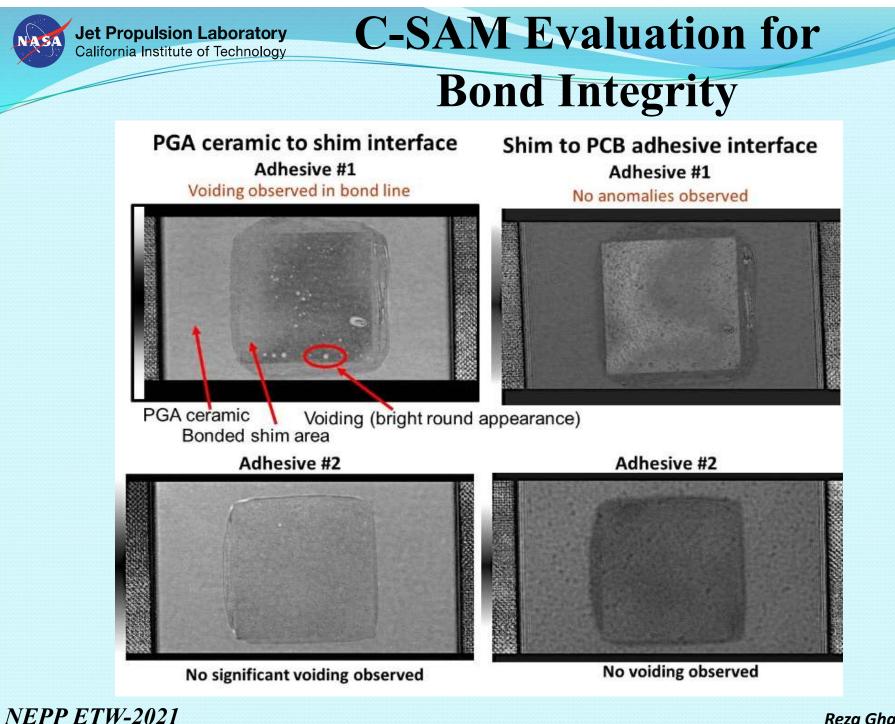
Jet Propulsion Laboratory California Institute of Technology Height Changed PoF Initial Crack at Corners



NEPP ETW-2021









Summary-I

Solder Joints are Weakest Link for Advanced Electronics Packaging

- Solder joint failure under standard TC conditions
- > NEPP reliability evaluation packaging task enveloped
 - > M2020 Cruise TC environmental requirement
 - > M2020 Controlled TC environment
- > M2020 unique and extreme cold TC PQV test verified

M2020 Leveraged NEPP PCB/3D Stack BGA

- Package long lead-time schedule impact
- M2020 funded building 5 test vehicles from NEPP
- Standard TC (-55/100C) was used for qualification
- Additional test vehicles were built under NEPP fund
- > Further TC and failure analysis performed under NEPP task
- All test results published under NEPP task

> M2020 Harsh Thermal Cycles (Cold Biased)

- > PGA cracking at the pin braze joints
- > PGA solder joint microcracking when pin height increased
- Author's modified versions with adhesive bonding were test verified: Minor solder joint changes after Harsh TCs and robust to shock/vibration via bond
- Understanding PoF is critical to develop robust modified packaging to meet TC requirement under Harsh TCs

NEPP ETW-2021



The research described in this publication is being conducted at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Copyright 2021 California Institute of Technology. U.S. Government sponsorship acknowledged.

The author would like to acknowledge the support of the JPL team including M2020 and industry/university partners. The authors also extend their appreciation to the program managers of the National Aeronautics and Space Administration Electronics Parts and Packaging (NEPP) Program.

Thank You!



Acknowledgment

NEPP ETW-2021