NEPP Processor Enclave: Post COVID Update

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by Edward Wyrwas (SSAI) and Steve Guertin (JPL)

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Acronyms

- Advanced Micro Devices (AMD)
- Application Specific Integrated Circuit (ASIC)
- Artificial Intelligence (AI)
- Advanced RISC Machine (ARM)
- Automated Test Equipment (ATE)
- Board Level Adapter Plate (BLAP)
- Body of Knowledge (BOK)
- Complementary metal oxide semiconductor (CMOS)
- Commercial off-the-shelf (COTS)
- Compute Unified Device Architecture (CUDA)
- Dual Data Rate (DDR)
- Device under test (DUT)
- Electrical, Electronic and Electromechanical (EEE)
- Field programmable gate array (FPGA)
- Fin Field-effect transistor (FinFET)
- General Purpose Input / Output (GPIO)
- Graphics Processing Unit (GPU)
- High Performance Computing (HPC)
- Input / Output (IO)
- Intellectual Property (IP)
- Linear energy transfer (LET)
- Key Process Indicators (KPI)
- LINear equations software PACKage (LinPack)
- Machine Learning (ML)
- Mean time to failure (MTTF)
- Multi-Bit Upset (MBU)
- National Aeronautic and Space Administration (NASA)
- NASA Electronic Parts and Packaging (NEPP)
- Numerical Python (NumPy)
- Open Compute Language (OpenCL)
- Open Graphics Language (OpenGL)
- Operating System (OS)
- Printed Circuit Board Assembly (PCBA)
- Procurement Request (PR)
- RApid Machine-lEarned Triage (RAMjET)
- Single-Bit Upset (SBU)
- Scientific Python (SciPy)
- Single-Event Effect (SEE)
- Single-Event Functional Interrupt (SEFI)
- Single-Event Upset (SEU)
- Single-Event Upset Cross-Section (σ_{SEU})
- Simultaneous Localization And Mapping (SLAM)
- System on Chip (SOC)
- System on Module (SOM)
- Transiting Exoplanet Survey Satellite (TESS)
- Technical Operation Report (TOR)

FY20-22 Hardware Roadmap

- FPGA Co-Processor Devices
  - Xilinx Zynq
  - Xilinx MPSOC
  - Xilinx Versal
- Low Power Microprocessors
  - AMD Ryzen 3 1200, 2200G
  - Intel Core i7 6500U (Purism Librem)
  - Intel Core i7 10710U Comet Lake (Purism Librem, expected Q3)
- SOCs with GPUs
  - AMD Ryzen Low Power R1102G, v1202B, R1305G, R1606
  - NVIDIA Jetson TX2, TX2i, Nano
  - NVIDIA Xavier AGX, NX, AGXi (expected Q3)
- Low Power SOCs
  - NXP i.MX 8 QuadMax, Pro
  - Edgeless EAI Series
  - Allwinner F1C200s
  - Samsung Exynos
  - Qualcomm Snapdragon
  - RISC-V (several candidates tracked)
  - Raspberry Pis (*Guertin JPL)
- Neural Network Devices
  - Google TPU (rev 1, rev 3)
  - Intel (Movidius/Nervana/Loihi)
  - RockChip Rk1808, Rk3399Pro
  - Nepes NM500
  - ARM Ethos-U55, U65 (NXP i.MX 8M Plus kit)
  - Sipeed Maix
  - Amlogic S905X3 (ODROID-C4 kit)
  - Gyrfalcon Lightspeeur AI
  - Xilinx Alveo
  - Texas Instruments Sitara AM57x
  - Kneron KL520, KL720
  - SimpleMachines
- Graphics Processing Units (discrete)
  - AMD Radeon e9173
  - NVIDIA GTX 1050

Red font devices were prepared for SEE testing during COVID in FY20 and FY21.
Green font indicates procurement in FY21.
Blue font indicates procurement in FY22.

FY22: Processor Enclave Testing

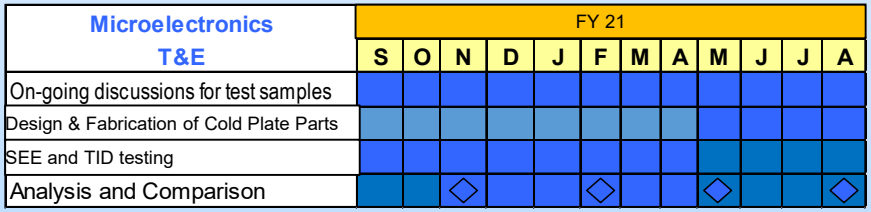
Description:

- This is a task over all device topologies and processes
- The intent is to determine inherent radiation tolerance and sensitivities
- Identify challenges for future radiation hardening efforts
- Investigate new failure modes and effects
- Testing includes total dose, single event and reliability. Test vehicles will include CPU, SOC and GPU devices from NVIDIA and other vendors as available
  - Compare to previous generations
  - Investigate failure modes/compensation for increased power consumption

FY22 Plans:

- Finish development of universal test suite which includes math (FFT, LinPack, Pi), output buffer (colors), memory hierarchy and neural networks
- Probable test structures for SEE and TID are COTS from:
  - NVIDIA (<16nm)
  - AMD (<14nm)
  - Intel (~10nm)
  - Samsung (<14nm)
  - Others (<45nm)
- Tests: characterization pre-rad, during and post-rad

Schedule:



Lead Center/PI: GSFC/SSAI/Wyrwas
Co-Is: Steve Guertin + Scott Stansberry

Deliverables:

- Test reports and quarterly reports
- Expected submissions for publications
- Cold plate and board level adapters

NASA and Non-NASA Organizations/Procurements:

- Source procurements:
  - Proton (MGH, Provision)
  - Heavy Ions (LBNL, TAMU)
  - TID (GSFC)
  - Laser (NRL)

FY22: AI & Machine Learning Devices

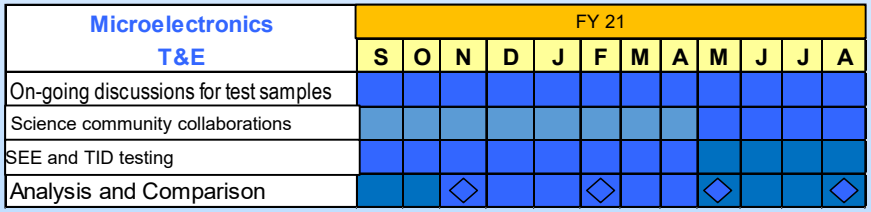
Description:

- This is a task over all device topologies and processes
- The intent is to determine inherent radiation tolerance and sensitivities and provide a baseline of current market offerings
- Identify challenges for future radiation hardening efforts
- Investigate new failure modes and effects
- Testing includes total dose, single event and reliability. Test vehicles will include 'simple interface' devices with USB or similar connectivity.
  - Identifies viable suppliers and provide insight into product obsolescence roadmaps
  - Investigate failure modes and mitigation strategies for increased power consumption and latch up events

FY22 Plans:

- Deploy AI and Machine Learning test suite developed in FY20, making refinements where necessary
- Probable test structures for SEE:
  - USB and other peripheral bus devices
  - 45nm down to 7nm
- Tests:
  - Electrical characterization pre-rad, during and post-rad
  - Functional testing with AI/ML accuracy and other KPI

Schedule:



Lead Center/PI: GSFC/SSAI/Wyrwas
Co-Is: Alyson Topper + Scott Stansberry

Deliverables:

- Test reports and quarterly reports
- Expected submissions for publications
- Additional cold plate and board level adapters

NASA and Non-NASA Organizations/Procurements:

- Source procurements:
  - Proton (MGH, Provision)
  - Heavy Ions (LBNL, TAMU)
  - TID (GSFC)
  - Laser (NRL)

Evaluation Timeline

*Radiation Testing (RT)
*Cold Block (CB) Adapter Development
*Test Feasibility Evaluation (FE)
*Continuation or
*Termination or

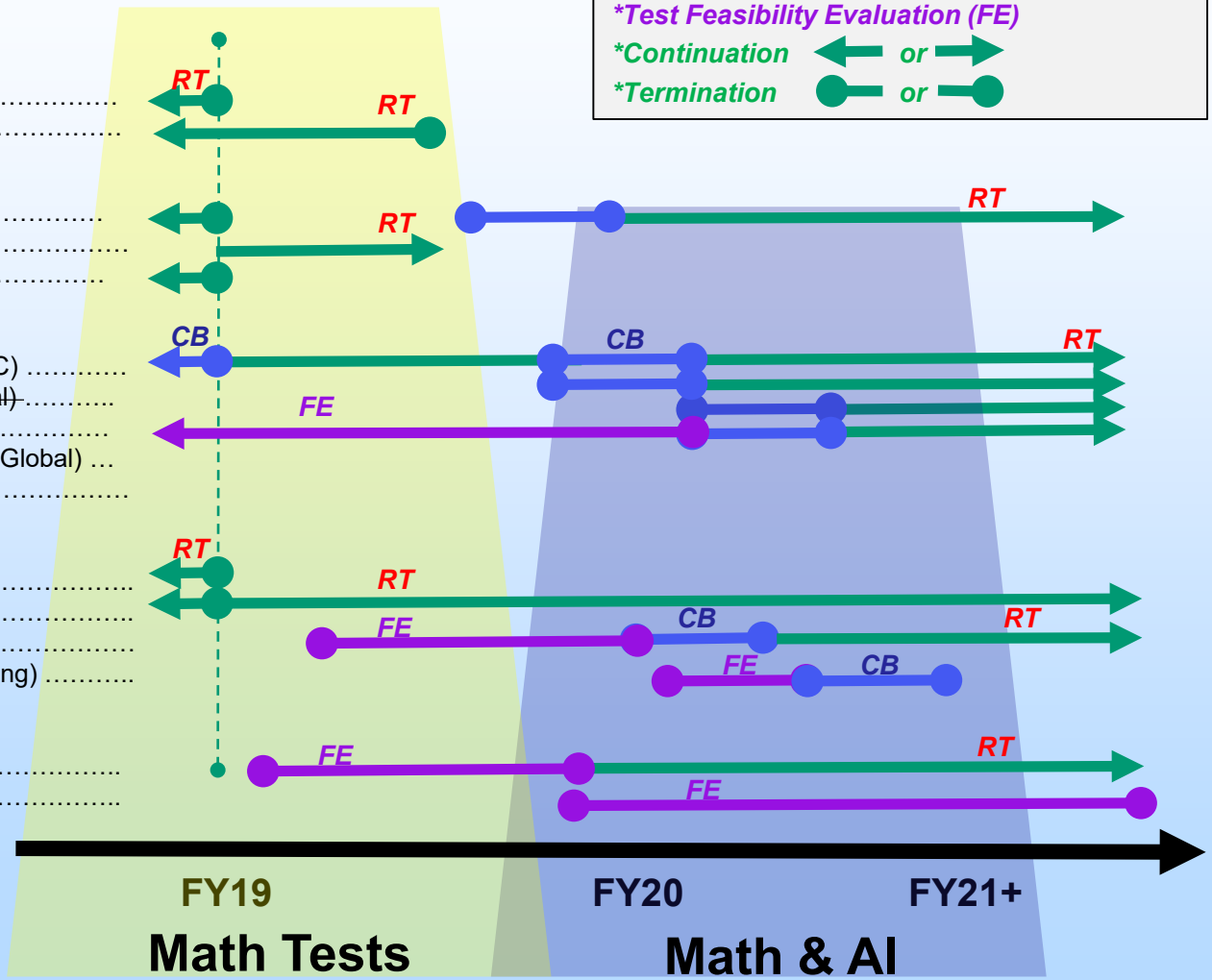
Microprocessors
- ≤14nm++ Intel (Intel) ……
- ≤10nm AMD (Global) ……

Microprocessors with embedded GPUs
- 14nm++ Intel (Intel) ……
- ≤ 10nm AMD (Global) ……
- 10nm Qualcomm 835 (Samsung) ……

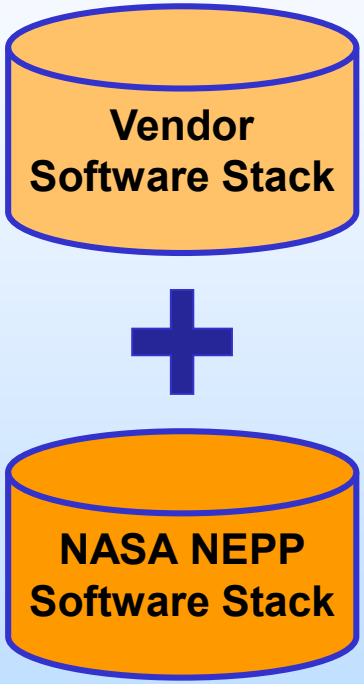
GPUs
- 14/16nm NVIDIA GTX 1050/1080 (TSMC) ……
- ~~14nm AMD Radeon RX580/Vega (Global)~~ ……..
- 14nm Intel Discrete GPU (Intel) ……
- 14nm Low Power, AMD Radeon e917x (Global) …
- ~~12nm NVIDIA RTX 2080 (TSMC)~~ ……

System on Chip
- 20nm NVIDIA Tegra X1 (TSMC) ……..
- 16nm NVIDIA Tegra X2 (TSMC) ……..
- 12nm NVIDIA Tegra Xavier (TSMC) ……
- ≤ 10nm Qualcomm Snapdragon (Samsung) ……..

Neural Network Devices
- Google TPU……..……..
- Many, many others……..……..



NEPP Software - Recap



- Software stack from vendor is comprised of Linux, PCBA carrier board drivers and hardware initializers, and some health prognostic tools
- Software stack from NASA NEPP is comprised of
  - 2x Mathematics tests (CUDA, OpenCL)
  - 1x Graphics buffer test (OpenGL)
  - 1x Linear Algebra test (Linpack)
  - 4x Artificial Intelligence tests (Python including SciPy and NumPy, Keras and TensorFlow 2.0)
- Android OS applications for Math and Graphics are in development too. The TensorFlow Lite one is complete.

Microsoft Teams Channel - Recap

- "NEPP – Processor Enclave"
  - NASA users can join with the team code: 1a2iu5y
- Contains many wiki and files which cover:
  - Set up, wiring and programming instructions for various devices and single board computers
  - Troubleshooting
- We discuss SOTA device landscapes in the chat
  - New COTS devices and development kits
  - New architectures and technology demos
  - Press release announcements and solicitations

GitLab

- NEPP and NEPP collaborators – authors credited
- Shared within NASA network
- So far > 40GB of content has been uploaded
  - CPU, GPU and AI Test Suites
  - Benchtop instrumentation
  - Build Guides
  - Distributable Reports
- The goal is to provide a singular source of standardized testing programs, scripts and applications for benchmarking and radiation testing GPUs, Microprocessors and AI devices

https://aetd-git.gsfc.nasa.gov/edward.j.wyrwas/nepp-processor-enclave

Bi-Weekly Processor Enclave Telecon

- **Space community, OEMs and component manufacturers**

- **Contact Steve Guertin (JPL) to join the mailing list with the call's dial-in and Webex information**

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Partners

- NASA JPL / NEPP west coast (Steve Guertin, Andrew Daniel)
- Sandia (David Lee)
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- Microprocessor Working Group
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