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NEPP 2021 FPGA Radiation Effects Update: Microchip PolarFire® (Single Event Effects) and Lattice Crosslink-NX (Total Ionizing Dose)

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2. NASA Goddard Space Flight Center

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Acronyms

Acronym	Definition
1MB	1 Megabit
3D	Three Dimensional
3DIC	Three Dimensional Integrated Circuits
ACE	Absolute Contacting Encoder
AHB	Advanced high performance bus
ADC	Analog to Digital Converter
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AMD	Advanced Micro Devices Incorporated
AMS	Agile Mixed Signal
ARM	Acorn Reduced Instruction Set Computer Machine
AXI	Advanced extensible interface
BGA	Ball Grid Array
BRAM	Block Random Access Memory
BTMR	Block triple modular redundancy
CAN	Controller Area Network
CBRAM	Conductive Bridging Random Access Memory
CCC	RTG4 clock conditioning circuit
CCI	Correct Coding Initiative
CGA	Column Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CN	Xilinx ceramic flip-chip (CF and CN) packages are ceramic column grid array (CCGA) packages
COTS	Commercial Off The Shelf
CRC	Cyclic Redundancy Check
CRÈME	Cosmic Ray Effects on Micro Electronics
CRÈME MC	Cosmic Ray Effects on Micro Electronics Monte Carlo
CSE	Crypto Security Engineer
CU	Control Unit
DC	Direct current
DCU	Distributed Control Unit
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
DFF	Flip-flop
DMM	Digital Multimeter
DMA	Direct Memory Access
DSP	Digital Signal Processing
DSPI	Dynamic Signal Processing Instrument
DTMR	Distributed triple modular redundancy
Dual Ch.	Dual Channel
DUT	Device under test
ECC	Error-Correcting Code
EDAC	Error detection and correction
EEE	Electrical, Electronic, and Electromechanical
EMAC	Equipment Monitor And Control
EMIB	Multi-die Interconnect Bridge
EPCS	Extended physical coding layer
ESA	European Space Agency
eTimers	Event Timers
ETW	Electronics Technology Workshop
FCCU	Fluidized Catalytic Cracking Unit
FeRAM	Ferroelectric Random Access Memory
FinFET	Fin Field Effect Transistor
FIR	Finite impulse response filter
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
FY	Fiscal Year
Gb	Gigabit
Gbps	Gigabit per second
GCR	Galactic Cosmic Ray
GEO	geostationary equatorial orbit
GIC	Global Industry Classification
GOMACTech	Government Microcircuit Applications and Critical Technology Conference
GPIO	General purpose input/output
GPIB	General purpose interface bus
GPU	Graphics Processing Unit
GR	Global Route
GRC	NASA Glenn Research Center
GSFC	Goddard Space Flight Center

Acronym	Definition
GTH/GTY/GTX	Transceiver Type
GTMR	Global TMR
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Test
HBM	High Bandwidth Memory
HDIO	High Density Digital Input/Output
HDR	High-Dynamic-Range
HiREV	High Reliability Virtual Electronics Center
HKMG	high-k metal gate
HMC	Hybrid Memory Cube
HPIO	High Performance Input/Output
HPS	High Pressure Sodium
HSTL	High speed transceiver logic
I/F	interface
I/O	input/output
I2C	Inter-Integrated Circuit
i2MOS	Microsemi second generation of Rad-Hard MOSFET
IC	Integrated Circuit
I-Cache	independent cache
JFAC	Joint Federated Assurance Center
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (FPGAs use JTAG to provide access to their programming debug/emulation functions)
KB	Kilobyte
L2 Cache	independent caches organized as a hierarchy (L1, L2, etc.)
LCDT	NEPP low cost digital tester
LEO	Low Earth Orbit
LET	Linear energy transfer
L-mem	Long-Memory
LP	Low Power
LUT	Look-up table
LVCMOS	Low-voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low –voltage transistor-transistor logic
LTMR	Local triple modular redundancy
LW HPS	Lightwatt High Pressure Sodium
M/L BIST	Memory/Logic Built-In Self-Test
Mil-STD	Military standard
MAPLD	Military Aerospace Programmable Logic Device
MFTF	Mean fluence to failure
µPROM	Micro programmable read-only memory
µSRAM	Micro SRAM
Mil/Aero	Military/Aerospace
MIPI	Mobile Industry Processor Interface
MMC	MultiMediaCard
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MP	Microprocessor
MP	Multiport
MPFE	Multiport Front-End
MPSoC	Multiprocessor System on a chip
MPU	Microprocessor Unit
Msg	message
MTTF	Mean time to failure
NAND	Negated AND or NOT AND
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
NOR	Not OR logic gate
NV(M)	Non-volatile (memory)
OCM	On-chip RAM
OSC-TMR-PLL	Embedded triple modular redundant phase locked loop
OSC	Oscillator
OSD	Office of the Secretary of Defense
PC	Personal Computer
PCB	Printed Circuit Board

Acronym	Definition
PCIe	Peripheral Component Interconnect Express
PCIe Gen2	Peripheral Component Interconnect Express Generation 2
Pconfiguration	SEU cross-section of configuration
Pfunctional_logic	SEU cross-section of functional logic
PHY	Physical layer
PLL	Phase Locked Loop
PLOL	Phase Locked Loop loss of lock
PMA	Physical Medium Attachment
POR	Power on reset
PPM	Parts per million
Proc.	Processing
PS-GTR	High Speed Bus Interface
PSEFI	SEU cross-section from single event functional interrupts
Psystem	System SEU cross-section
QDR	quad data rate
QFN	Quad Flat Pack No Lead
QML	Qualified manufactures list
QSPI	Serial Quad Input/Output
RC	Resistor capacitor
R&M	Reliability and Maintainability
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
RGB	Red, Green, and Blue
RH	Radiation Hardened
RT	Radiation Tolerant
RTD	Representative tactical design
RTG4FCCC_0	RTG4 Phase lock loop Core
SATA	Serial Advanced Technology Attachment
SCU	Secondary Control Unit
SD	Secure Digital
SD/eMMC	Secure Digital embedded MultiMediaCard
SD-HC	Secure Digital High Capacity
SDM	Spatial-Division-Multiplexing
SEE	Single Event Effect
SEF	Single event failure
SEFI	Single Event Functional Interrupt
SEL	Single event latchup
SERDES	Serializer/deserializer
SET	Single event transient
SEU	Single event upset
Si	Silicon
SK Hynix	SK Hynix Semiconductor Company
SMDs	Selected Item Descriptions
SMMU	System Memory Management Unit
SOA	Safe Operating Area
SOC	Systems on a Chip
SPI	Serial Peripheral Interface
sRIO	Serio Rapid I/O
SSTL	Sub series terminated logic
TBD	To Be Determined
Temp	Temperature
THD+N	Total Harmonic Distortion Plus Noise
TMR	Triple Modular Redundancy
T-Sensor	Temperature-Sensor
TSMC	Taiwan Semiconductor Manufacturing Company
UART	Universal Asynchronous Receiver/Transmitter
UltraRAM	Ultra Random Access Memory
USB	Universal Serial Bus
VNAND	Vertical NAND
WDT	Watchdog Timer
WSR	Windowed shift register
XAUI	Extended 10 Gigabit Media Independent Interface
XGXS	10 Gigabit Ethernet Extended Sublayer
XGMII	10 Gigabit Media Independent Interface)

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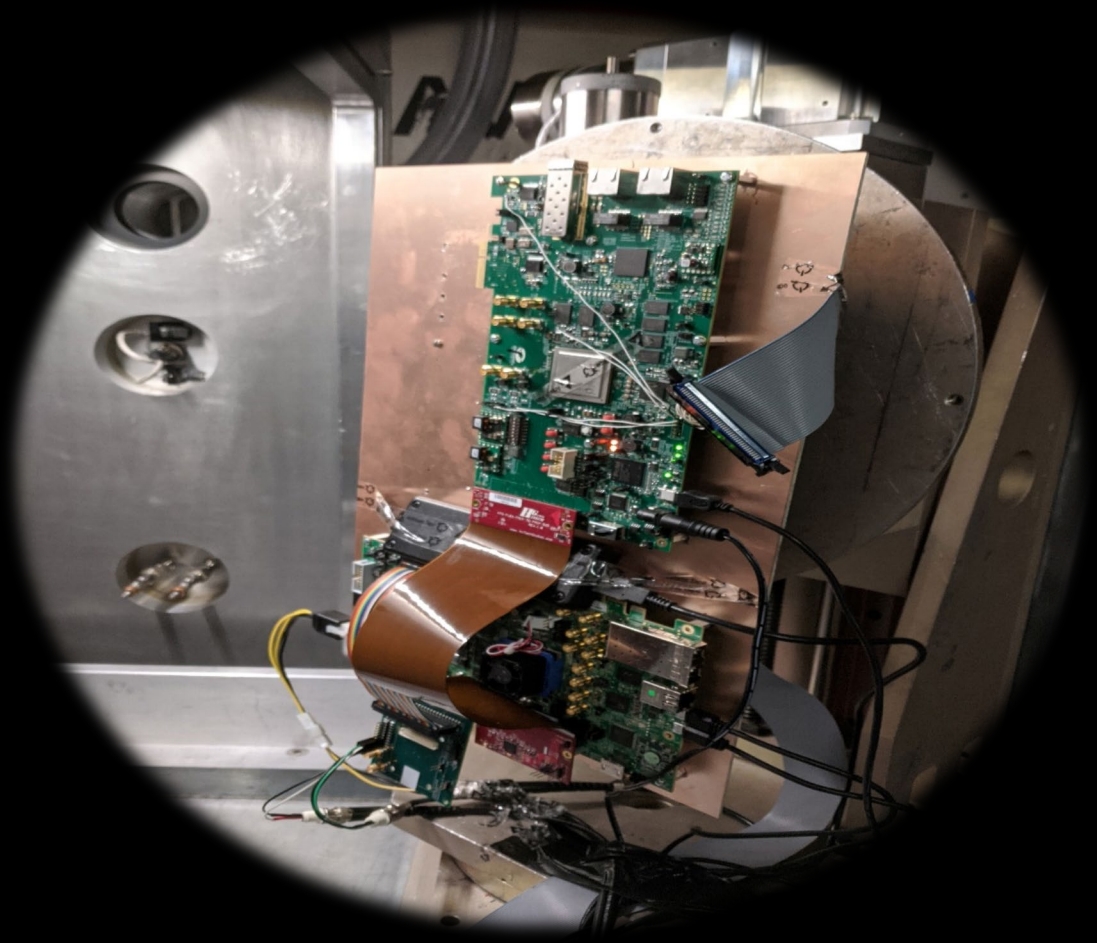
FPGA: Field programmable gate array
SEE: single event effects
TID: Total ionizing dose
SONOS: Silicon Oxide Nitride Oxide Silicon
FD-SOI: Fully Depleted Silicon On Insulator

Agenda

- Microsemi PolarFire ® 28 nm SONOS NV-based FPGA: SEE Test and Analysis
- Lattice 28 nm CrossLink-NX (FD-SOI) FPGA: TID testing using conventional test methods and the Dial-Down Approach

SONOS FPGA SEE Study: Microsemi PolarFire ® (MPF300TS-1FCG1152I)



Microsemi PolarFire Study Objectives

DUT: device under test
RT: Rad Tolerant

SEU: single event upset
SEL: single event latchup

- This is an independent investigation that evaluates the single event destructive and transient susceptibility of the Microsemi PolarFire® FPGA device.
- Design/Device susceptibility is determined by monitoring the DUT for SET and SEU induced faults by exposing the DUT to a heavy ion beam.
- Potential SEL is checked throughout heavy-ion testing by monitoring device current.
- FPGA part# MPF300TS-1FCG1152I (This is not the RT part).
  - However, there is no difference in SEE between the RT and the non-RT part.
  - Only packaging (and qualification) differentiates the two.
- This investigation is an extension of phase I. The focus is to further monitor voltage-drop SEFIs (observed in last year's testing) and Clocks.
- Although this is an independent study, we thank Microsemi for their partnership.

$$\sigma_{SEF} = f\left(\sigma_{configuration}, \sigma_{BRAM}, \sigma_{functionalLogic}, \sigma_{HiddenLogic}\right)$$

system σ_{SEU} ≈ Configuration σ_{SEU} + Block RAM σ_{SEU} + Functional logic σ_{SEU} + SEFI σ_{SEU}

SONOS configuration is not expected to have bit flips. However, pass/fail configuration readbacks were performed after each experiment.

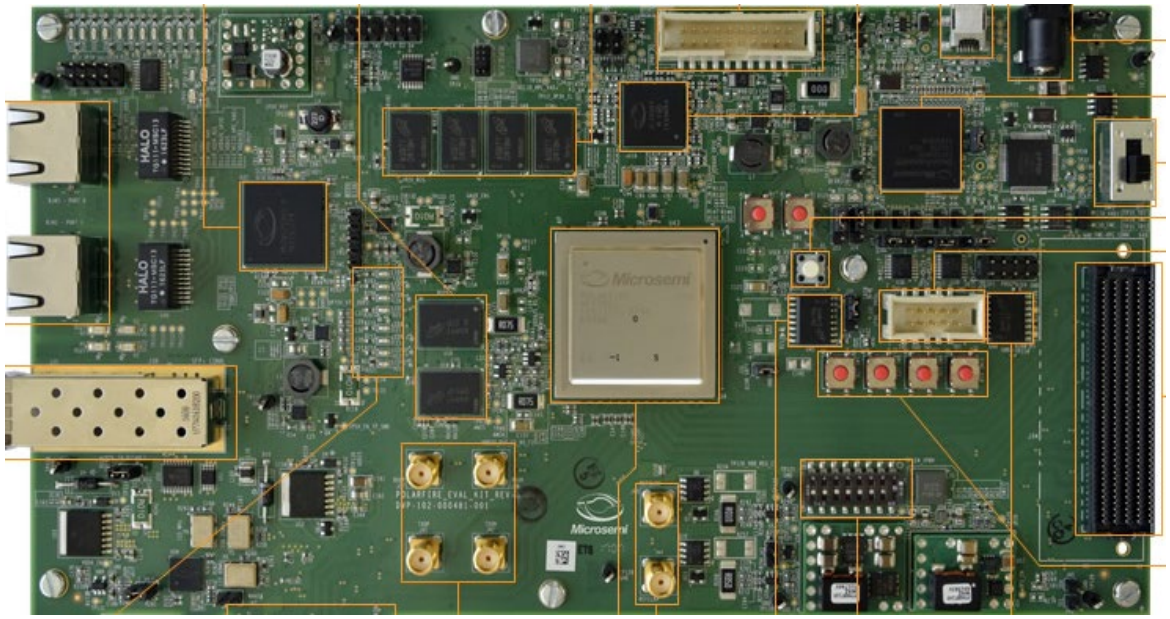
Impact to Community: Microsemi PolarFire ®

- SONOS non-volatile (NV) technology on a 28 nm technology node. Innately hardened configuration memory.
  - Reconfigurable FPGA with SEU immune configuration.
  - It is the first Microsemi FPGA product that has passed accelerated radiation testing for programmability in space. (See Microsemi for data)*
  - SEL (at extremes) > 80 MeV·cm^2/mg with GPIO at 1.8V (See Microsemi for data*).
- User fabric logic (flip-flops, combinatorial logic, global routes) are not hardened.
  - However, the increase in logic gates better allows for user inserted mitigation (e.g., TMR and watchdogs).
- Trust related embedded structures (might not be usable in your deployment environment… plan ahead and test):
  - Physically unclonable function (PUF)
  - Secure eNVM ® (non-volatile memory security feature)
  - Tamper detectors and counter measures

**Colored items are updated information from this year's radiation test campaigns.

DUT Preparation for Heavy-Ion SEE Testing

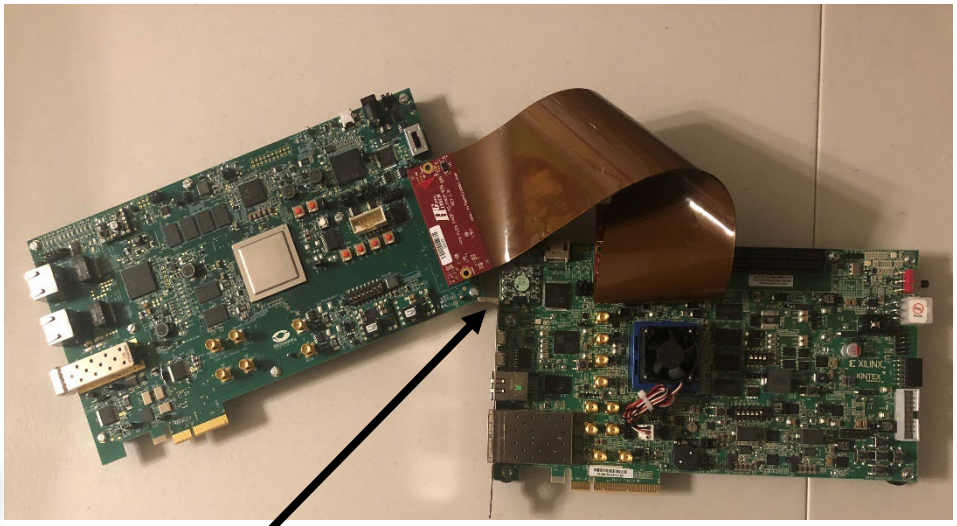
- NEPP acquired two evaluation-boards (MPF300-EVAL-KIT) populated with MPF300TS-1FCG1152I PolarFire® devices.
- The DUTs were thinned using mechanical etching via an Ultra Tec ASAP-1 device preparation system.
- The parts were successfully thinned to roughly 100 um.



NEPP use of an evaluation board as a daughterboard instead of developing custom daughter card.

Test Setup: Xilinx KCU105 Motherboard Tester

FMC: FPGA Mezzanine Card
LCDT: Low Cost Digital Tester

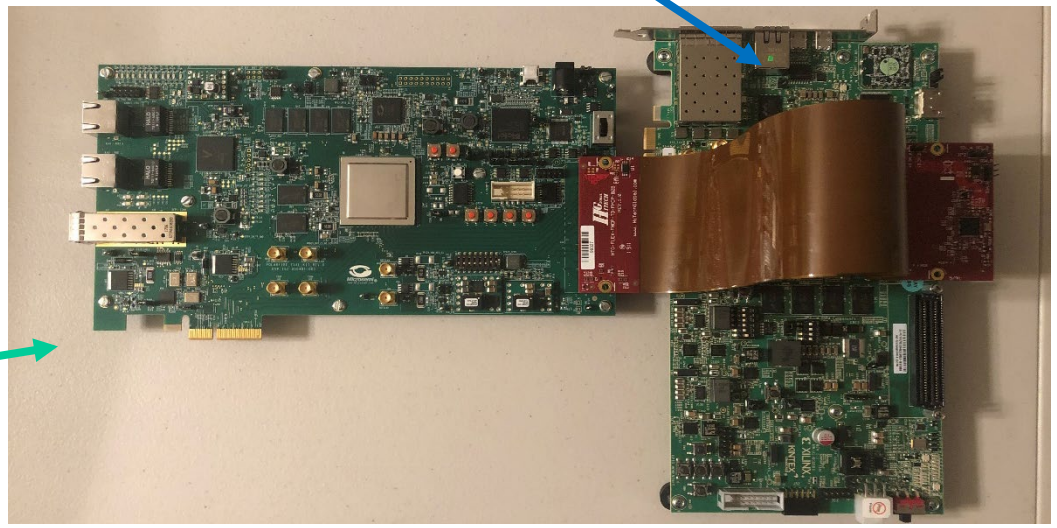


NEPP is now using evaluation boards as motherboards (testers). LCDT replacement

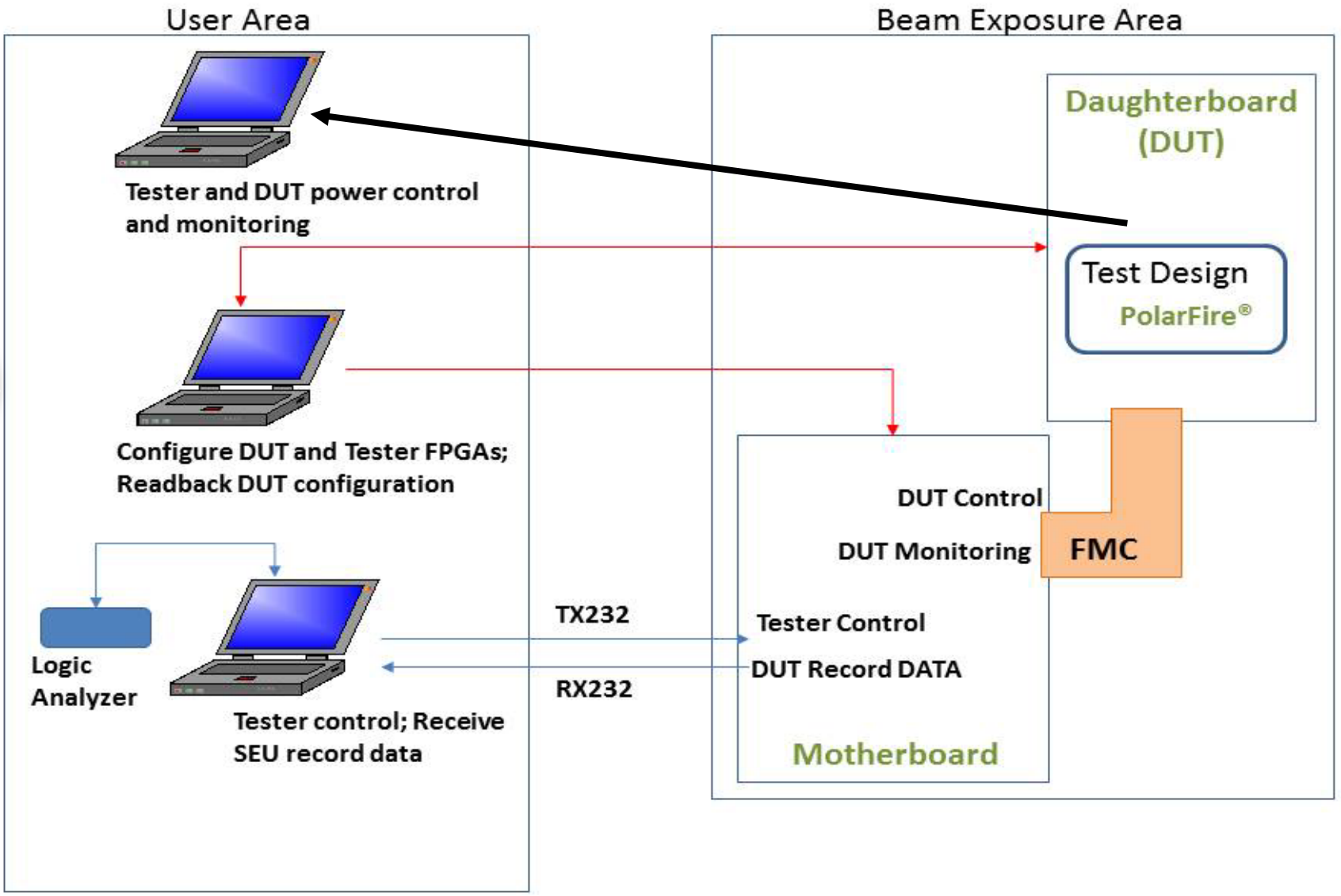
Flexible FPGA Mezzanine Card (FMC)

Motherboard

Daughterboard



Test System: At Heavy-Ion Facility



Summary: Phase I (Extension) DUT Test Structures

PLL: phase locked loop

LSRAM: large synchronous random access memory

URAM: distributed/synchronous random access memory

OSC: embedded oscillator

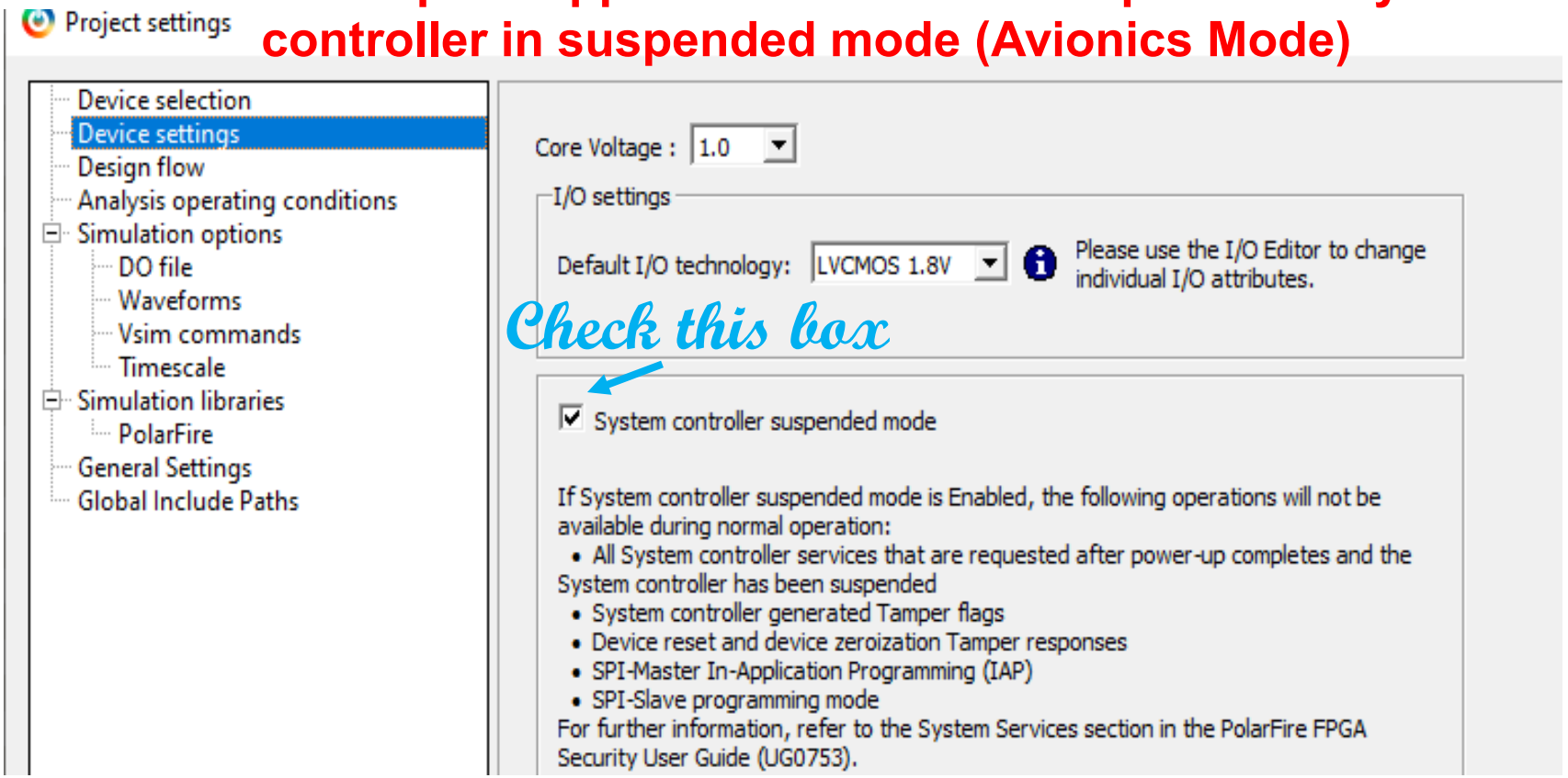
WSR: windowed shift register

Generic Component Study

Test Structure	Frequency Range
Configuration	N/A
LSRAM	10 MHz
URAM	10 MHz
PLL (Shift Registers (WSR))	160 MHz
OSC (Shift Registers (WSR))	160 MHz
Direct Clock Connection (Shift Registers (WSR))	160 MHz

User Advisory: System Controller

Most space applications will need to place the system controller in suspended mode (Avionics Mode)



- **Phase I extension: the embedded System Controller was expected to be tested in suspend mode because of the voltage-drop SEFIs observed in previous phase I radiation tests.**
- **Note that the suspend mode turns off a significant amount of tamper related mitigation.**

Heavy-Ion Test Facility and Test Conditions

Linear energy transfer (LET)

- **Facility:** Lawrence Berkeley National Laboratories 88-inch Cyclotron, 16 MeV/amu tune.
- **Flux:** $1.0x10^3$ to $1.0x10^5$ particles/(cm^2·s)
- **Fluence:** All tests were run to 1 x 10^7 particles/cm^2 or until destructive or functional events occurred.
- **Test Temperature:** Room Temperature.
- **Power Supply Voltage:** V_{cc} = 1.0 V; V_{IO} = 1.8 V

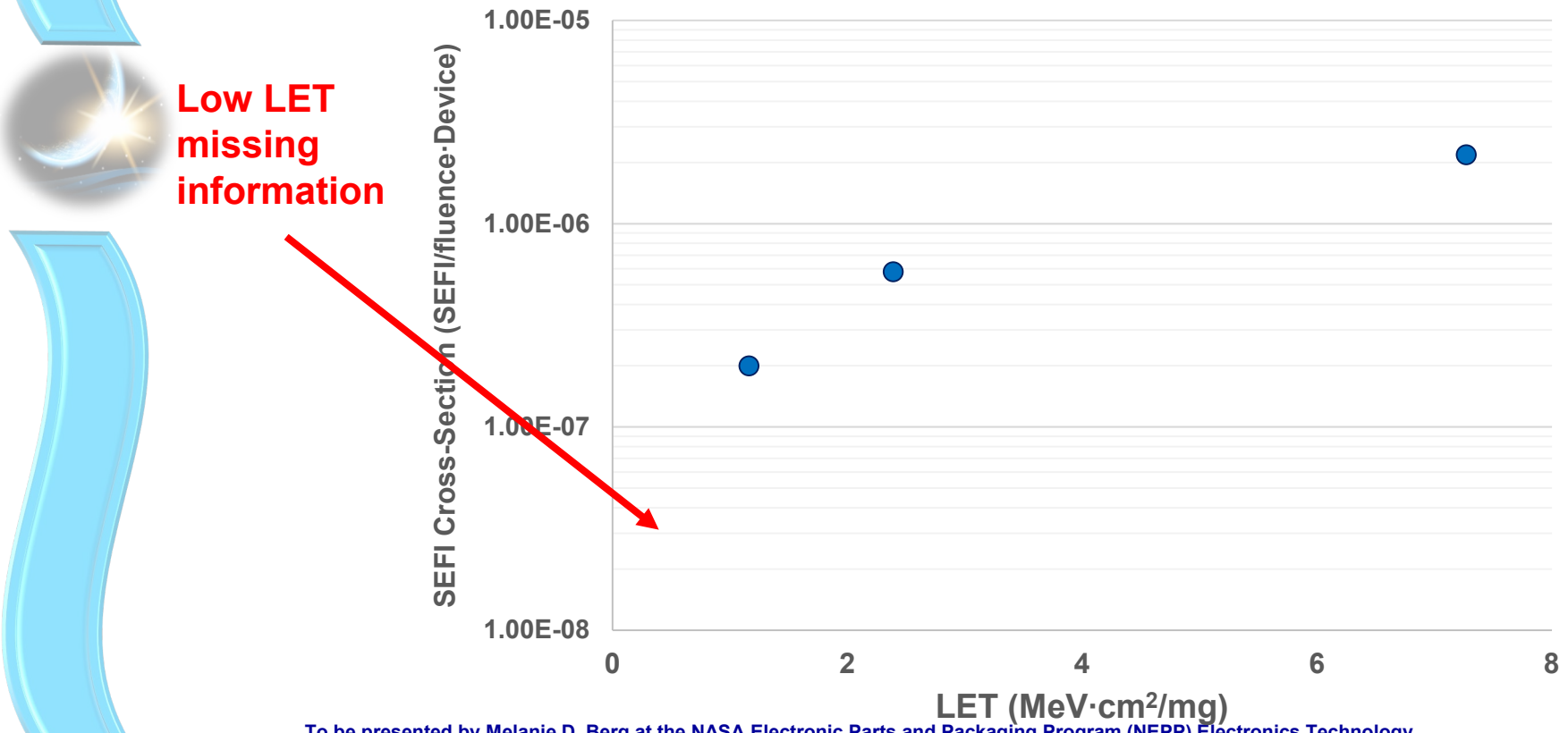
- **Problems with system controller suspend mode, limited our testing.**
- **Because of the evaluation board setup - more action is required to suspend the system controller (than checking the box in the design setting).**

Ion	Energy (MeV/Nucleon)	Effective LET(MeV·cm^2/mg)0°
N	16	1.16
O	16	1.54
Ne	16	2.39
Ar	16	7.27

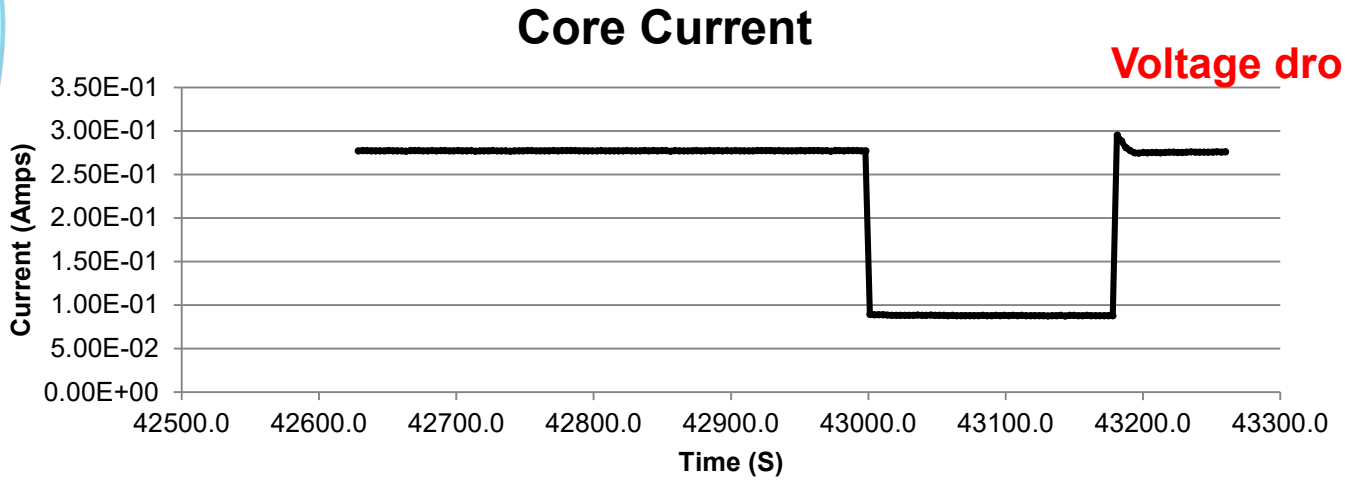
Voltage-Drop SEFI Cross Sections

$$\frac{SEFI}{fluence \cdot Device} = \frac{SEFI \cdot cm^2}{\#particles \cdot Device}$$

- LET_{onset} < 1.0 MeV·cm²/mg
- LBNL did not have ions available below 1.0 MeV·cm²/mg at the time of the campaign. Will test at another time.
- Knowledge of LET_{onset} is crucial for error-rate prediction



Voltage Drop SEFI Error Signatures



- Every experiment (if run with enough particle fluence) experienced a voltage (current) drop:
  - Most SEFIs had a duration of 1.7 ms.
  - Some SEFIs lasted 100's of seconds (100s to 400 s) (low probability of occurrence and might be cut shorter with an instant reset to the controller… we will test this assumption).
  - All SEFIs are self-clearing because they stem from the system controller. Configuration is never lost.
  - A reset is required after the SEFI because state-space is lost, metastability was observed on flip-flops, and PLLs became unstable.
- A follow-on test campaign will be performed with the system controller fully placed in suspend mode.

Important Note: For All FPGA Devices and Their Security Features

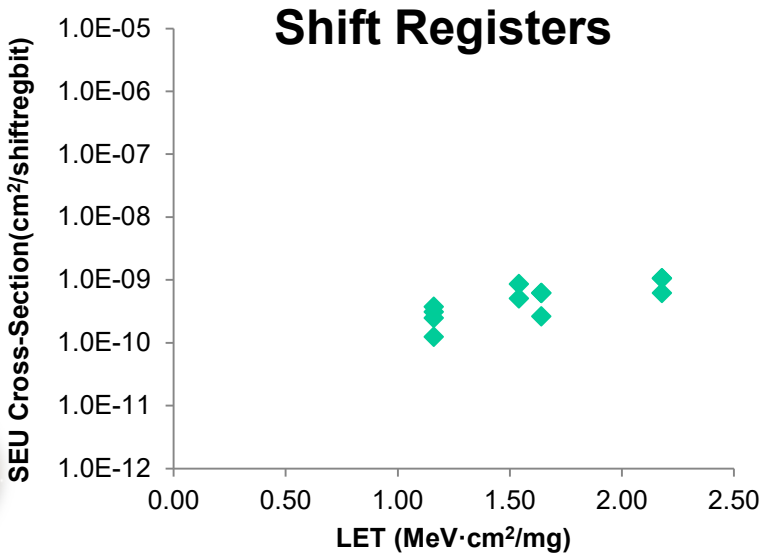
- Due to the new requirements for FPGA trust and security efforts:
  - FPGA manufacturers have added new security features.
  - Designers are required to use said security features.
  - Be aware, because most of these security features will not work in radiation environments (man-made, TID, or SEE)
- Consequences (not specific to PolarFire®):
  - Zeroing of design or configuration
  - Lock-out of device (inability to reprogram)
- Proper radiation testing specifically targeting your FPGA in your target environment should be performed prior to implementation.
- For the case of PolarFire®:
  - Because of the voltage-drops, most space missions will not be able to use the security features provided by the system controller.
  - Alternative mitigation might be required… plan ahead.

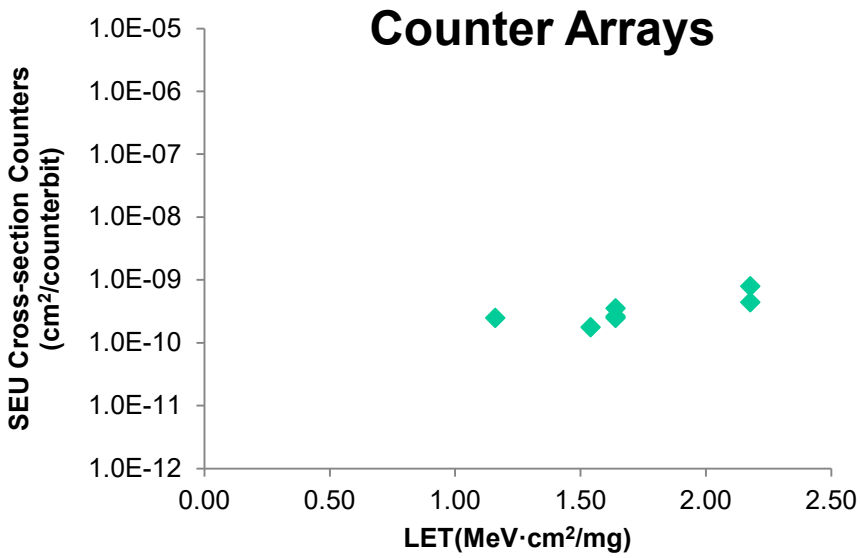
Embedded Memory SEU Cross Sections per Bit

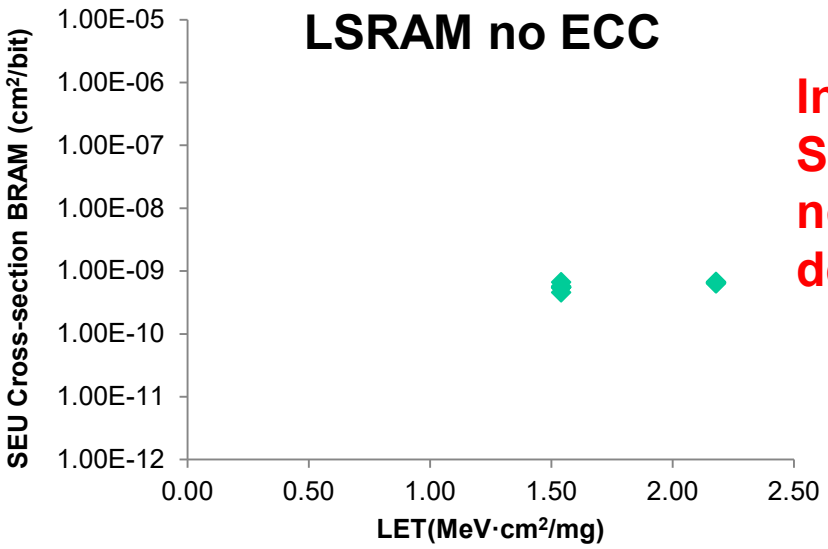
	N 1.2 MeV·cm²/mg	O 1.5 MeV·cm²/mg	Ne 2.5 MeV·cm²/mg	Ar 7.3 MeV·cm²/mg
LSRAM no ECC	3.0×10^{-10} cm²/bit	5.3×10^{-10} cm²/bit	7.3×10^{-10} cm²/bit	Not tested
LSRAM with ECC	0	0	0	0
URAM	1.8×10^{-10} cm²/bit	Not Tested	5.1×10^{-10} cm²/bit	Not Tested

- Memory locations are continuously read and then written.
  - After a full memory read/write cycle, data are inverted.
- Voltage drop SEFIs were observed in all tests because the system controller was not in suspend mode.
- No ECC related upsets were observed testing LSRAM with ECC through 7.3 MeV·cm²/mg:
  - One upset was observed at 1.2 MeV·cm²/mg. An address appeared to not be written when expected.
  - This was not an ECC related issue… a glitch caused the inability to write a cell. Extremely low probability of occurrence. Only occurred once during all testing.

Microsemi PolarFire ® SEU Data







Interesting note: per bit SEU cross-sections do not seem to be design dependent.

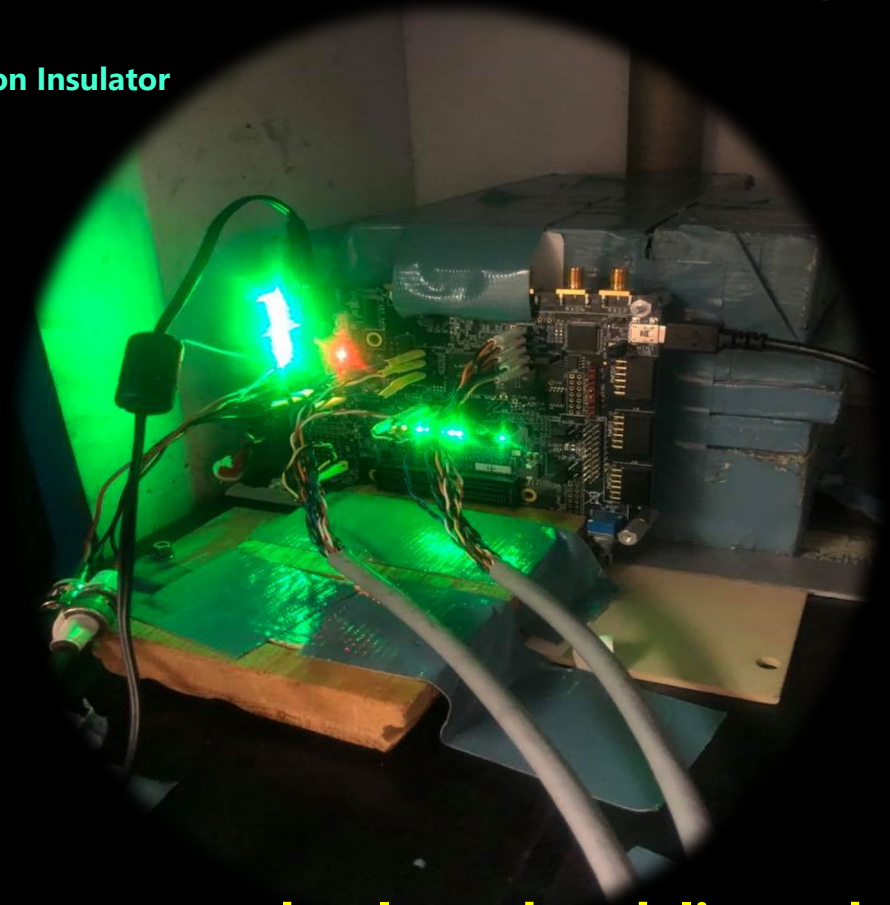
Microsemi PolarFire ® Additional SEE Testing

- Lower LET experiments are necessary to characterize the system controller voltage-drop LET_{onset} and to better predict error-rates.
  - Requires use of heavy-ion tests with LETs as low as 0.1 MeVcm^2/mg.
  - Characterization is necessary for missions that require the use of the system controller (not in suspend mode).
- Higher LET experiments are necessary in order to fill out the SEU cross-section curve; and to find saturation.
- NEPP will investigate:
  - System controller SEFI (cross-section reduction) while placed in suspend mode. SEU cross-sections are expected to have an on-set moved (higher) to roughly 7 MeV·cm^2/mg (See Microsemi data).
  - More complex embedded components
  - Test-as-you-fly (representative tactical designs (RTD)).

Full report (phase I extension) will be provided in July 2021

FD-SOI FPGA Total Ionizing Dose(TID) Study: Lattice CrossLink-NX (LIFCL-40-8BG400CES2)

FD-SOI: Fully Depleted Silicon on Insulator



FD-SOI is a planar process technology that delivers the benefits of reduced silicon geometries while simplifying the manufacturing process.

Lattice CrossLink-NX TID Objectives

DUT: device under test

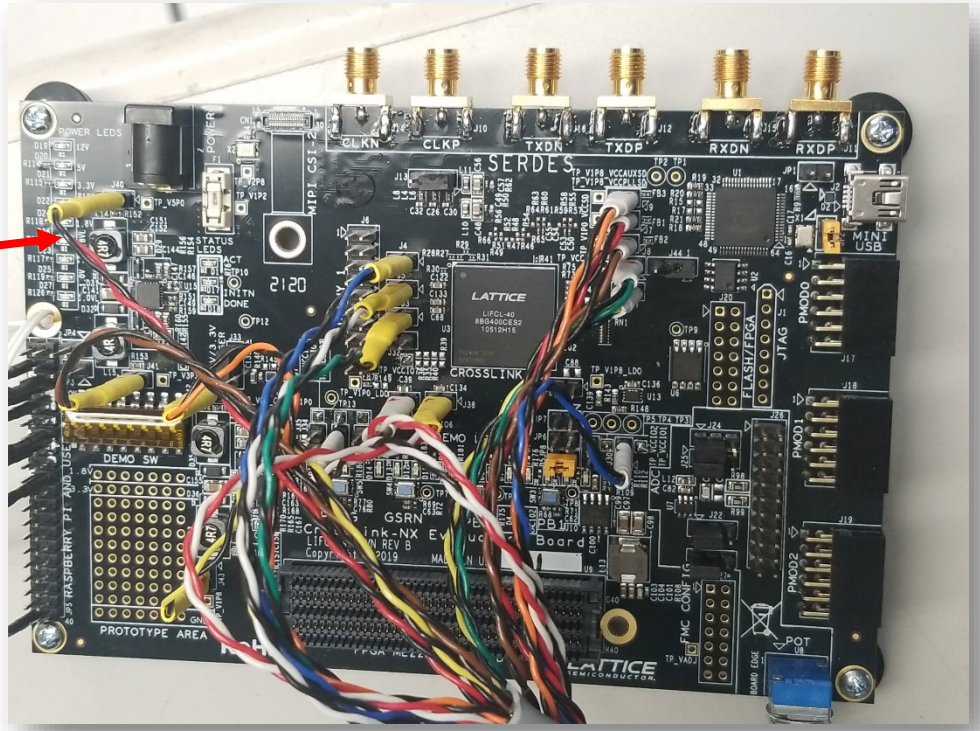
- This is an independent investigation that evaluates the TID degradation and potential destructive behavior of the Lattice CrossLink-NX FPGA device.
- Design/Device susceptibility is determined by exposing the DUT to Co-60 gamma rays in repetitive steps and measuring DUT performance dose effects throughout the experimental process.
- FPGA part# LIFCL-40-8BG400CES2 10512H15
- Although this is an independent study, we thank Lattice for their partnership.

Overview(1)

- TID experiments were held in March 2021.
- Tests were performed with the DUT on an evaluation board.
- Tests were expected to be performed as a “first-look.”
  - Evaluation board voltage regulators are known to be a problem during TID testing.
  - In parallel, NEPP is designing a custom board for TID evaluation purposes.

DAQ: data acquisition module

Current monitoring wires for the DAQ



Overview(2)

- Two devices under test (DUT4 and DUT5) were tested with Co-60 exposure steps up to approximately 300 krads.
- Three Distinctive test-structures were downloaded to each DUT for experimental measurements:
  - Shift register* with PLL with additional delay lines
  - Shift register* without PLL with additional delay lines
  - DSP*: finite impulse response filter (FIR)
- TID measurements taken:
  - Input-rise to output-rise delay (oscilloscope + test lead)
  - Input-fall to output-fall delay (oscilloscope + test lead)
  - Critical path degradation (only measured for DUT 5): New dial down approach for measuring internal delay paths.
  - Expected functional behavior (shift registers and DSP-FIRs)
  - Switching-rates: Rise time and Fall time (oscilloscope + test lead)
  - Electrical parametric behavior (current: DAQ)
- Dose rate effects might have a dependence on exposure effects.
- Problems with Evaluation board voltage regulators had to be addressed during testing.

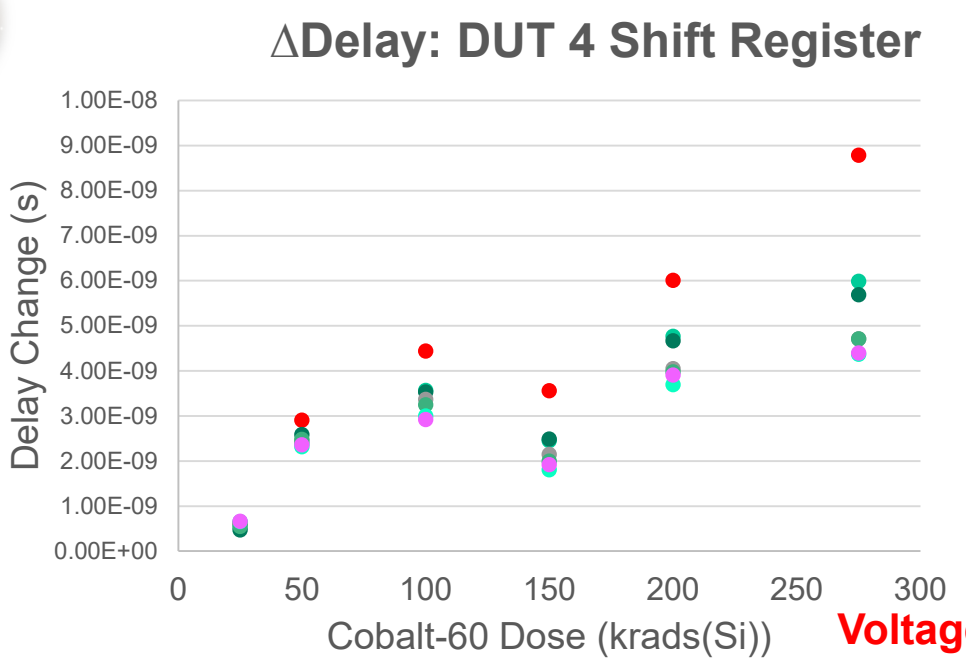
*Melanie Berg et. al, "FPGA SEU Radiation Test Guidelines:" ***https://nepp.nasa.gov/files/23779/fpga_radiation_test_guidelines_2012.pdf***

Lattice CrossLink-NX TID Experiments

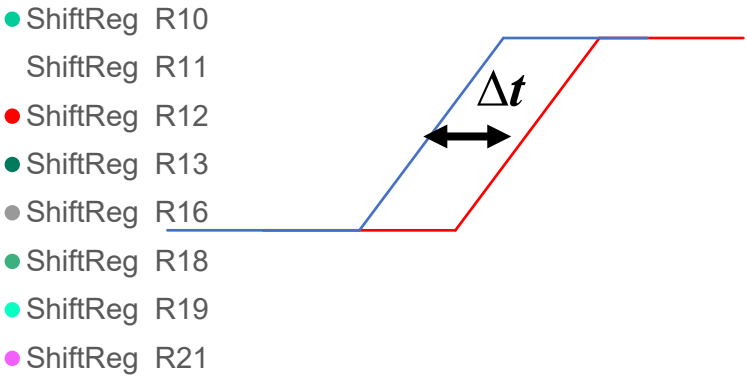
- DUT characteristics are first measured. The DUT is then placed in the TID chamber with cement block shielding.
- DUT heartbeats are monitored during irradiation steps.
- After each irradiation step is complete, the DUT is removed and tested for irregularities:
  - Additional I/O (were added to test structures) for measuring delays:
    - Input signal is provided by a function generator.
    - Signal flows through internal DUT circuitry to multiple DUT outputs
    - Signal input and DUT output are compared using an Oscilloscope and GHz probes prior to each irradiation step.
  - Functional Behavior
    - Shift registers and DSP filters are run at speed to determine if degradation has affected behavior.
    - Dial down approach is used to determine how much degradation to internal circuit paths has occurred per irradiation step.
  - Electrical parametric behavior:
    - Current leakage
    - Rise and fall times (switching characteristics)

DUT 4: Input-Rise to Output-Rise Delay Δt Measurements

- Δt Increase is almost linear across dose steps.
- Dip occurs at 150 krads.
- Rise to rise Δt are significant at 50 krads dose and greater
- GPIO Pin 12 appears to have the sharpest Δt.
- 4.5 ns < Δt <9 ns (*Δt is significant for source-synchronous designs*)



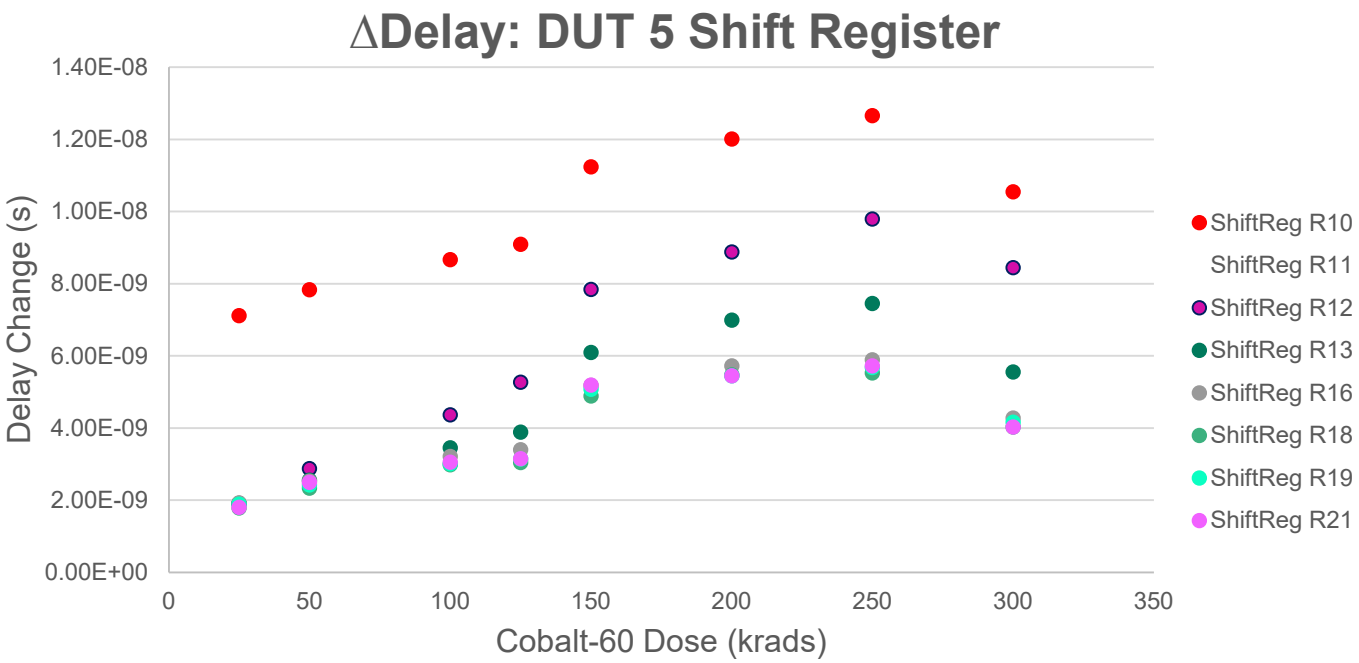
- GPIO pins are 3.3 V
- R*n*: *n* is a GPIO pin number
- Input signal is replicated and sent to 8 output pins



Voltage regulator died after 275 krads(Si)

DUT 5: Input-Rise to Output-Rise Delay Δt Measurements

- Similar Δt linear increase for DUT5 (as compared to DUT 4)
- Dip occurs at 300 krads for this set of experiments.
- Rise to rise Δt are significant at 25 krad dose and greater
- GPIO Pin 10 appears to have the sharpest Δt and is an outlier.
- DUT 5 experienced greater in Δt. In the 10 ns range!!!



Could Dose Rates Be The Source of The TID Measurement Dips

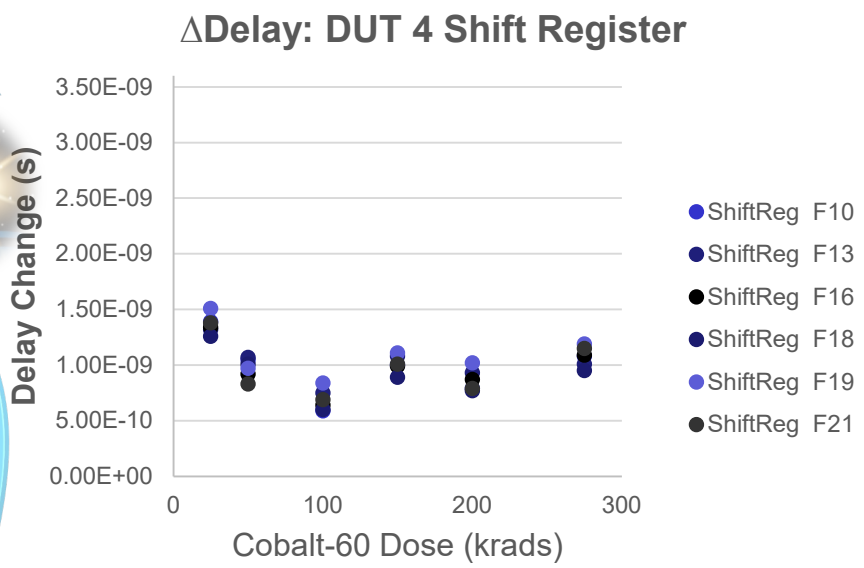
DUT 5 Rate Table

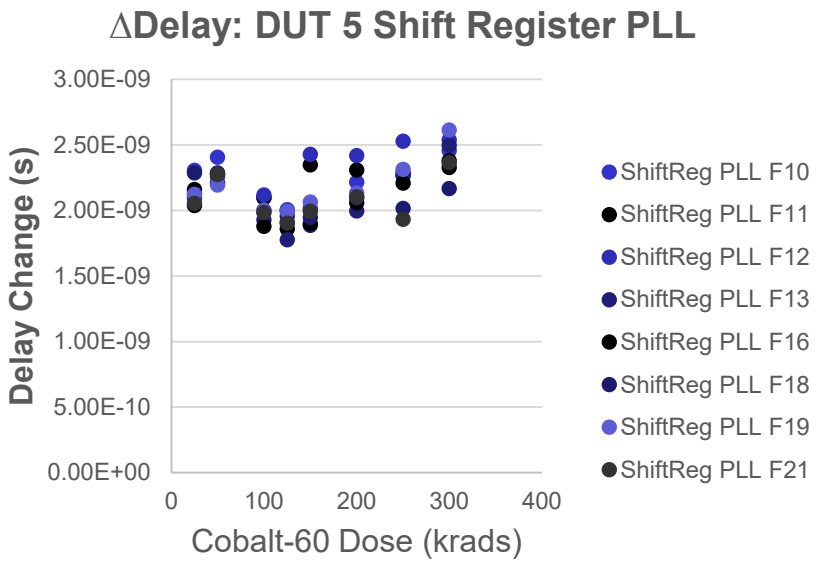
Start	Run #	Stop	Rate (Rad/Min)	Total Dose (krad(Si))
3/24/2021	1	3/24/2021	196.5	25
3/24/2021	2	3/25/2021	23.28	50
3/25/2021	3	3/25/2021	228.5	100
3/25/2021	4	3/26/2021	31.24	125
3/26/2021	5	3/26/2021	225.92	150
3/26/2021	6	3/26/2021	229.92	200
3/26/2021	7	3/29/2021	14.17	250
3/29/2021	8	3/29/2021	209.47	275
3/29/2021	9	3/29/2021	209.47	300
3/29/2021	10	3/30/2021	26.69	330

Voltage regulator died at 330 krad(Si)

DUT4 and DUT 5 Input-Fall to Output-Fall Delay Δt Measurements

- **Overall Δt are within 3 ns.**
- **Not much change after the first irradiation.**





- **Note: Measuring Rise-Rise and Fall-Fall provide information on I/O delays (not internal path delays).**
- **These measurements must be considered when source-synchronous designs are implemented… plan ahead.**

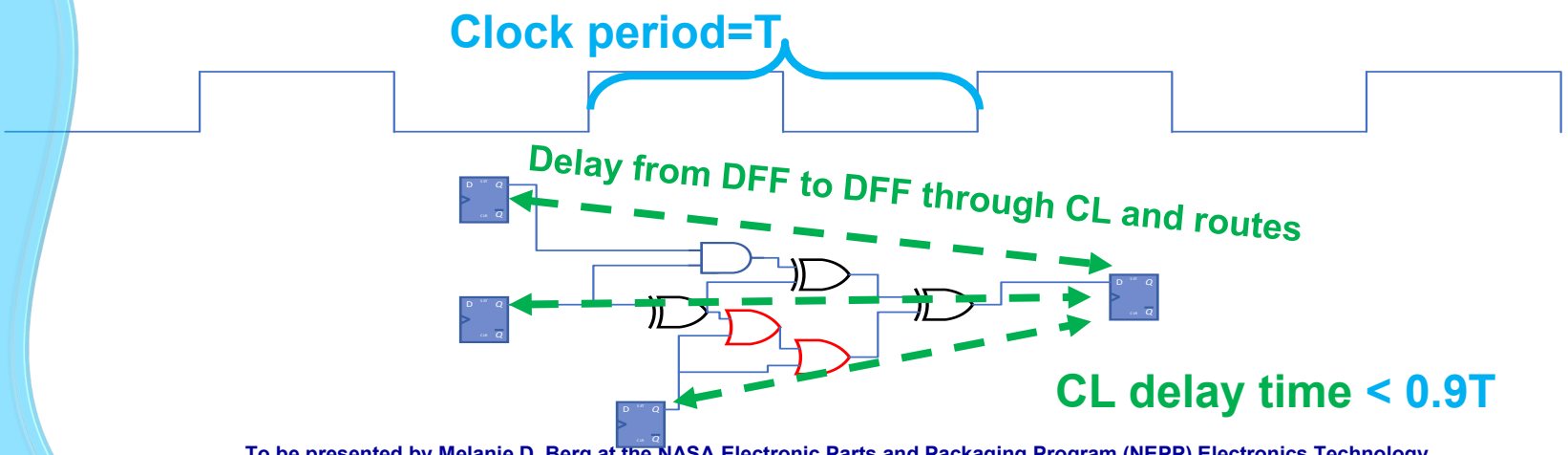
FPGAs and TID Experimental Techniques

- Measuring FPGA TID performance degradation, requires additional techniques compared to our conventional methods of evaluation.
- Conventional Methods:
  - Current leakage,
  - Switching characteristics,
  - Delay measurements:
    - Ring oscillators (only uses buffers/inverters and requires I/O to measure).
    - Strings of inverters or buffers.
  - For anything that requires I/O intervention:
    - I/O will have their own degradation characteristics. Non-linearities can interfere with internal node degradation measurements.
- The Dial-Down approach is used to get a better understanding of internal degradation that will meet the needs of FPGA designers.
  - Generally, design specifications require 10% slack in clock period for combinatorial logic delay.
    - Should designers allot for additional slack due to TID degradation?
  - There is no I/O intervention for pass/fail measurements.
  - Essentially, the design measures itself.

Synopsis of The Dial-Down Approach

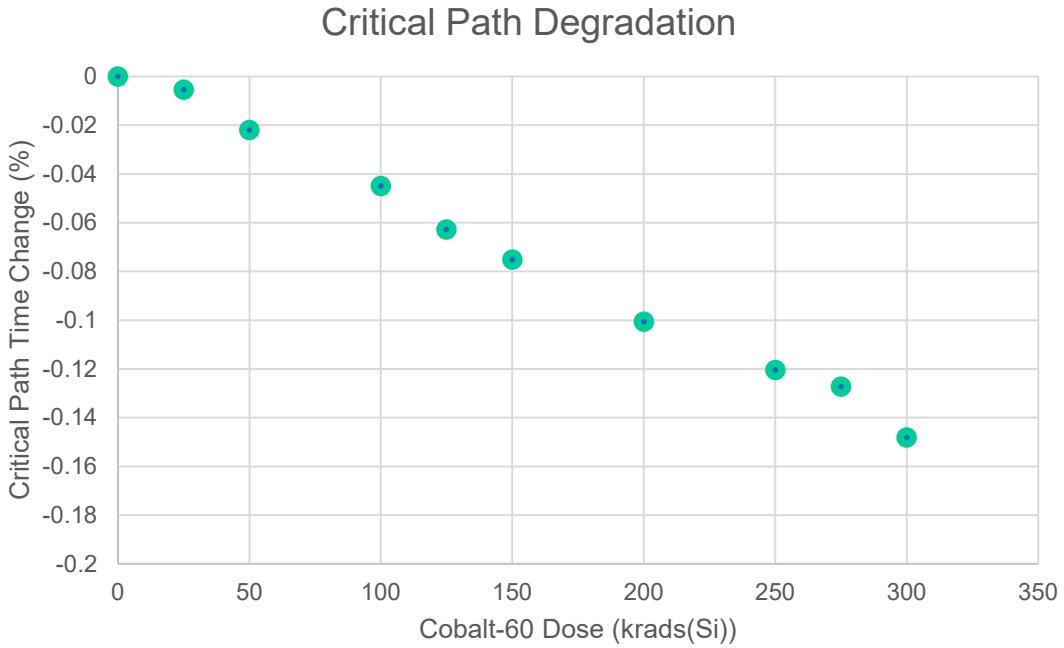
- Synchronous Design: sample/hold
  - During hold, combinatorial logic (CL) compute.
  - DFFs sample every (rising)edge of the clock.
- Computation time (CL delay) must be smaller than clock period (T):
  - Otherwise, the logic will create incorrect states (sometimes metastability).
- CL delay degradation can be measured by finding the tightest-fit clock period.
  - As delay grows, the clock period needs to increase.
  - The clock frequency is dialed down to find the tightest fit pre-exposure to each rad-step: The "Dial-Down Approach."
- Requires testing across a variety of designs.
- Failure detection is observed by faulty internal behavior and is not affected by I/O degradation.

CL: combinatorial logic
DFF: flip flop



Lattice CrossLink-NX Dial-Down TID Measurements

- The DUT test-structure for the dial down experiment was 2 chains of DSP finite impulse response filters.
- Graph shows percentage Δt for internal critical path.
- Δt reaches 10% close to 200 krads (for this design and this DUT).
- This was a first look investigation. Future tests will include shift registers and counters (and other representative tactical designs (RTDs)



Full report will be provided in July 2021

TID and Important Notes for FPGA Designers

- **Rise and Fall Time degradation:**
  - **Can affect performance**
  - **Can violate FPGA manufacturer reliability requirements (FPGA will not work properly)**
- **Internal delay degradation**
  - **Functional behavior**
- **I/O delay:**
  - **Can cause source synchronous designs to malfunction**

NEPP Future Work
SEE in FPGA Devices

To be presented by Melanie D. Berg at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 15-18, 2020 and published on nepp.nasa.gov.

Potentially In the Works for This Coming Year…

- Ongoing work towards fluence-to-failure representative tactical designs (RTD) test-as-you-fly metrics and analysis techniques.
- Further Investigation of Lattice 28 nm CrossLink-NX (FD-SOI) SRAM-based FPGA
  - Proton
  - TID
  - Devices are in-hand.
- Further SEE investigation of Microsemi PolarFire ® 28 nm NV-based FPGA
  - Proton
  - Heavy-ion
  - Test-as-you-fly
  - Devices are in-hand.
- Xilinx SRAM-based MPSoC 16nm FinFET ruggedized package
  - Proton
  - Heavy-ion
  - Test-as-you-fly (NASA-specific)
  - Devices are in-hand.

Thank You
Questions?

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