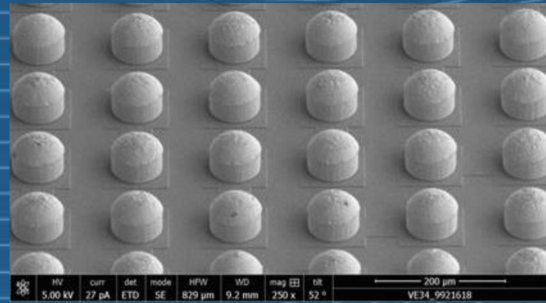
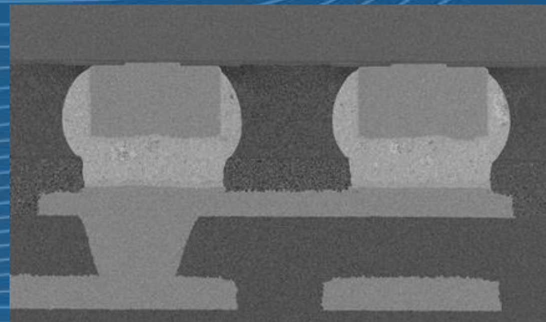
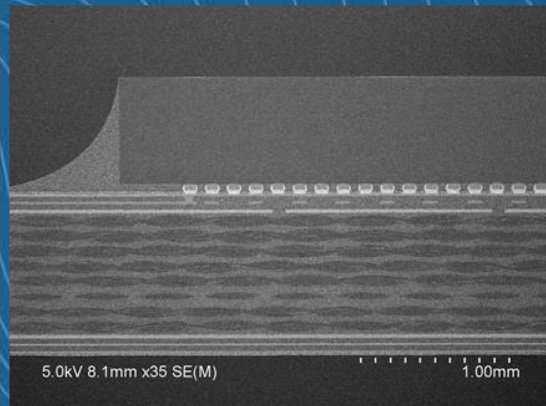
CAES PIONEERING ADVANCED ELECTRONICS







Overview of the CAES Organic Class Y PIDTP

Scott Popelar, Ph.D.
Development Engineer Chief
CAES Space Systems Division
Colorado Springs, CO

June 13, 2022

Organic Class Y Flip Chip PIDTP

Objective and Contents

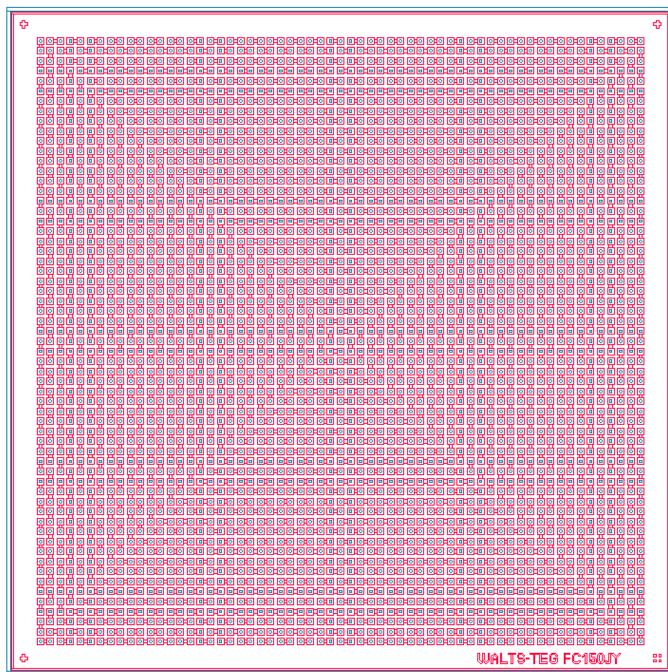
CAES PIONEERING ADVANCED ELECTRONICS

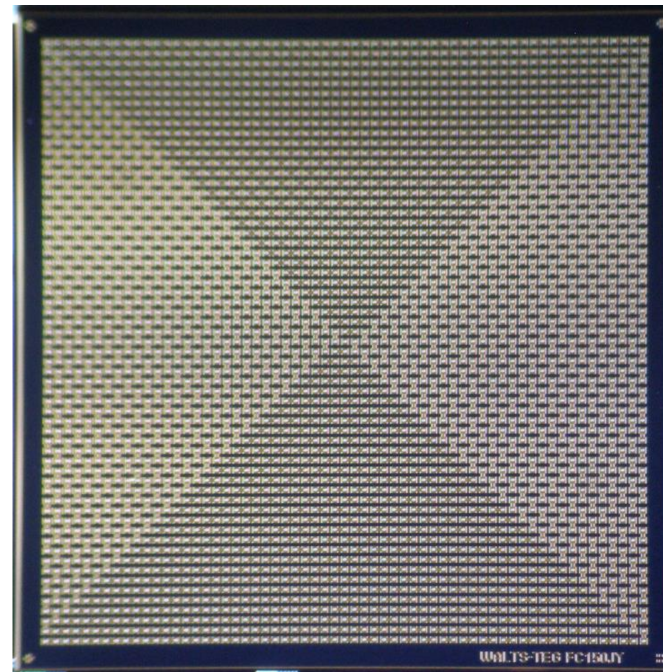
- **PIDTP Objective**
  - Satisfy Package Integrity Demonstration Test Plan (PIDTP) requirements for non-hermetic Class Y flip chip on organic assembly technology by addressing manufacturability, quality and reliability issues defined in MIL-PRF-38535 Rev M
  - Address both copper pillar and solder bump flip chip interconnect types

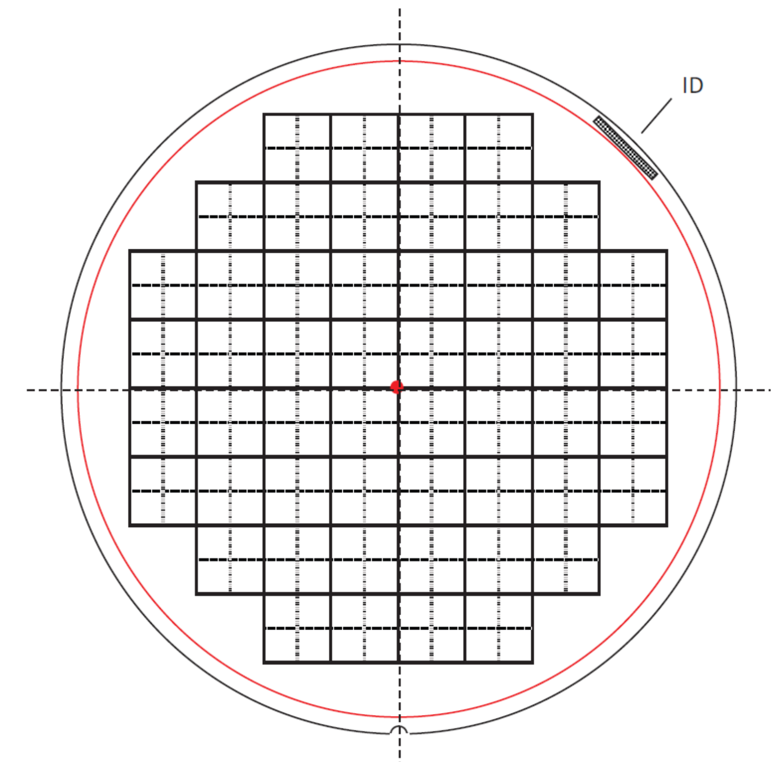
- **PIDTP Contents**
  - FC150 daisy chain flip chip test vehicle description
  - HDBU organic test substrate description
  - Underfill material description and outgassing results
  - Copper pillar wafer bumping Wafer Level Acceptance (WLA) analysis
  - FC150 copper pillar assembly reliability assessments
  - Solder bump wafer bumping Wafer Level Acceptance (WLA) analysis
  - FC150 solder bump assembly reliability assessments
  - Conclusions and Next Steps
  - Organic Class Y Poster Child

CAES PIONEERING ADVANCED ELECTRONICS

- **FC150 Flip Chip Daisy Chain Test Die**
  - 150µm I/O pitch daisy chain test vehicle
  - 10x10mm die size with 3,718 I/O per die
  - 200mm diameter wafer with 208 die per wafer





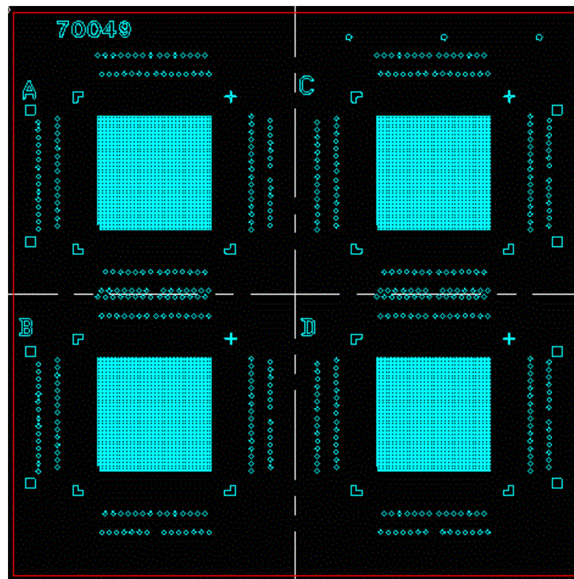


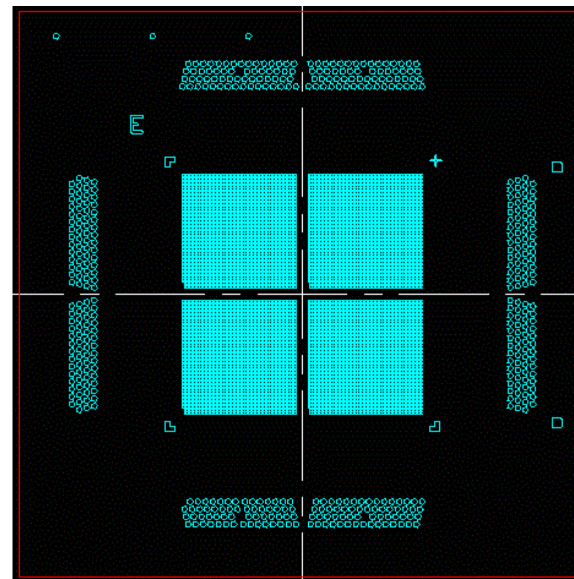
Organic Class Y Flip Chip PIDTP

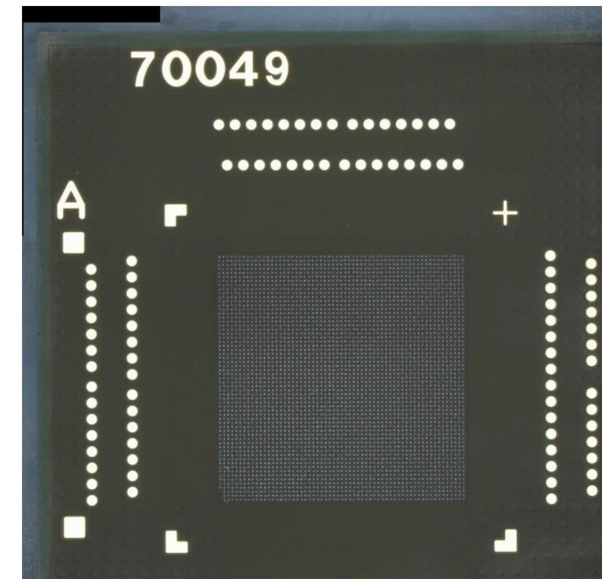
FC150 HDBU Organic Test Substrate

CAES PIONEERING ADVANCED ELECTRONICS

- **FC150 Flip Chip High Density Build-Up (HDBU) Test Substrate**
  - High Density Build-Up organic substrate technology
  - Dual-sided, 1.0mm thick, 45x45mm substrate size
  - 80µm solder mask defined pads with Electroless Nickel/Immersion Gold (ENIG) plating
  - Eutectic Sn/Pb solder-on-pad (SOP)
  - Four 10x10mm die sites per substrate







Organic Class Y Flip Chip PIDTP

FC150 HDBU Organic Test Substrate – Stack-up Definition (CAES Proprietary)

CAES PIONEERING ADVANCED ELECTRONICS

- **High Density Build-Up (HDBU) Stack-up**

DESIGN RULE TABLE & LAYER STRUCTURE

LAYER NAME	DESIGN RULE	THICKNESS	MATERIAL
EI (SOLDER RESIST)		21±10	
EL (LAYER 1)	90 DIA. (Via land) W15 G15	15±8	
DI (VIA)	50 DIA.	33±10	
DL (LAYER 2)	90 DIA. (Via land) W15 G30	15±8	
CI (VIA)	50 DIA.	33±10	
CL (LAYER 3)	90 DIA. (Via land) W15 G15	15±8	
BI (VIA)	50 DIA.	33±10	
BL (LAYER 4)	90 DIA. (Via land) W24 G20	15±8	
AI (VIA)	50 DIA.	33±10	
AL (LAYER 5)	125 DIA. (Via land) 250 DIA. (T/H land) W40 G50	20±10	
CORE (Through hole)	150 DIA.	800 NOM.	
ALB (LAYER 6)	125 DIA. (Via land) 250 DIA. (T/H land) W40 G47	20±10	
AIB (VIA)	50 DIA.	33±10	
BLB (LAYER 7)	90 DIA. (Via land) W32 G42	15±8	
BIB (VIA)	50 DIA.	33±10	
CLB (LAYER 8)	90 DIA. (Via land) W25 G15	15±8	
CIB (VIA)	50 DIA.	33±10	
DLB (LAYER 9)	90 DIA. (Via land) W33 G37	15±8	
DIB (VIA)	50 DIA.	33±10	
ELB (LAYER 10)	90 DIA. (Via land) W34 G29	15±8	
EIB (SOLDER RESIST)		25±10	
Through hole filling			IR10F
Copper thickness in via hole		FILLED VIA	
Copper thickness in through hole		10 MIN.	

W : MINIMUM PATTERN WIDTH
G : MINIMUM PATTERN CLEARANCE

DESIGN VALUE TABLE

ITEMS	DESIGN VALUE		TOLERANCE	COUNT
F/C PAD	S/R OPENING	71 DIA.	±20	5184
	METAL	101 DIA.	±20	
	MINIMUM PITCH	150		
BGA PAD	S/R OPENING	400 DIA.	±20	783
	METAL	450 DIA.	±20	

SURFACE FINISH

ITEMS		THICKNESS	MATERIAL
ELECTROLESS Ni PLATING		3 NOM.	Ni
ELECTROLESS Au PLATING		0.03 NOM.	Au

Cu LAYER TREATMENT

ITEM	REQUIREMENT
OTHER LAYERS	IMPROVED CZ
EXTERNAL LAYERS	STANDARD CZ

SOLDER EL DL CL BL AL CORE ALB BLB CLB DLB ELB EI DI CI BI AI AIB BIB CIB DIB EIB SOLDER

SOLDER PRECOAT SPECIFICATION

PRECOAT SIDE	PRECOAT POINT	THICKNESS	COINING DIAMETER	MATERIAL
TOP SIDE	F/C PAD	HIGHER THAN SOLDER RESIST	NO COINING	63Sn/37Pb SOLDER
BOTTOM SIDE	BGA PAD	410 NOM._ABOVE S/R	NO COINING	63Sn/37Pb SOLDER BALL (ø500)
NO PRECOAT OF OTHER POINTS				

WARPAGE SPECIFICATION

AREA	VALUE
OVERALL	150 MAX.
⚠ F/C AREA (ON SOLDER RESIST SURFACE)	25 (TARGET MAX)

(UNITS: μm)

CAES | 899 BGA x-2-x HDBU DETAIL DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS - MILLIMETERS THIRD ANGLE PROJECTION 2 DECIMALS - ±0.25 3 DECIMALS - ±0.13 4 DECIMALS - ±
AUTHOR MFoster
DATE 29-DEC-2021
REV 2 DRAWING# 40-76xxx-YY
SCALE na SIZE D SHEET 2 OF 2

- Substrate Core Material =
  - CTE = 22ppm/°C
- Conductor Material = Copper
- Dielectric Material =
- Solder Resist =
- Landing Pad Material = ENIG
- Solder on Pad = 63Sn/37Pb alloy
- BGA Ball = 63Sn/37Pb alloy

CAES PIONEERING ADVANCED ELECTRONICS

- **Underfill Material Properties and Outgassing**

ORS ONEIDA RESEARCH SERVICES, INC.

TEST REPORT
INTERNAL VAPOR ANALYSIS

8811 AMERICAN WAY • SUITE 100 • ENGLEWOOD, CO 80112 • PHONE: (315) 736-5480

JULIE LANDON
AEROFLEX COLORADO SPRINGS, INC.
4350 CENTENNIAL BLVD.
COLORADO SPRINGS, CO 80907
UNITED STATES

ORS REPORT NO. : 218346-004
DATE TESTED : 2/26/2016
QUANTITY TESTED : 5
PACKAGE TYPE : AEROFLEX 48-LD FP IC
MFG. CODE : 74111 (UNDEFILL ONLY)
LOT# EE5498-RGA

PO: SWO-228298
Rel. No:

SAMPLE ID		16	17	18	19	20			
ION SOURCE PRESSURE	torr	8.9E-6	8.0E-6	8.6E-6	8.3E-6	9.6E-6			
NITROGEN	%v	99.8	99.8	99.8	99.8	99.9			
OXYGEN	ppmv	ND	ND	ND	ND	ND			
ARGON	ppmv	263	267	261	272	257			
CO2	ppmv	156	183	160	177	125			
MOISTURE	ppmv	646	540	589	582	704			
HYDROGEN	ppmv	263	442	279	267	183			
METHANE	ppmv	ND	ND	ND	ND	ND			
AMMONIA	ppmv	ND	ND	ND	ND	ND			
HELIUM	ppmv	ND	ND	ND	ND	ND			
FLUORO-CARBONS	ppmv	ND	ND	ND	ND	ND			
METHANOL	ppmv	209	309	263	273	224			

COMMENTS:

ND = None Detected
1% = 10,000 ppm

Tested per ORS SOP MEL-1018: "DLA Land and Maritime Suitability for Military Devices - Internal Gas Analysis"
All samples were prebaked 16 - 24hrs. @ 100°C prior to analysis.
Samples were tested at 100°C.

PIDTP Material Properties

- CTE = 22ppm/°C (below Tg)
- CTE = 80ppm/°C (above Tg)
- Tg = 115°C
- Thermal Conductivity = 0.52W/m-K

Moisture Outgassing Results

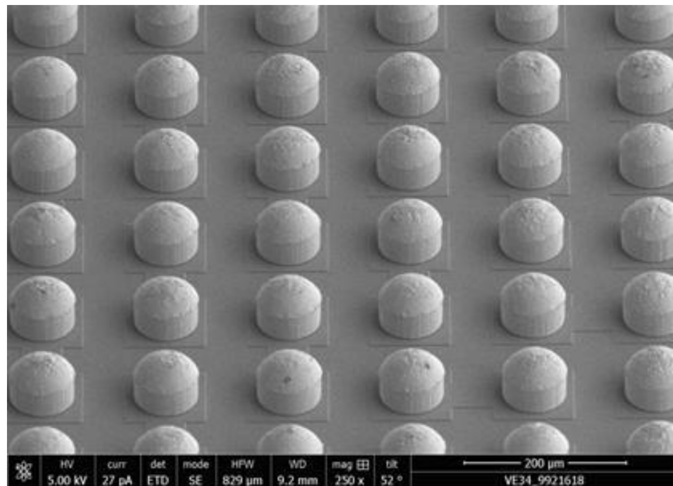
- MIL-STD-883 TM1018
  - Moisture = 612ppm
- ASTM E-595
  - TML = 0.28%
  - CVCM = 0.01%
  - WVR = 0.12%

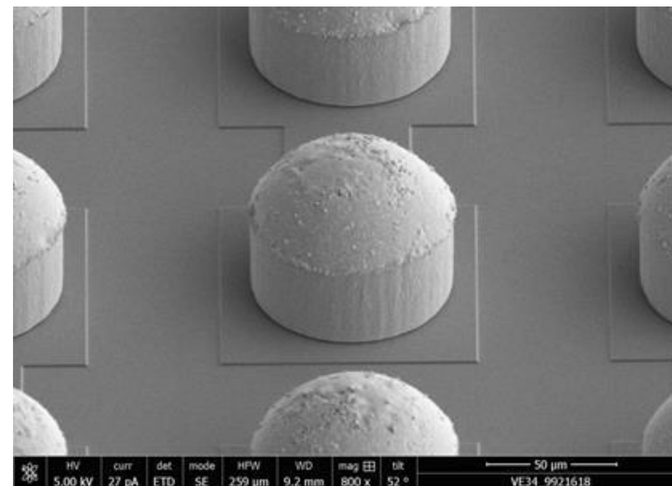
Copper Pillar Wafer Level Acceptance (WLA)

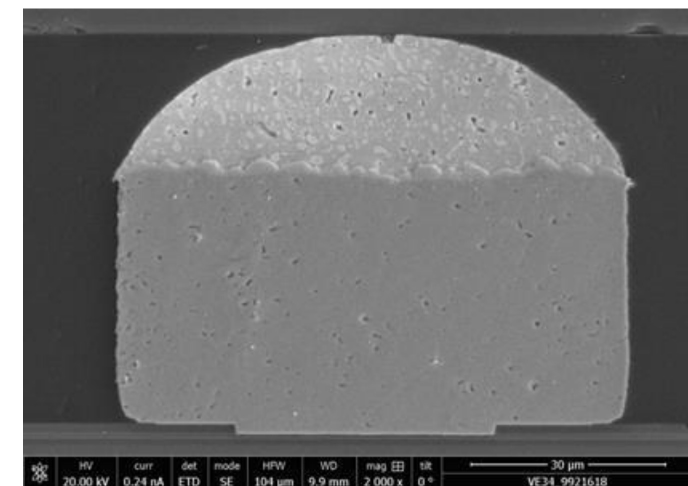
FC150 Copper Pillar Construct

CAES PIONEERING ADVANCED ELECTRONICS

- **FC150 Test Die Copper Pillar**
  - 40µm octagonal passivation opening
  - 80µm diameter electroplated Ti/Cu/Ni under bump metallurgy (UBM)
  - 80µm diameter copper pillar
  - 40µm copper pillar bump height with 25µm eutectic 63Sn/37Pb solder cap







Copper Pillar Wafer Level Acceptance (WLA)

FC150 Copper Pillar WLA Results

CAES PIONEERING ADVANCED ELECTRONICS

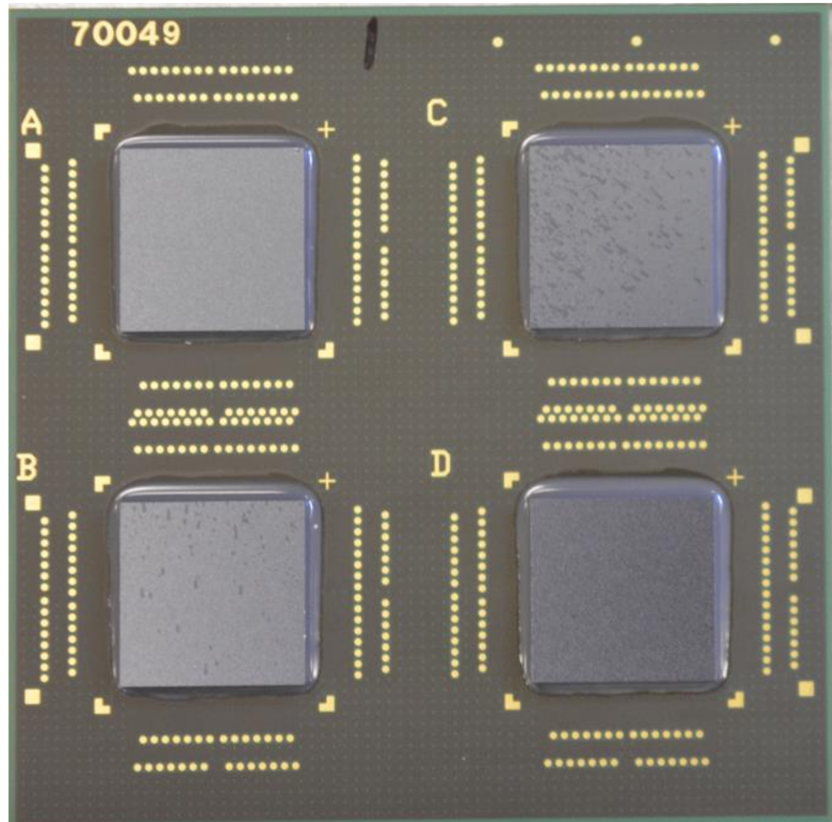
- **FC150 Test Die Copper Pillar – WLA Criteria and Results**
  - FC150 Wafer ID’s SI833-0020-10-D5 and SI833-0021-01-A7

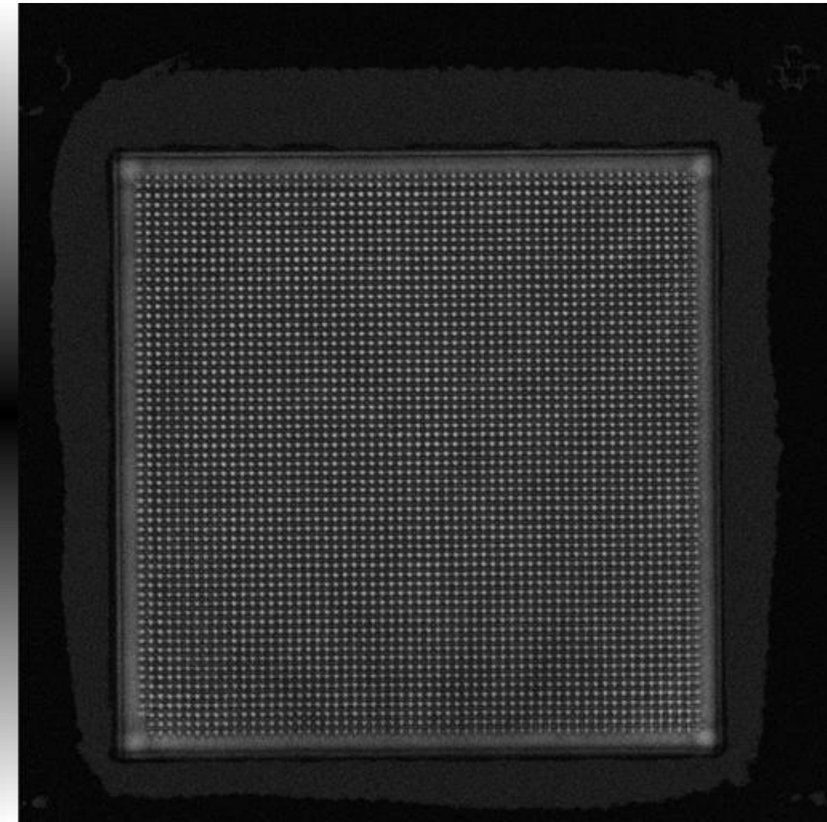
Test Type	Test Method	Criteria	Status
Wafer Level Acceptance	Bump Yield • Automated optical inspection	Bump defect rate < 200 ppm	< 5 ppm
Wafer Level Acceptance	Bump Height • Automated optical inspection	Nominal +/- 15 μm	Cpk = 1.4
Wafer Level Acceptance	Bump Shear • JESD22-B117A	Minimum load of 3 mg/μm^2	Cpk = 9.5

FC150 Copper Pillar PIDTP Reliability Assessments

FC150 Copper Pillar Flip Chip Assembly

- **FC150 Assembly Monitor – Visual Inspection and CSAM**
  - Good underfill fillet formation with minimal underfill dispense bleedout
  - No underfill voids detected via CSAM inspection



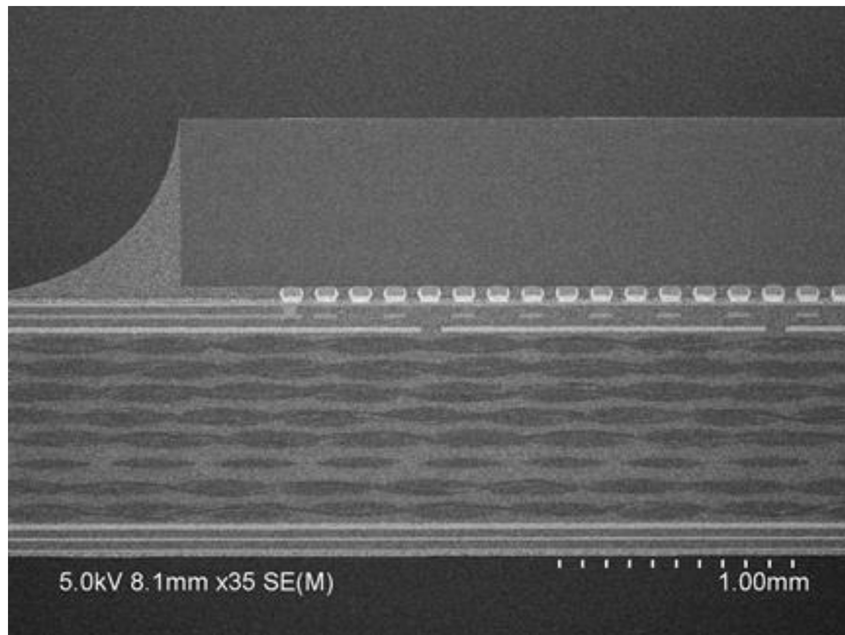


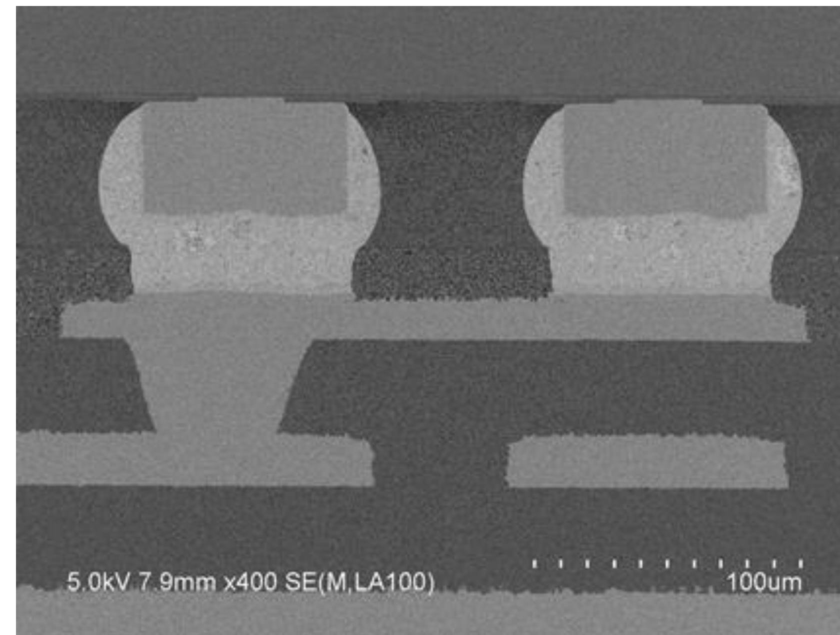
FC150 Copper Pillar PIDTP Reliability Assessments

FC150 Copper Pillar Flip Chip Assembly

CAES PIONEERING ADVANCED ELECTRONICS

- **FC150 Assembly Monitor – Cross Section SEM**
  - Excellent solder joint wetting and formation; no defects detected
  - Flux formulation enables wicking up copper pillar for enhanced reliability
  - No underfill defects detected





FC150 Copper Pillar PIDTP Reliability Assessments

FC150 Copper Pillar Flip Chip Reliability Assessments

CAES PIONEERING ADVANCED ELECTRONICS

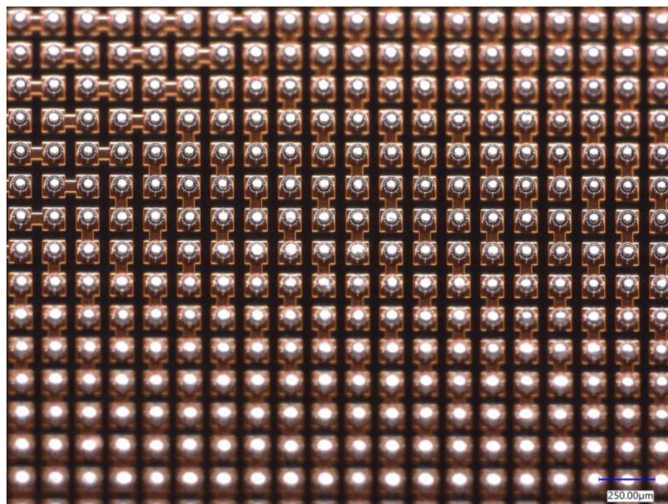
- **Condition B Temperature Cycle Testing (-55/125°C)**
  - Parts assembled with underfill
  - 4000 cycles, no failures detected
- **125°C High Temperature Storage**
  - Parts assembled with underfill
  - 4000 hours, no failures detected
- **150°C High Temperature Storage**
  - Parts assembled with underfill
  - 4000 hours, no failures detected
- **Multiple Reflow Testing**
  - Parts assembled with underfill
  - 10 reflow exposures, no failures detected
- **Moisture Loading**
  - Parts assembled with underfill
  - 1000 hours 85°C/85%RH, no failures detected

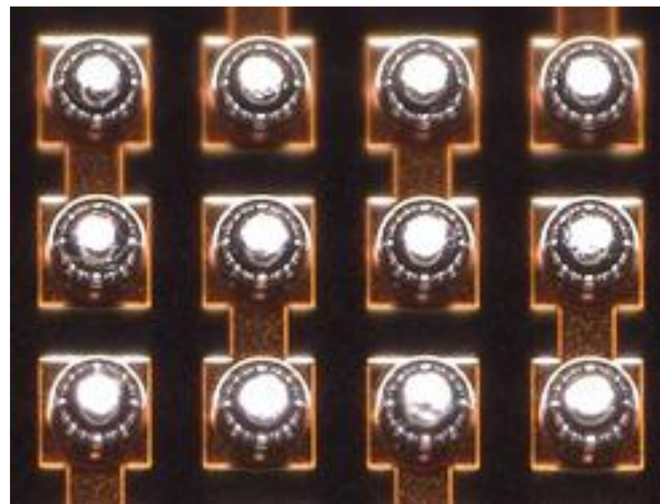
Solder Bump Wafer Level Acceptance (WLA)

FC150 Solder Bump Construct

CAES PIONEERING ADVANCED ELECTRONICS

- **FC150 Test Die Solder Bump**
  - 150μm I/O pitch daisy chain test vehicle
  - 10x10mm die size with 3,718 I/O
  - 40μm octagonal passivation opening
  - Polyimide re-passivation layer with 30μm diameter openings
  - 65μm diameter electroplated Ti/Cu/Ni under bump metallurgy (UBM)
  - 70μm eutectic 63Sn/37Pb solder bump





Solder Bump Wafer Level Acceptance (WLA)

FC150 Solder Bump WLA Results

CAES PIONEERING ADVANCED ELECTRONICS

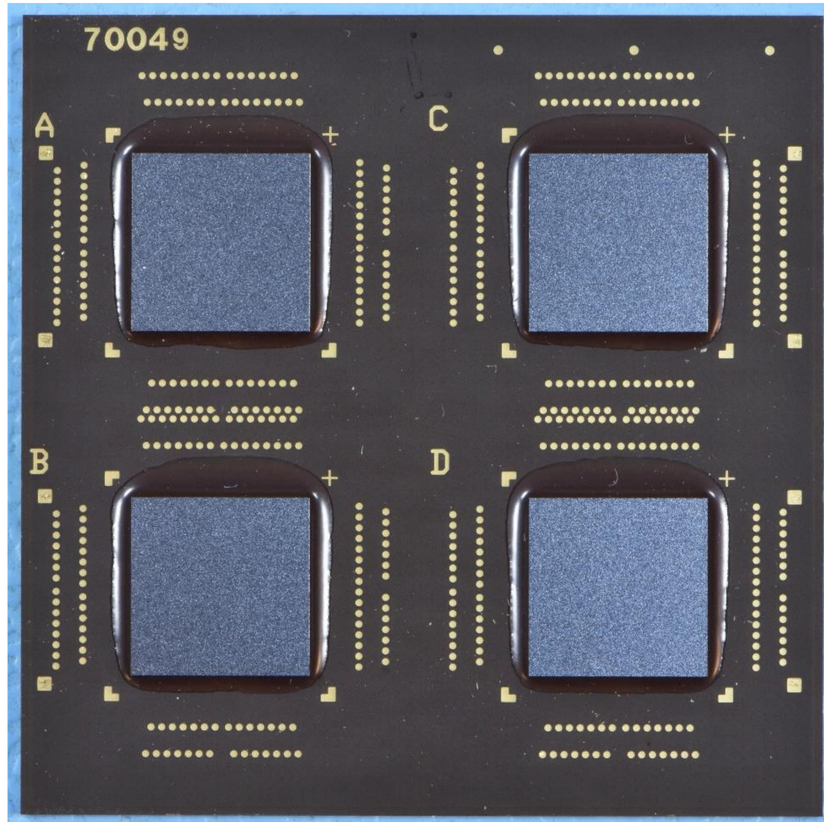
- **FC150 Wafer Level Acceptance – Criteria and Results**
  - FC150 Wafer ID's SI8E3-0021-04-A5, SI8E3-0021-03-F5, SI8E3-0021-02-D2

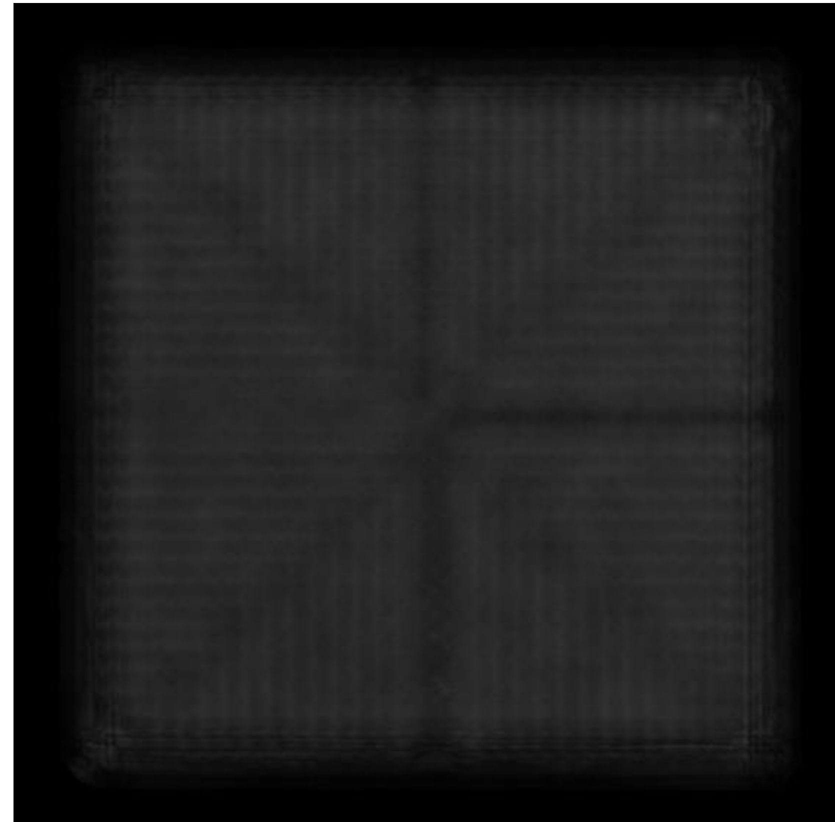
Test Type	Test Method	Criteria	Status
Wafer Level Acceptance	Bump Yield • Automated optical inspection	Bump defect rate < 200 ppm	< 20 ppm
Wafer Level Acceptance	Bump Height • Automated optical inspection	Nominal +/- 15 µm	Cpk = 1.5
Wafer Level Acceptance	Bump Shear • JESD22-B117A	Minimum load of 3 mg/µm^2	Cpk = 5.9

FC150 Solder Bump PIDTP Reliability Assessments

FC150 Solder Bump Flip Chip Assembly

- **FC150 Assembly Monitor – Visual Inspection**
  - Good underfill fillet formation with minimal underfill dispense bleedout
  - No underfill voids detected via CSAM inspection

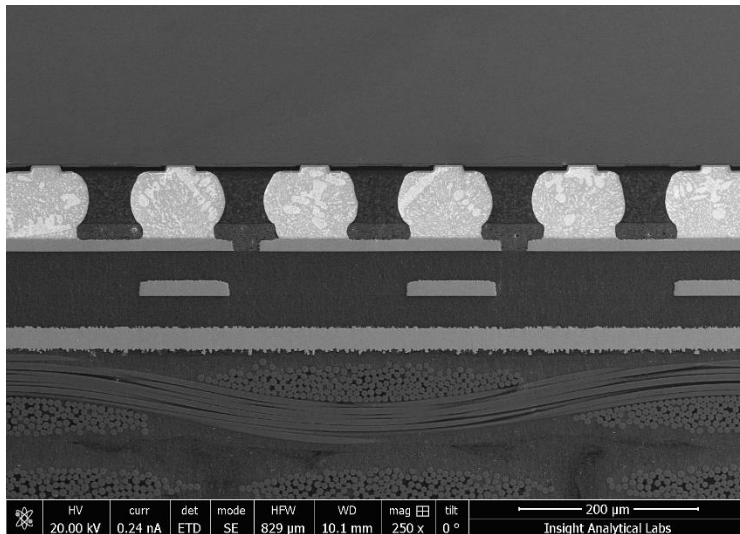


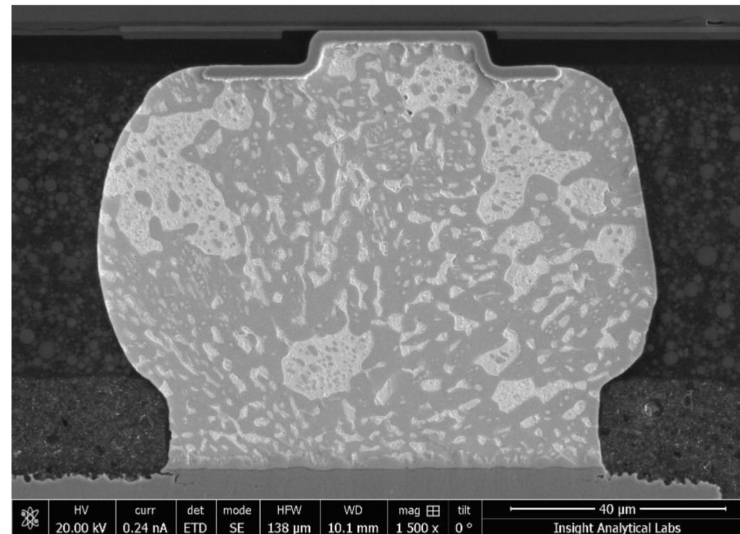


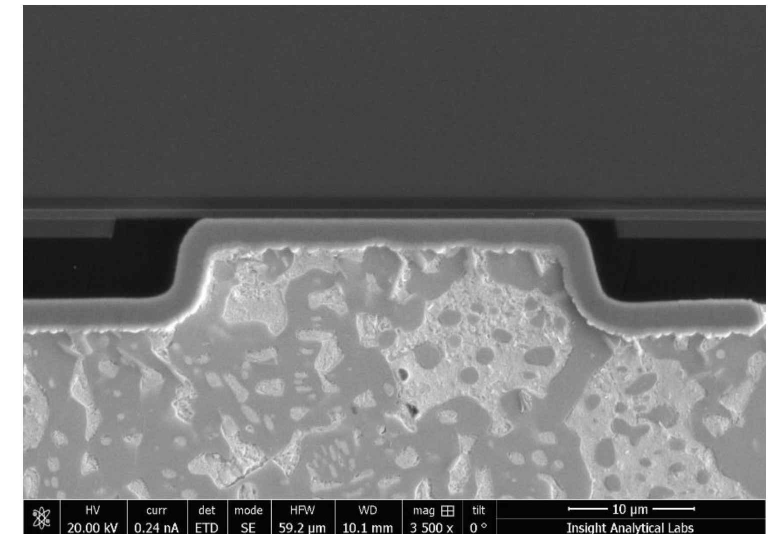
FC150 Solder Bump PIDTP Reliability Assessments

FC150 Solder Bump Flip Chip Assembly

- **FC150 Assembly Monitor – Cross Section SEM**
  - Excellent solder joint wetting and formation; no defects detected
  - No underfill defects detected







FC150 Solder Bump PIDTP Reliability Assessments

FC150 Solder Bump Flip Chip Reliability Assessments

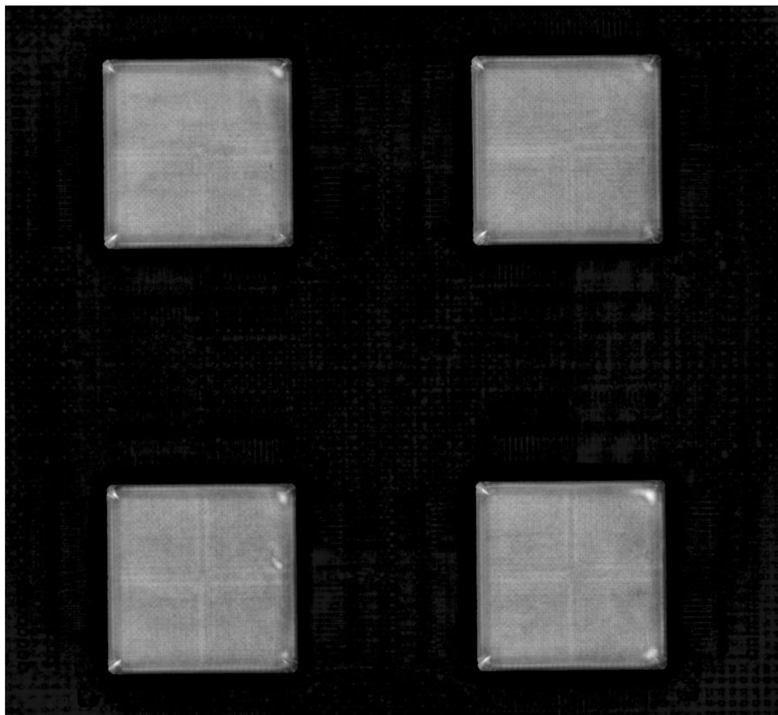
CAES PIONEERING ADVANCED ELECTRONICS

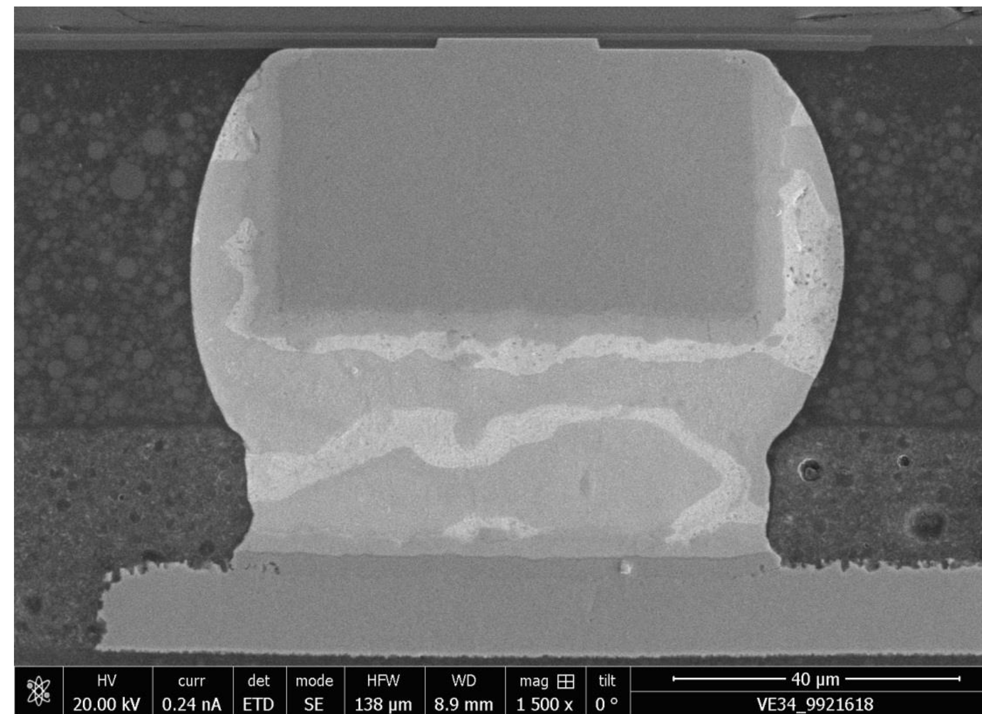
- **Condition B Temperature Cycle Testing (-55/125°C)**
  - Parts assembled with underfill
  - 5000 cycles, no failures detected; extended testing to 8000 cycles (3 failures detected)
- **125°C High Temperature Storage**
  - Parts assembled with underfill
  - 4000 hours, no failures detected
- **150°C High Temperature Storage**
  - Parts assembled with underfill
  - 4000 hours, no failures detected
- **Multiple Reflow Testing**
  - Parts assembled with underfill
  - 10 reflow exposures, no failures detected
- **Multiple Reflows followed by Condition B Temperature Cycle Testing**
  - Parts assembled with underfill
  - 5000 cycles, no failures detected

FC150 Copper Pillar PIDTP Reliability Assessments

Temperature Cycle Testing – Sample Failure Analysis

- **Condition B Temperature Cycle Testing (-55/125°C)**
  - CSAM and Cross section analysis after 4000 cycles (zero failures)
  - No indication of underfill delamination; no evidence of underfill voids
  - Significant grain coarsening within solder joint (expected)



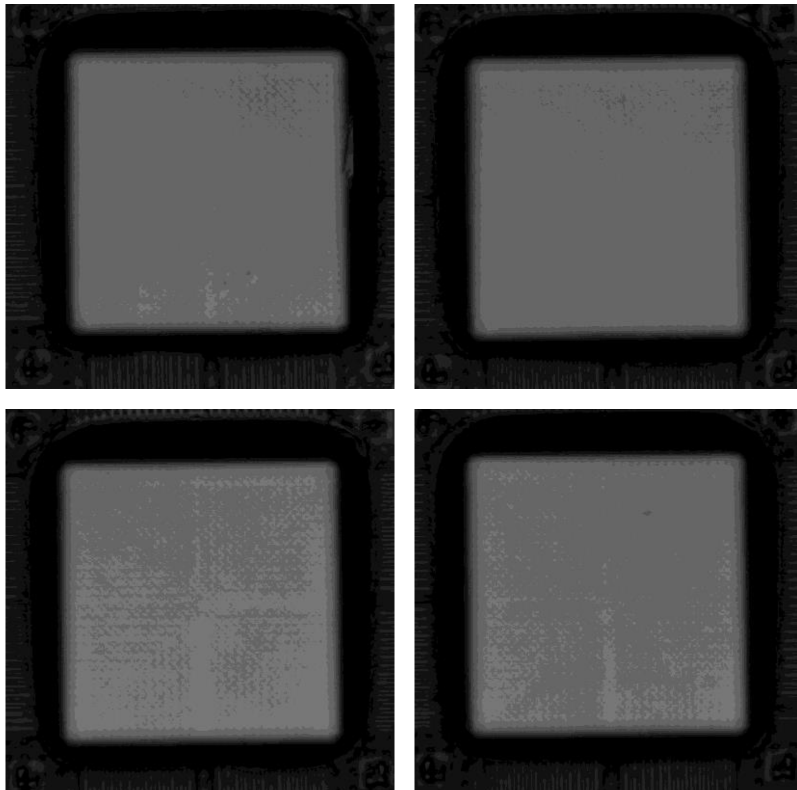


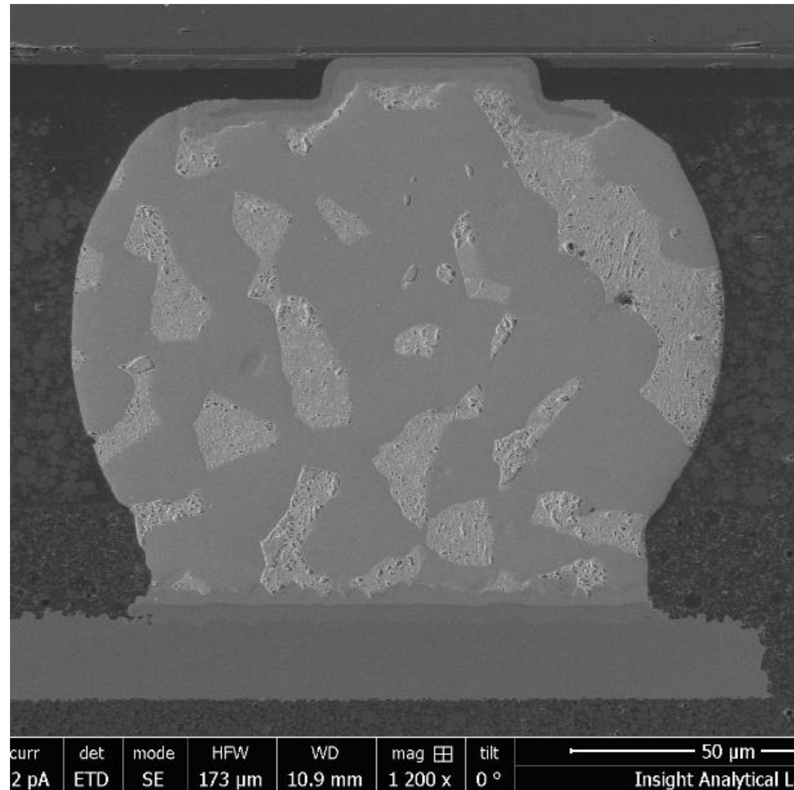
FC150 Solder Bump PIDTP Reliability Assessments

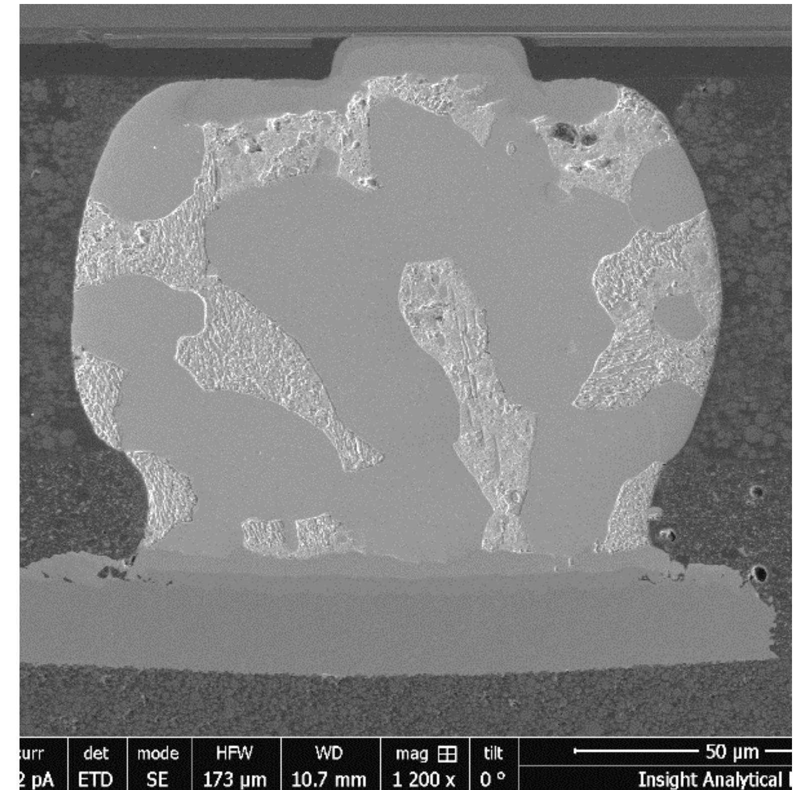
High Temperature Storage Testing – Sample Failure Analysis

CAES PIONEERING ADVANCED ELECTRONICS

- **125°C and 150°C High Temperature Storage**
  - CSAM and Cross section analysis after 2000 hours; extended testing to 4000 hours (zero failures)
  - No indication of underfill delamination; no evidence of underfill voids
  - Grain coarsening within solder joint and IMC growth (expected)







Organic Class Y Flip Chip PIDTP

Conclusions and Next Steps

CAES PIONEERING ADVANCED ELECTRONICS

- **Conclusions**
  - CAES has completed flip chip on organic PIDTP documentation and reliability assessments per MIL-PRF-38535, utilizing its FC150 test vehicle
  - PIDTP documentation and reliability assessments have been completed for both copper pillar and solder bump flip chip interconnect constructs
  - CAES has qualified wafer bumping supplier for copper pillar and solder bump wafer bumping for Organic Class Y products

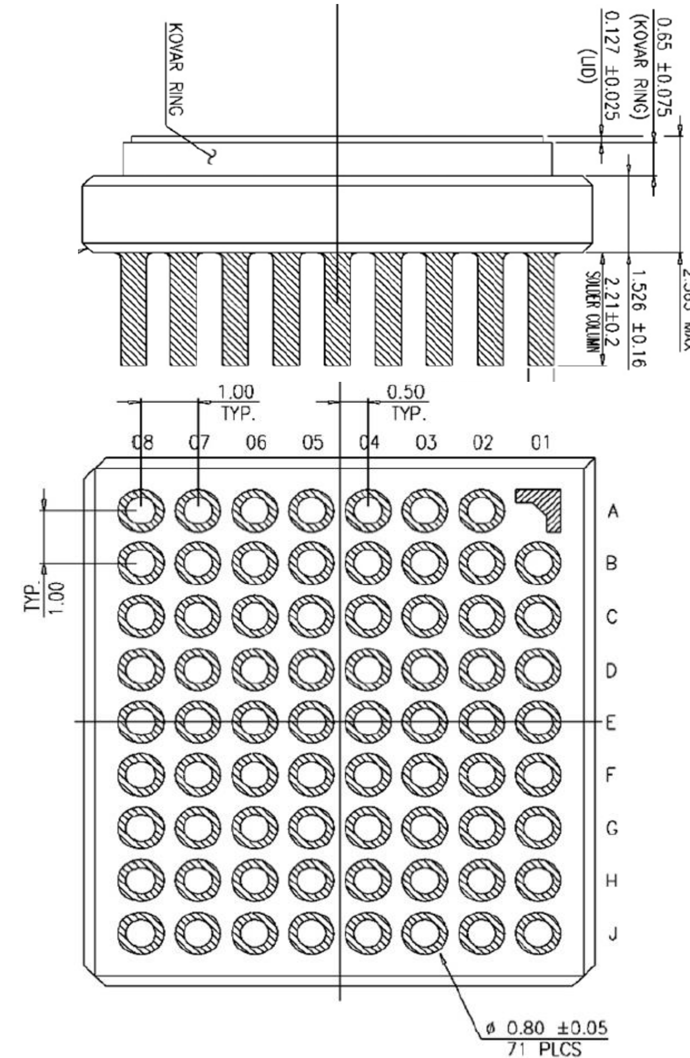
- **Next Steps**
  - DLA audit of CAES Colorado Springs facility to certify for Organic Class Y flip chip manufacturing
    - Scheduled for July 19-21; goal is conditional certification pending release of MIL-PRF-38535 Rev M
  - DLA audit of wafer bumping facility to allow for QML wafer bumping of CAES products
    - Target second half of 2022

CAES Organic Class Y Poster Child – High Speed LVDS Standard Product conversion from Hermetic Flip Chip QML-V to Organic Class Y

Organic Class Y Poster Child

CAES High Speed LVDS Standard Product

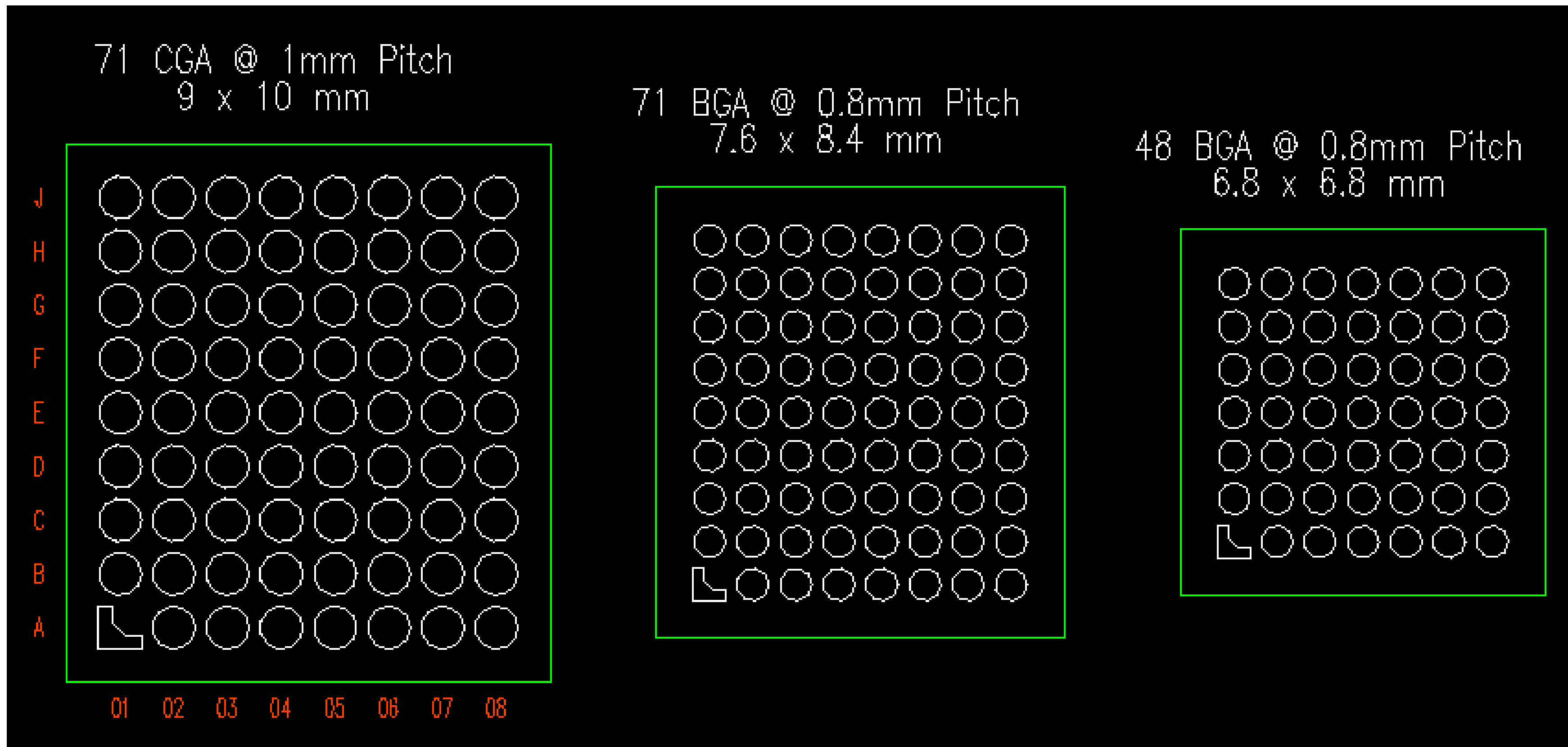
- **71 I/O Ceramic Column Grid Array Package**
  - CAES High Speed LVDS Standard Product
  - Hermetic flip chip QML-V package configuration



Organic Class Y Poster Child

CAES High Speed LVDS Standard Product

- **High Speed LVDS footprint shrink to 48 I/O BGA Organic Class Y Package**
  - Organic Class Y footprint shrink utilizes 0.8mm pitch and no seal ring requirement
  - Significant reduction in footprint area and mass with Organic Class Y configuration



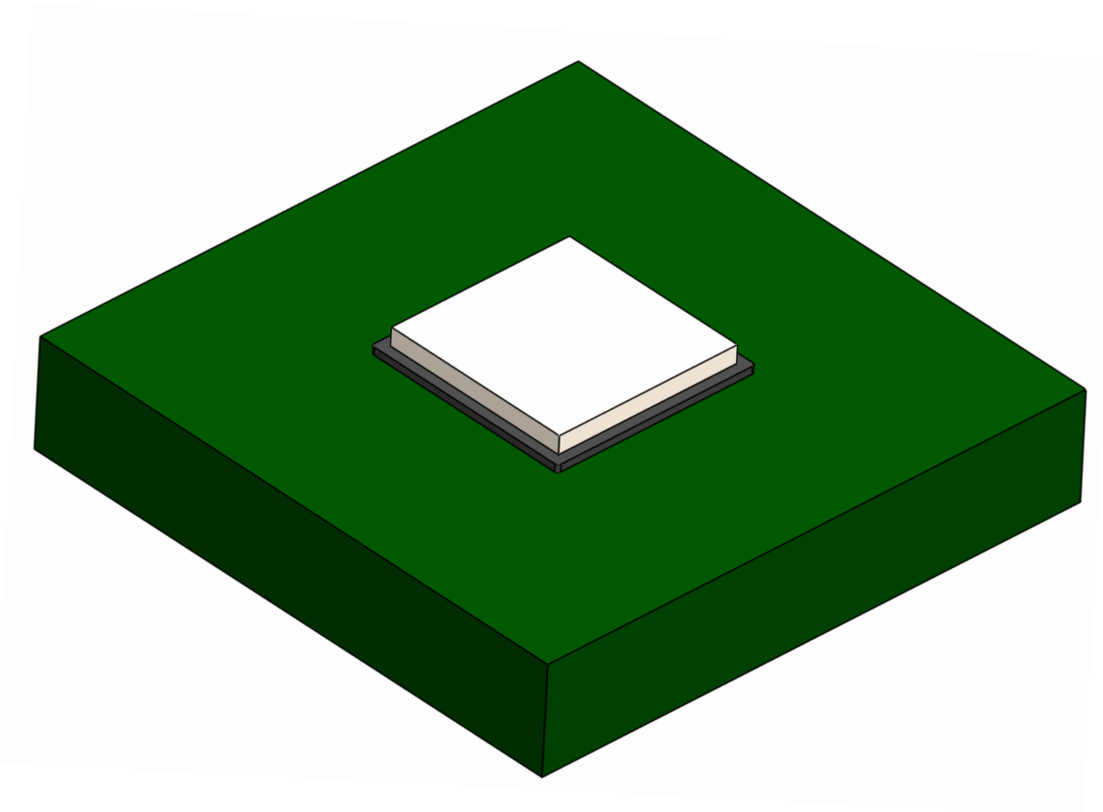
~50% reduction in footprint area

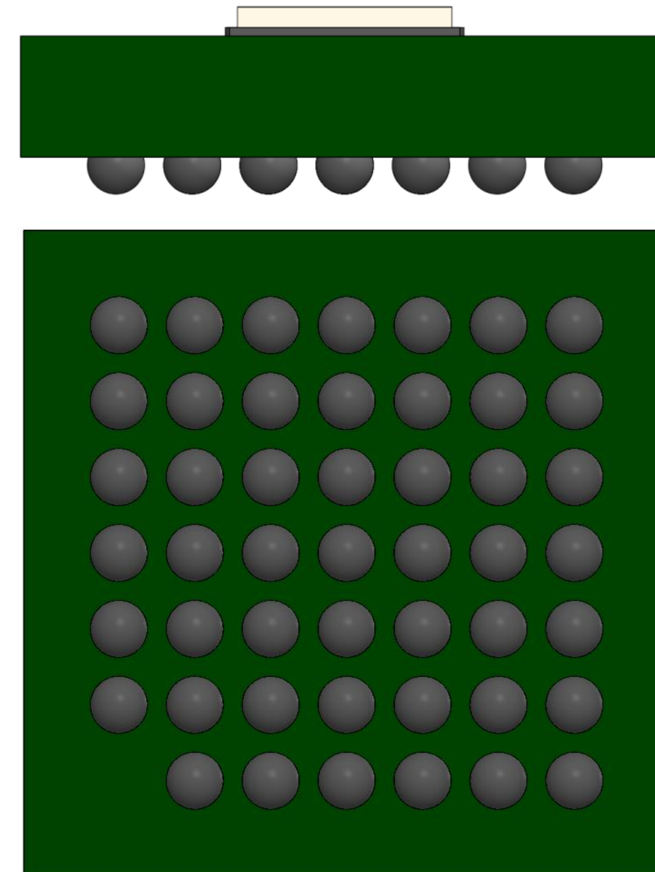
~75% reduction in mass

Organic Class Y Poster Child

CAES High Speed LVDS Standard Product

- **High Speed LVDS in Organic Class Y package configuration**
  - Lower package and manufacturing cost, higher assembly yield
  - Smaller package footprint and overall mass compared to ceramic





Questions?