Development of SEB-Immune High Voltage SiC Power Devices for Lunar Applications

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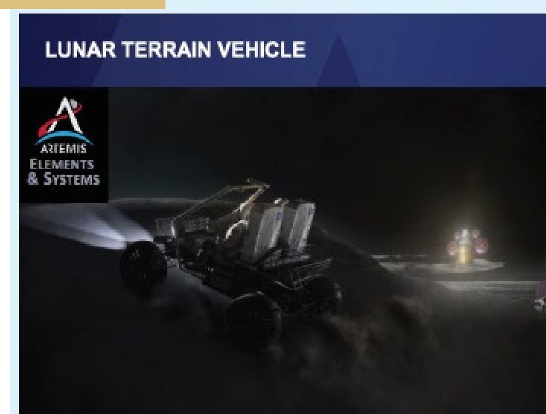
NASA Lunar Surface Technology Research (LuSTR)

Vanderbilt Engineering

Next-gen spacecraft and lunar transportation require orders-of-magnitude more power!



NASA's Lunar Exploration Program Overview Sept.2020

Relative Capabilities of Si, SiC, GaN

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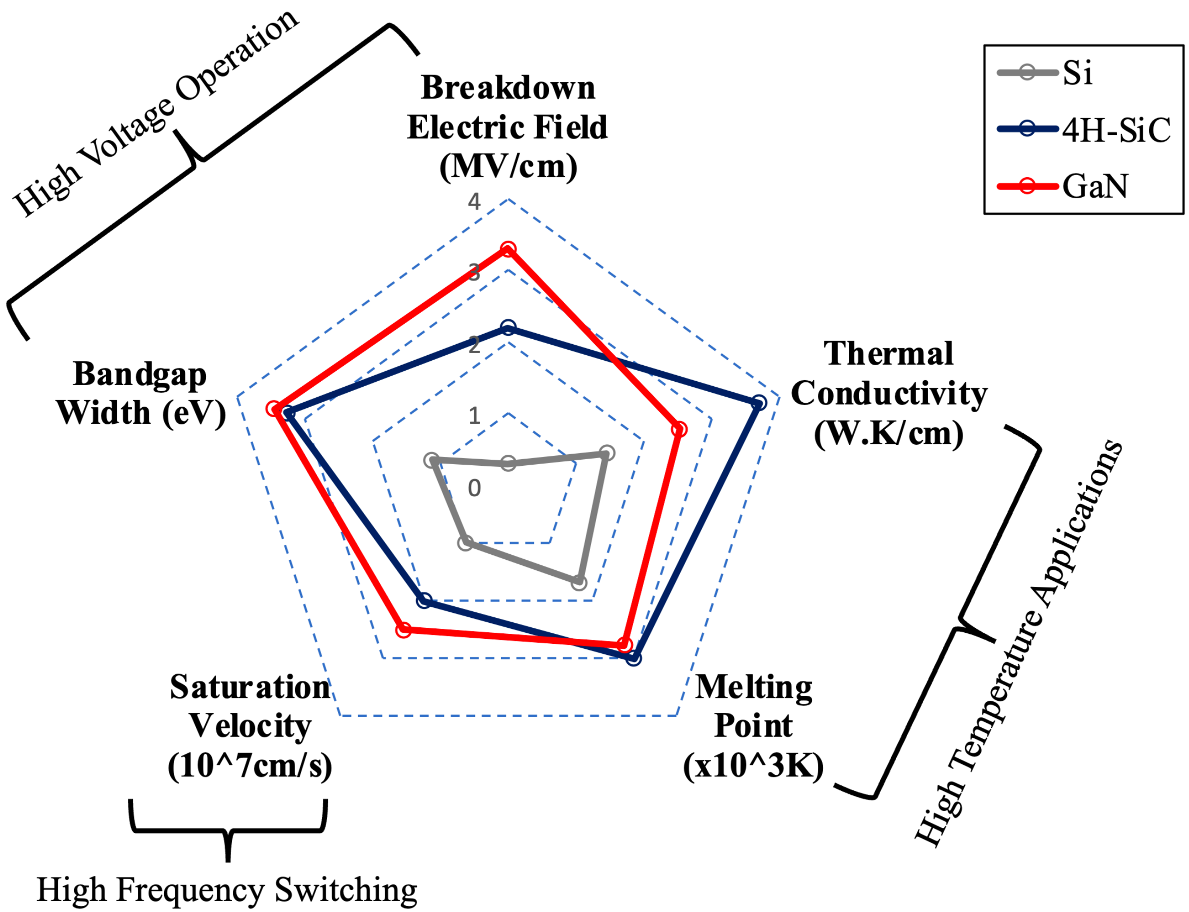
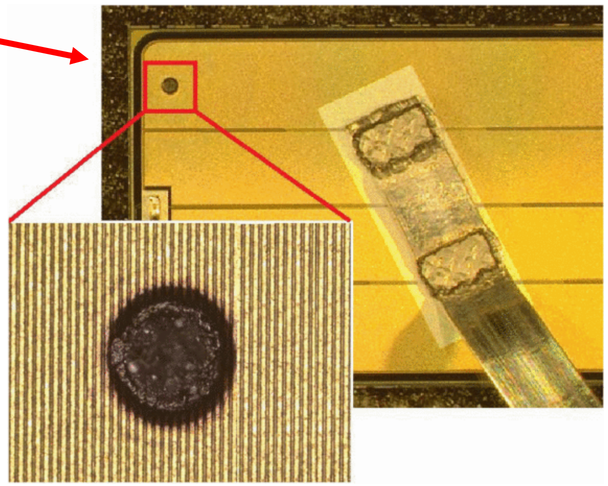


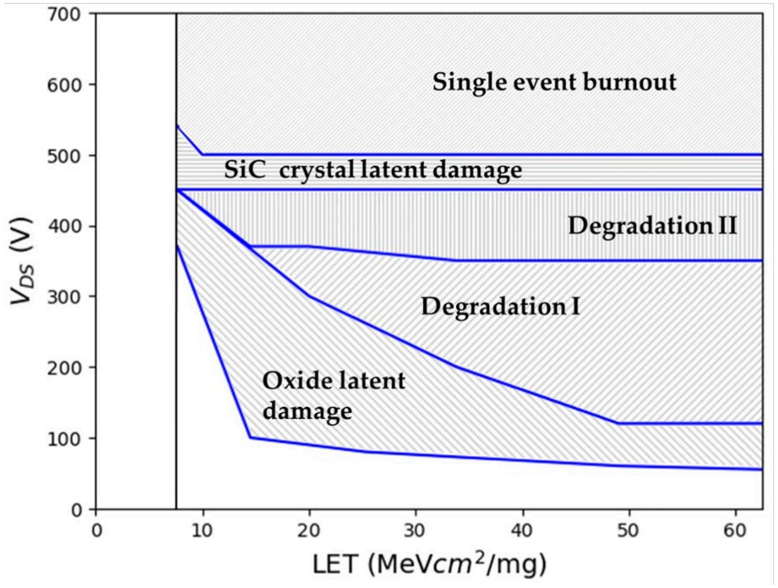
After T.P Chow, et al, IEEE TED, 2017 quoted in A. Sengupta, ProQuest Dissertation Publishing, 2021.

Radiation Effects in SiC Power Devices

- Total Ionizing Dose (TID) – charge trapped in insulating layers
  - Parametric shifts in device electrical characteristics (i.e., threshold voltage)
- Single Event Effects – ions deposit charge in active device regions
  - Transient current/voltage pulses
  - ***Parametric shifts in leakage currents***
  - ***Single event burnout (SEB) - catastrophic***
  - ***Single event gate rupture (SEGR) - catastrophic***

From: G. Consentino et. al, 2014 IEEE Applied Power Electronics Conference and Exposition





Overview of the different types of damage induced by heavy-ion in 1200V SiC power MOSFETs as a function of the ion LET from C. Martinella et. al, Microelectronics Reliability, Jan 2022.

Power Device – Safe Operating Area (SOA)

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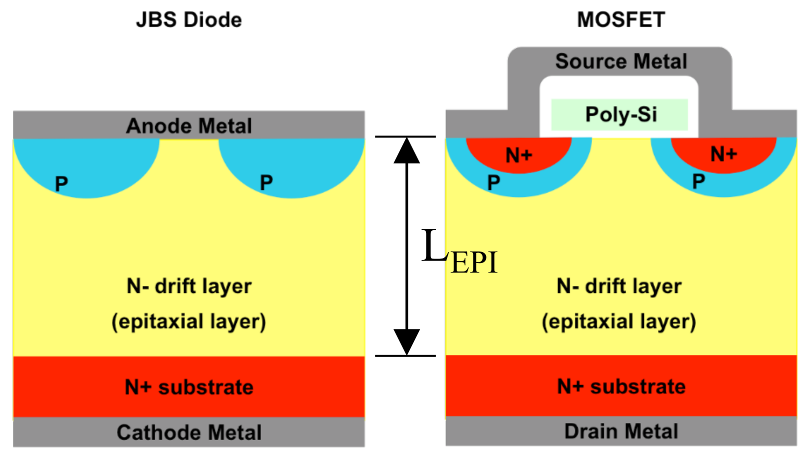
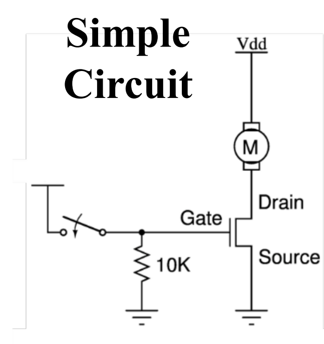
- Vertical power device
  - Suitable for diodes and MOSFETs
  - Vertical current flow
  - Performance dominated by epitaxial region resistance, R_{ON}

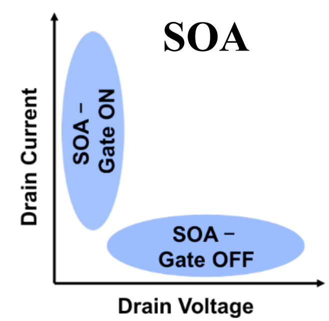
Doping Density ≈ e14's-e16's
L_{EPI} ≈ 10's-100's µm



$$R_{ON} = \rho * L_{EPI}/A_{EPI}$$

$$\text{Power} = I^2 * R_{ON}$$





Power Device – Ion-Induced Operating Area

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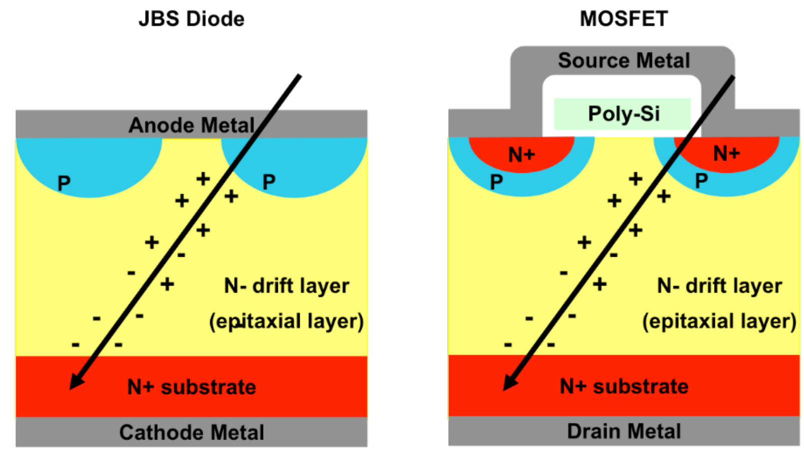
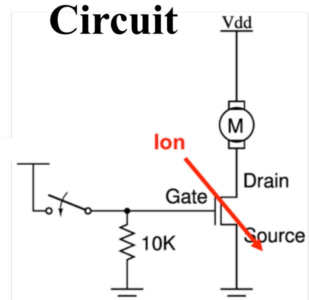
- Ion strike
  - Deposits charge along track
  - Vertical current flow
  - Creates resistive shunt between source and drain
  - Thermal damage occurs at the metal-semiconductor interface, and in crystal lattice

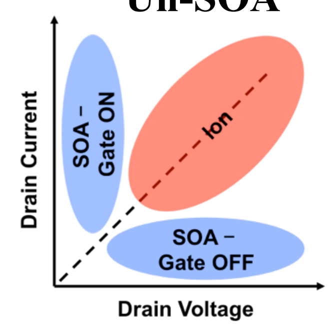
Ion Density ≈ e18's-e20's
L_{ION} ≈ 10's-100's μm



Simple Circuit



Un-SOA



$$R_{ION} = \rho_{ION} * L_{ION}/A_{ION}$$

$$\text{Power} = I_{ION}^2 * R_{ION}$$

LuSTR SiC Program

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Electrical Performance:

- SEE-tolerant SiC power diodes: Minimum 1200 V, 40 A, with maximum recovery time of 40 ns
- SEE-tolerant SiC power transistors: Normally off (enhancement mode), minimum 600 V, 40 A, $R_{ds\_on} < 24\ m\Omega$ while preserving low switching losses.

Radiation Goal:

- No heavy-ion induced permanent destructive effects upon irradiation while in blocking configuration (in powered reverse-bias/off state) with ions having a silicon-equivalent surface incident linear energy transfer (LET) of 40 MeV-cm^2/mg of sufficient energy to maintain a rising LET level throughout the epitaxial layer(s).

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Design of SEB-Immune Diode/MOSFET

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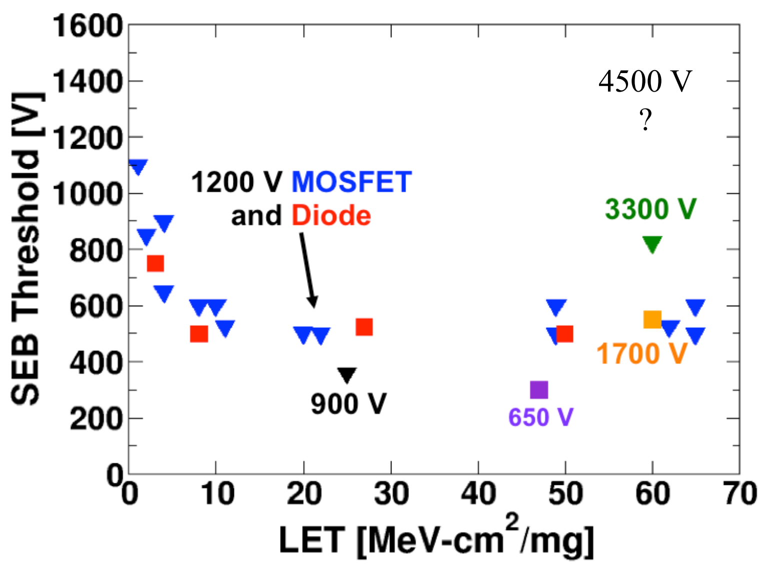
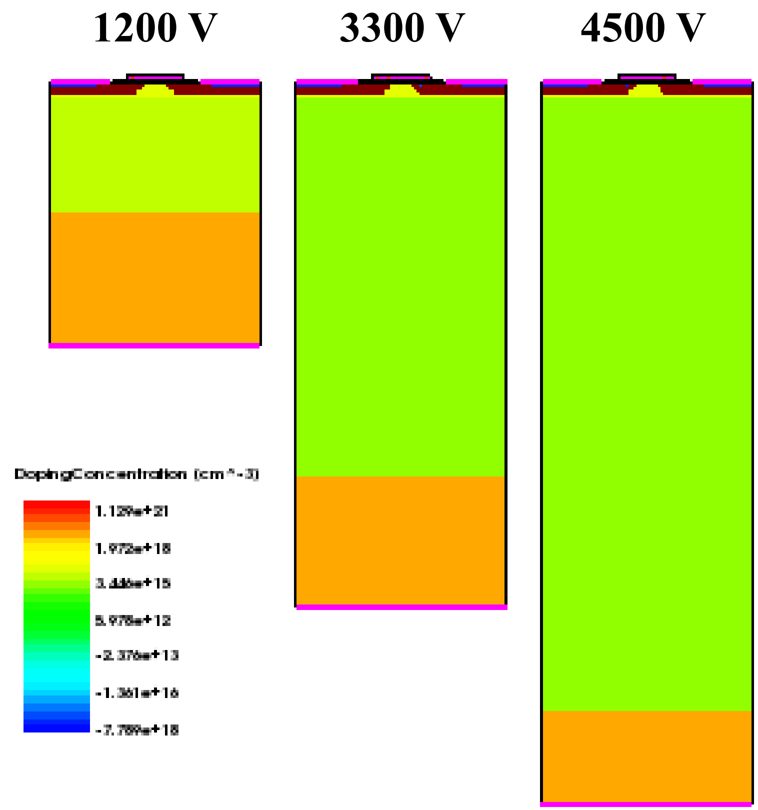
- VU and GE design device intended to survive catastrophic SEB
- 3D TCAD heavy ion sensitivity study – VU
  - Increase epi thickness
  - Decrease epi doping
  - Effective increase in voltage rating
  - Note: **3300 V device shows SEB @ 850V**

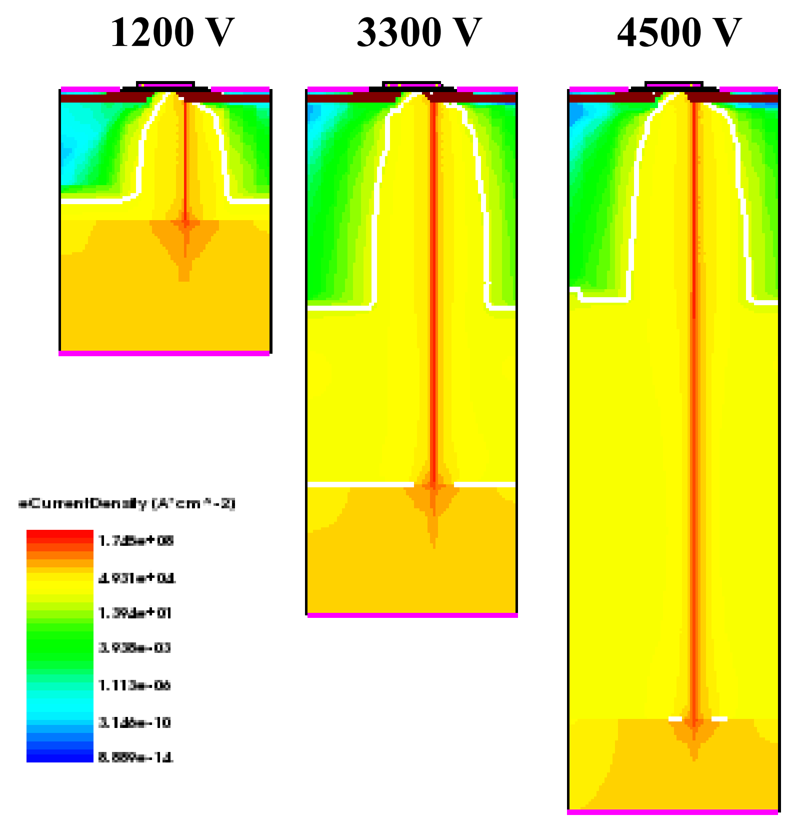




Ion-Induced Electron Current Density

3D TCAD heavy ion simulation of SiC MOSFET variants

- LET = 60 MeV-cm^2/mg @ 500 V
- **3300 V and 4500 V devices show significantly lower electric fields** compared to the 1200 V device
- Current densities similar for all variants



Ion-Induced Electric Field Redistribution

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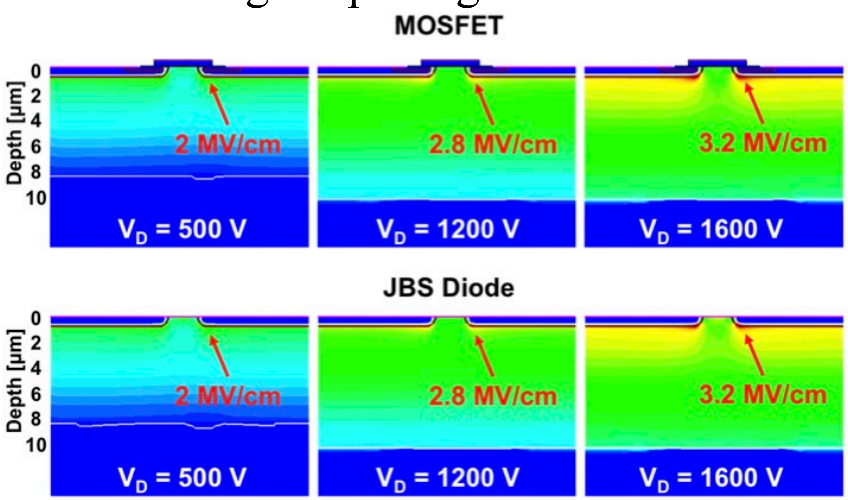
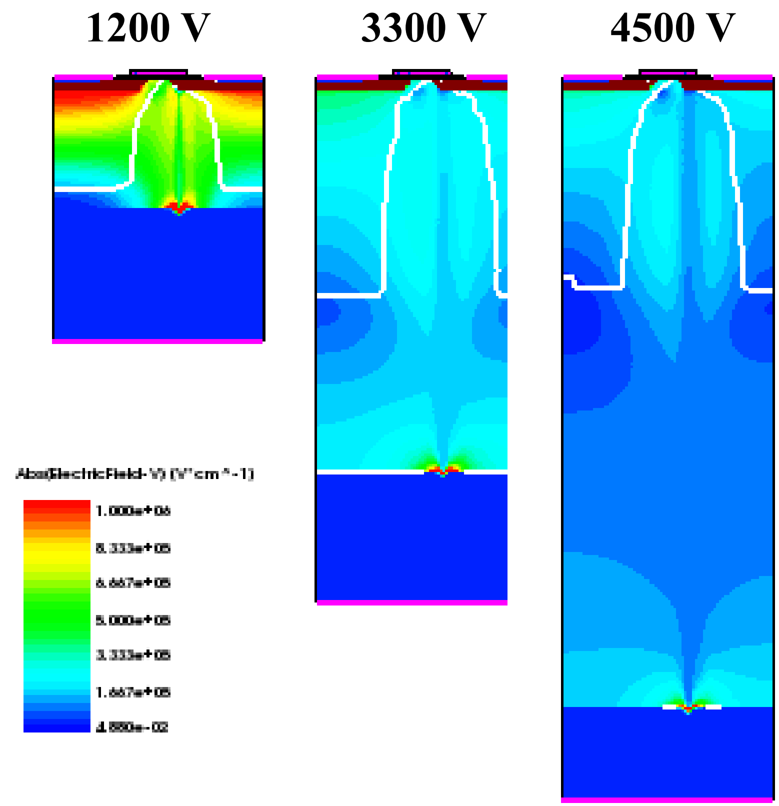
3D TCAD heavy ion simulation of SiC MOSFET variants

- LET = 60 MeV-cm^2/mg @ 500 V
- **3300 V and 4500 V devices show significantly lower electric fields** compared to the 1200 V device
- Power density $(\vec{J} \cdot \vec{E})$ is much lower with the longer Epi length at back interface



2D-cutplanes of the internal electric field for 1200V MOSFET and diode, when biased at 500 V, 1200 V, and 1600 V after D.R. Ball, VU Dissertation, 2020



Design of SEB-Immune Diode/MOSFET

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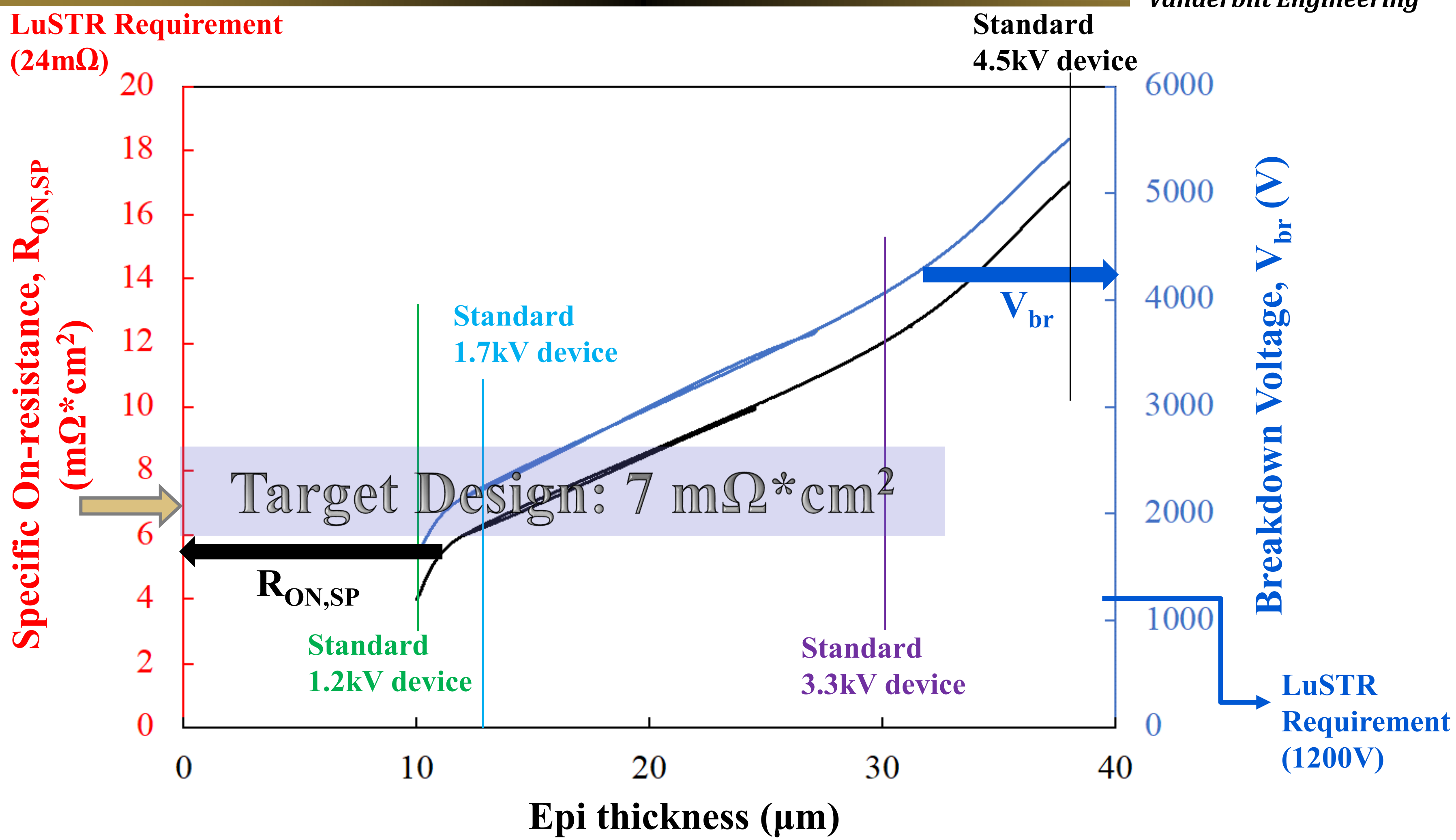

4.5kV devices should meet all LuSTR requirements

Target design should meet all LuSTR requirements with lower on resistance

Experiment: Ion beam testing of 1200 V SiC Heavy Ion Irradiation With Short Range Ions

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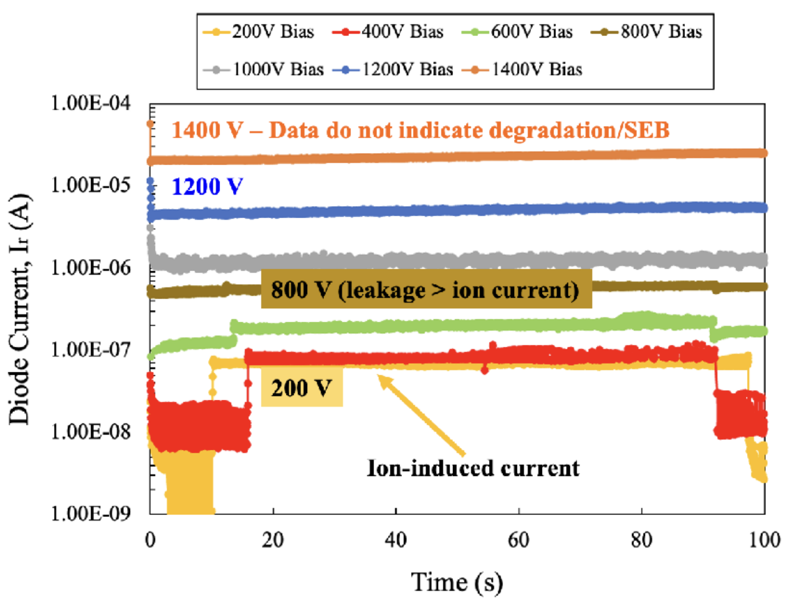
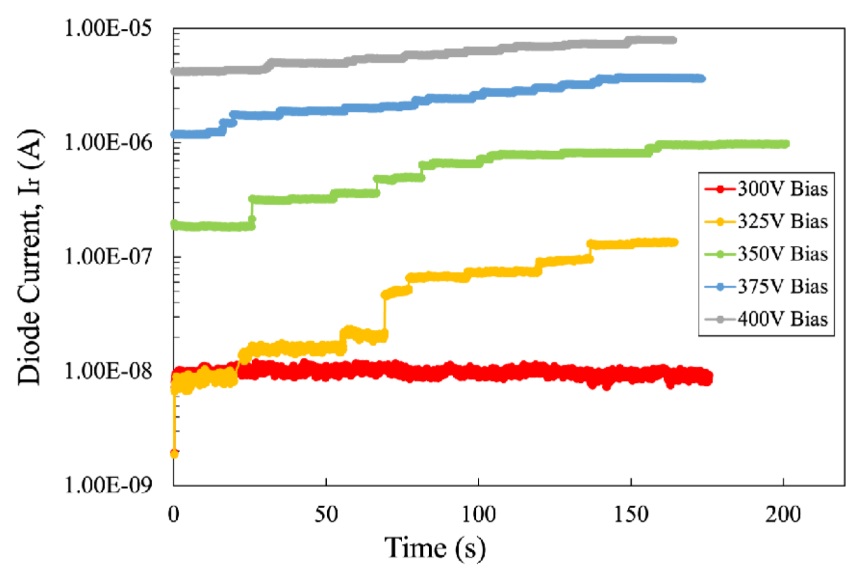
- Heavy ion radiation testing of 1200 V SiC diode with 10 µm thick epi layer
  - Ion LET = 7 MeV-cm^2/mg with range of 6 µm performed at VU Pelletron
  - ***Device shows no ion-induced leakage, nor catastrophic SEB***
  - ***Supports concept of increasing epitaxial layer thickness, also has implications for SEB rates due to angular effects***

Accepted for poster at NSREC 2022

VU Pelletron Irradiation - short range ions



TAMU Cyclotron Irradiation - long range ions



Timeline of Activities

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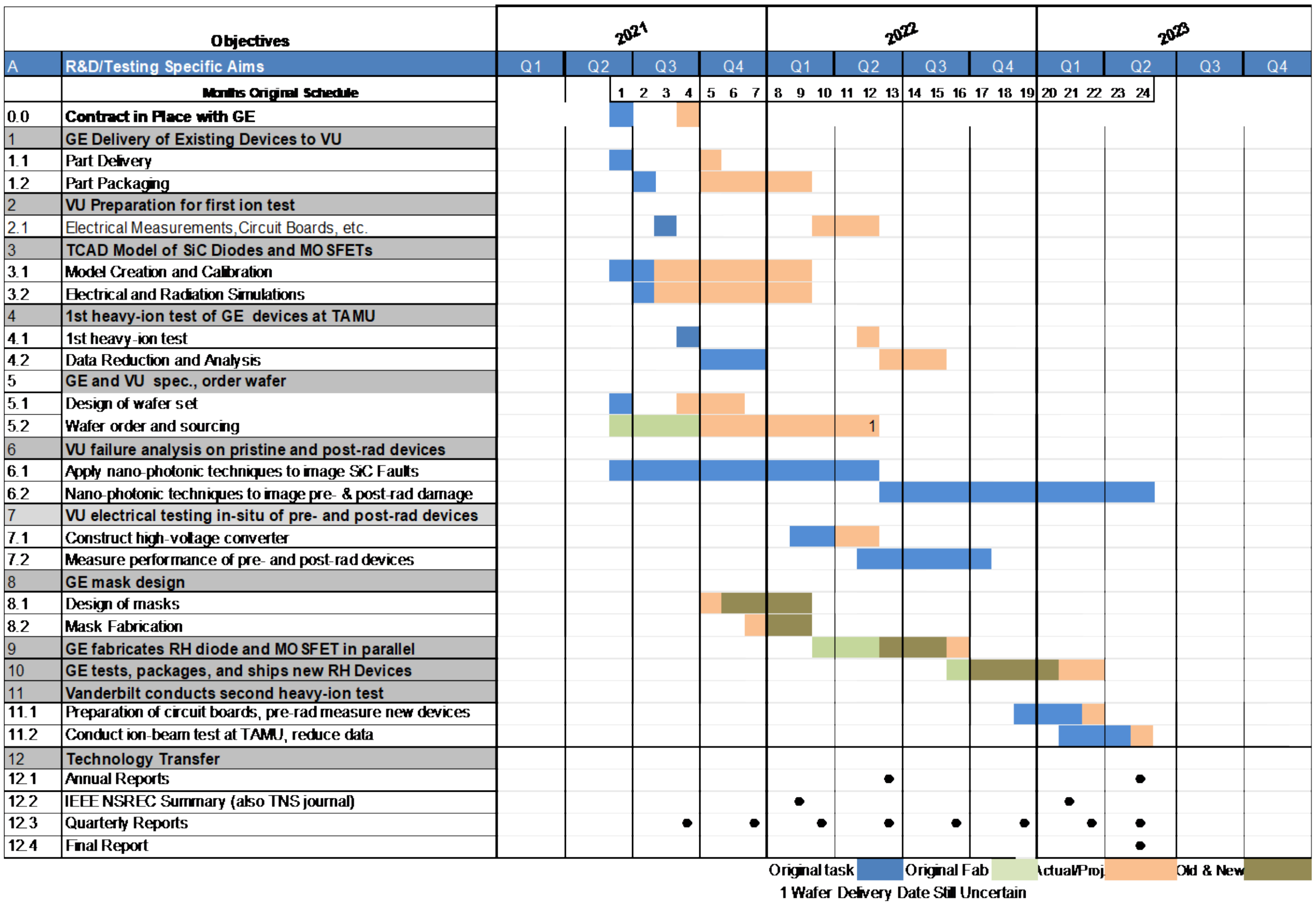

Leverage existing parts

- GE MOSFETS/Diodes
- VU 20 kV PiN diodes
- Commercial devices

New Design Activities MOSFETS/Diodes

Packaging, Parylene Coating, Electrical Testing

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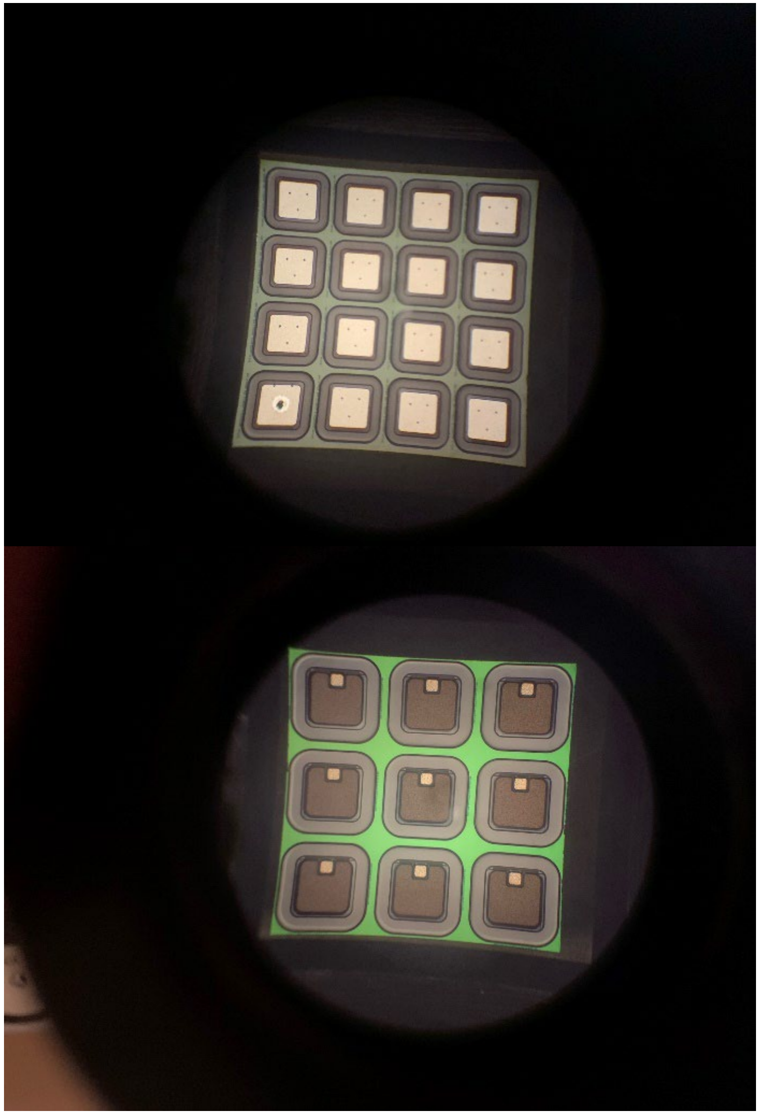

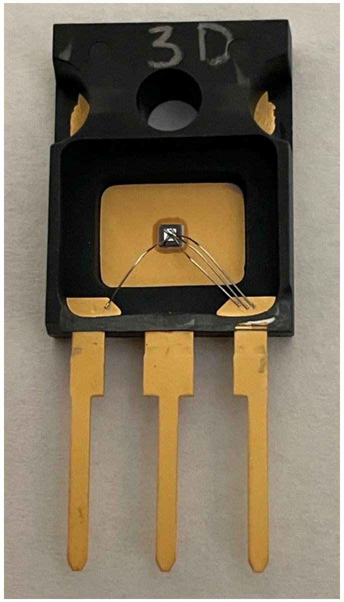

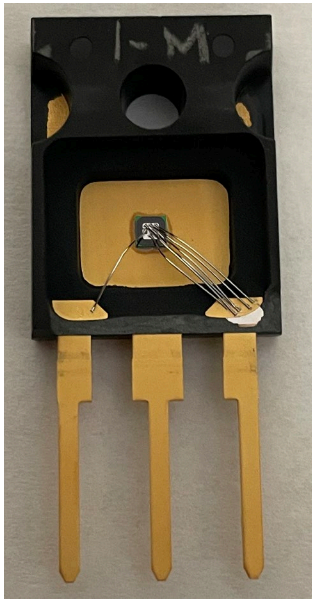

Performed for 124 Parts

Scheduled Heavy-ion Testing at TAMU (June 2022)

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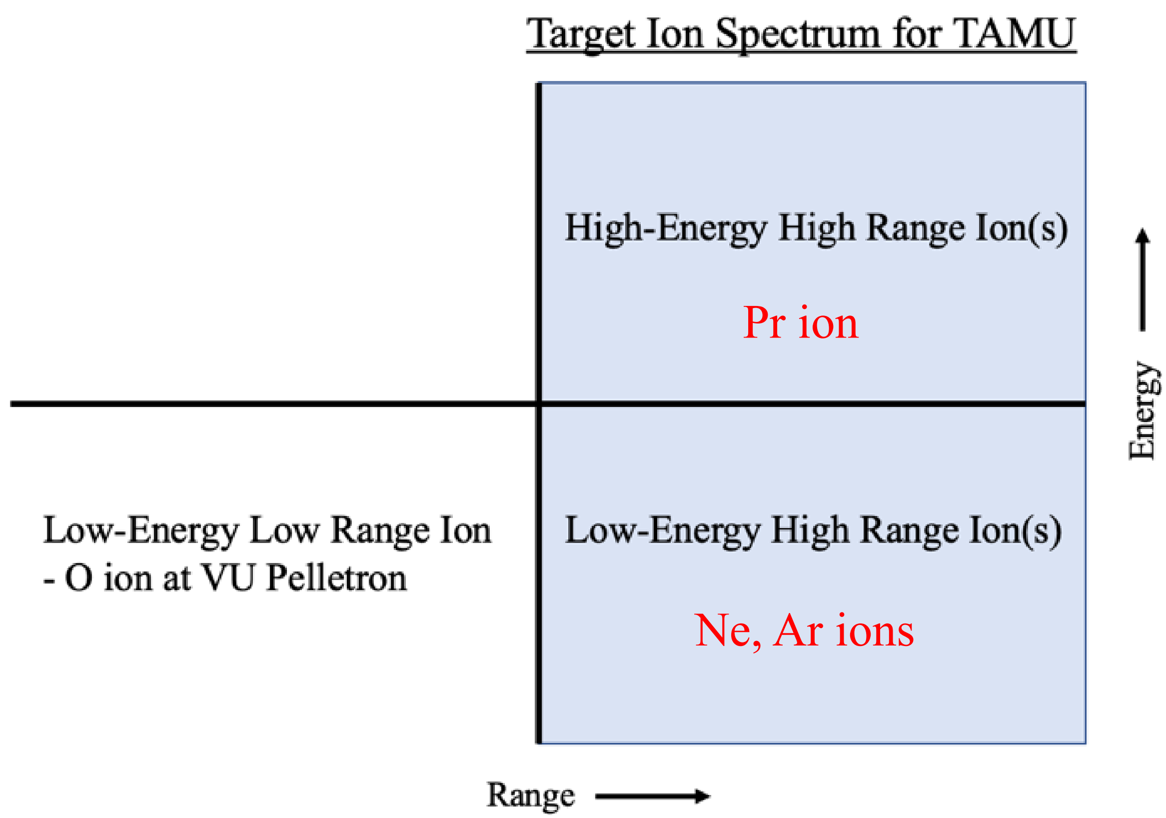

Testing Priorities:

1. **SEB threshold determination for 3300 V devices**
2. Correlation with previous results for 1200 V devices

Heavy-ion Testing at TAMU (June 2022)

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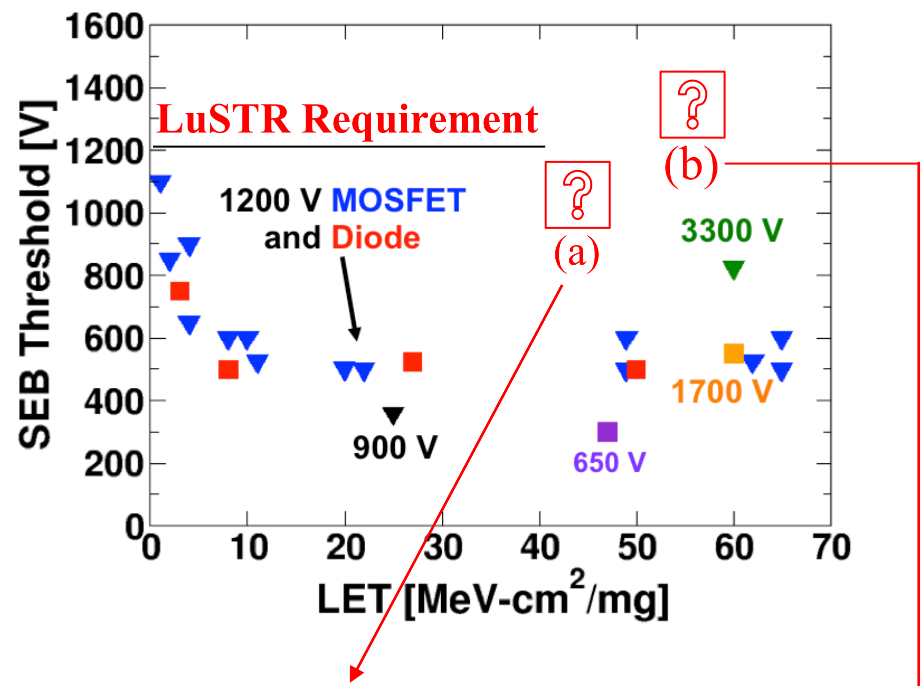
Devices to be tested:

- 1.2kV Planar MOSFET
- 3.3kV Planar Diode
- 3.3kV Planar MOSFET
- 3.3kV Charge-Balance (CB) Diode
- 3.3kV Charge-Balance (CB) MOSFET



(a) Predicted SEB Threshold for 3.3kV planar devices @LET ~ 43 MeV/(mg/cm^2)

(b) Predicted SEB Threshold for new target devices

Summary

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- Silicon carbide diodes and MOSFETs well-suited to NASA LuSTR high-voltage bus goals for lunar exploration, but SEB is reliability issue
- Testing and simulation indicate the SEB voltage boundary is related to the thickness of the epitaxial region-thicker epi corresponds to higher SEB voltage
- Simulations and test results show it is possible to create a new “target” device that meets the LuSTR goals for electrical breakdown, SEB voltage boundary, and on resistance
- General Electric has the wafers and will soon begin fabrication of target diodes and MOSFETs
- Heavy-ion testing for existing GE 3.3. kV diode and MOSFET variants is scheduled for late June

Definition of Acronyms

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“Epi” – Abbreviation of “Epitaxial”
GE – General Electric Corporation
JBS – Junction-Barrier Schottky Diode
LET – Linear Energy Transfer
LuSTR – Lunar Surface Technology Research
SEB – Single Event Burnout
SEE – Single Event Effects
SELC – Single Event Leakage Current
SiC – Silicon Carbide
TAMU – Texas A&M University
TCAD – Technology Computer-Aided Design Software
V_{BR} – Breakdown Voltage of a material
VU – Vanderbilt University
WBG – Wide-bandgap semiconductor material