Reliability Study of Enhancement Mode Gallium Nitride Field Effect Transistors

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Agenda

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- ❑ Basic Operating Principles of GaN Transistor Technology
- ❑ Stress Test
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  - Methodology
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  - Electrical Parametric Set-Up
  - Burn-In
  - Data Analysis
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Motivation

- Silicon transistor technology has reached its theoretical limits in terms of size, switching speed, power/current density and stand-off voltage.
- Wide Band Gap Transistors promise unprecedented power/current density, efficiency, high voltage and high-speed operation compared to Si technology.
- There are at least three degenerative effects that are a result of exposure to high electric fields. These include catastrophic voltage break down V_{GS}, increased leakage current I_{DS}, and $R_{DS(on)}$ shift.
- The purpose of this investigation is to gain insight into the effects of voltage and temperature on a few of these susceptible parameters (V_{GS}, I_{DS} and $R_{DS(on)}$) in terms of performance and reliability.

Basic Operating Principles

- GaN FET devices operate based on the piezo-electric properties of the GaN crystalline structure (Wurtzite).
- When the GaN material is subjected to mechanical stresses imposed by thin layer deposition of AlGaN to its surface, a high concentration of highly mobile elections is formed at the interface.
- Conduction of the device is facilitated by this 2-dimensional electron gas (2DEG).

Stressors

Stressor	Impact
Voltage: V_{DS} = 200Vdc, 160Vdc	Dielectric Failure, $R_{DS(on)}$ shift
Temperature: T_J	Observation
Hard Switching: Transient Power Dissipation	$R_{DS(on)}$ shift

The goal was to devise a test that can accelerate the life the eGaN FET and analyze its reliability with a focus on $R_{DS(on)}$ shift, V_{DS} stand-off voltage, and V_{GS} threshold drift.

Methodology

- Employ a resistive hard switching circuit and monitor leakage current, I_{DS} at elevated V_{DS} > 200Vdc.
- Incur device dynamic switching power dissipation driven by dV/dt and high drain current.
- Monitor $R_{DS(on)}$ shift and apply stress to the gate circuit V_{GS}.

Device Selection

Enhancement mode Gallium Nitride (eGaN) power transistor

Ratings:

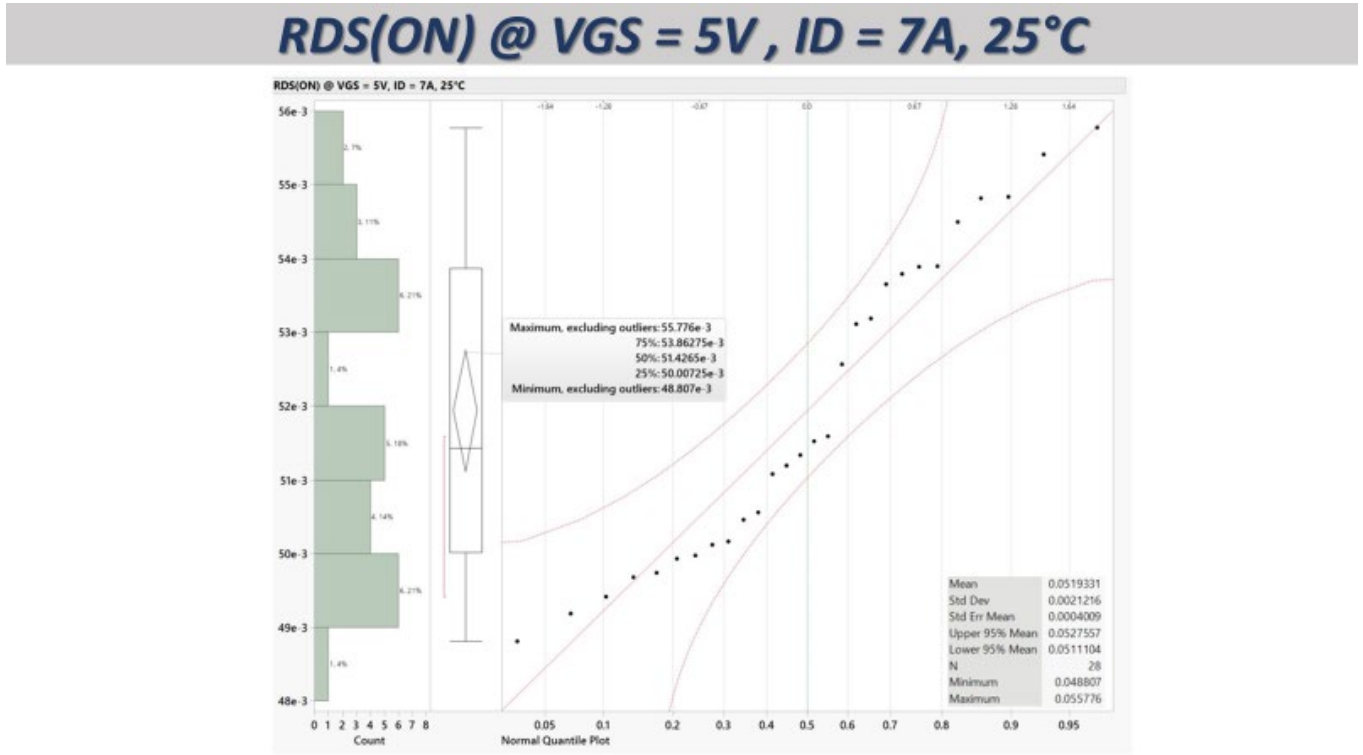
- V_{DS} = 200V
- $R_{DS(on)}$ = 50mΩ
- I_D = 8.5A, Pulsed I_D= 42A

Package:

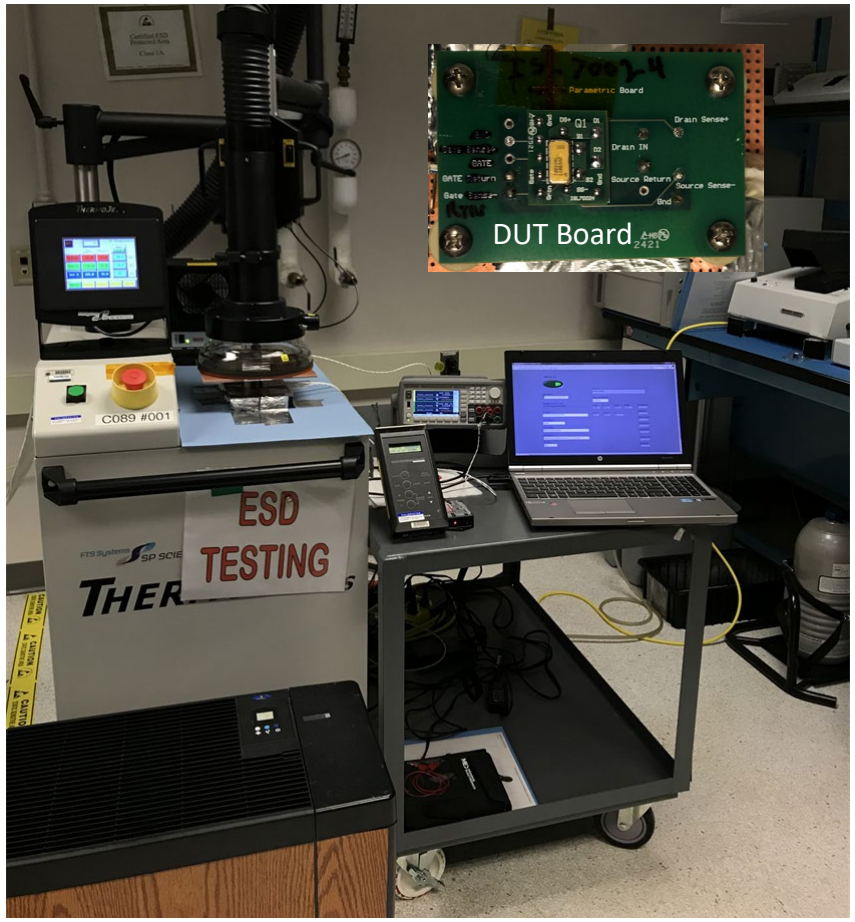
- Radiation hardened, hermetically sealed
- 4 lead ceramic surface mount device
- Incorporating a 2.77mm x 0.95mm die scale low-loss, high-speed, high-power density eGaN FET

Electrical Parametric Test Set-Up

Electrical measurements were performed at T_A = 25°C, -55°C and 125°C, in accordance with the data sheet



Initial Rds(on) Measurements

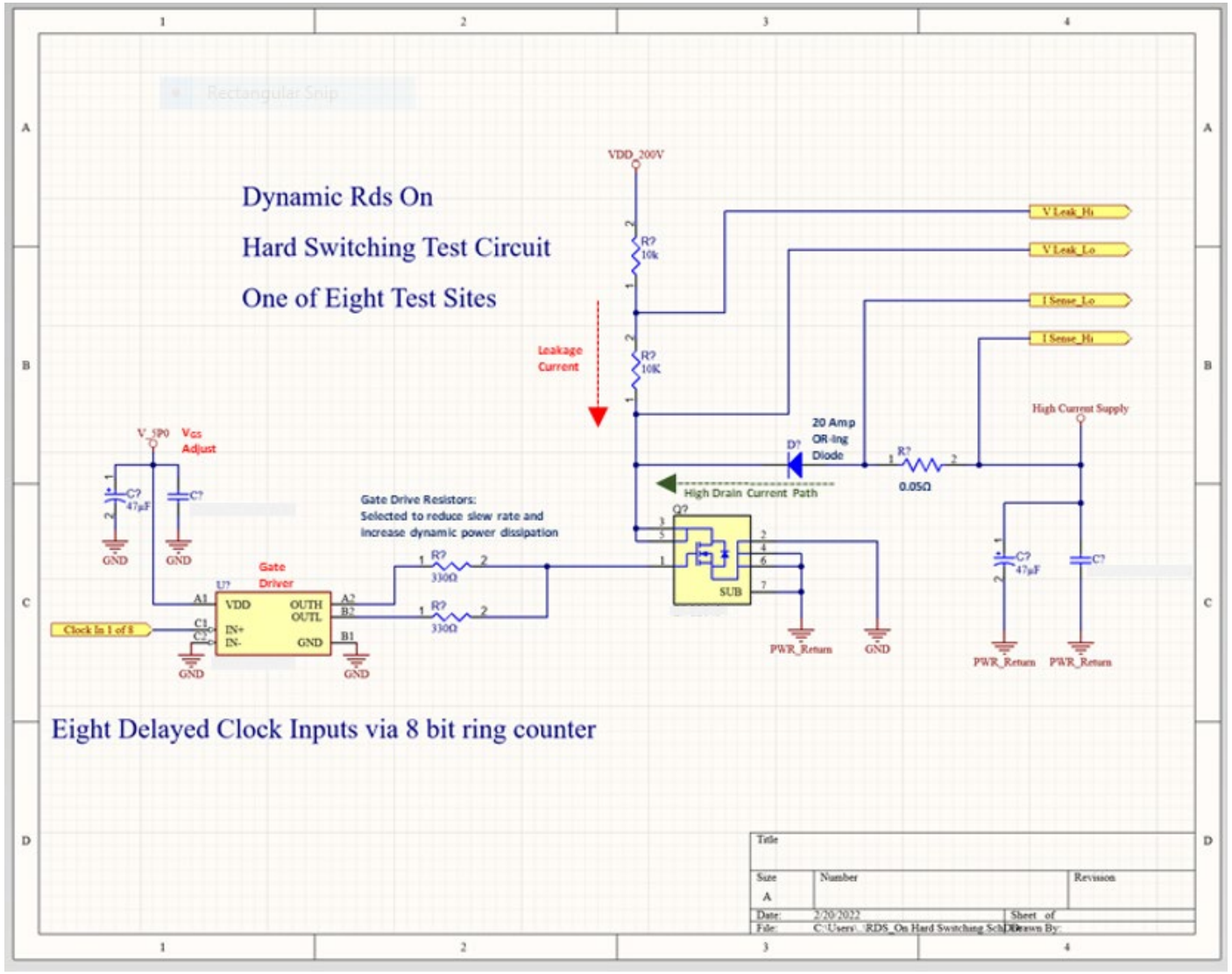


Electrical Test Set-Up

Burn-In Hard Switching Test [5]

- Consisted of two boards each populated with 6 eGaN devices.
- Transistors commutated in a sequential fashion.
- A single transistor per board is turned on at a given instance in time.
- Board 1 was biased with a 200Vdc HV supply while Board 2 is biased with a 160Vdc supply.
- Voltages were selected to exasperate degenerative effects such as $R_{DS(on)}$ drift.
- Burn-in (BI) data acquisition consisted of:
  - Drain current measurements using a data logger
  - Composite drain current measurements
  - Static $R_{DS(on)}$ measurements
  - Dynamic $R_{DS(on)}$ measurements
- Device characterization performed while mounted in the burn-in fixture prior to BI.

Burn-In Hard Switching Test – Schematic



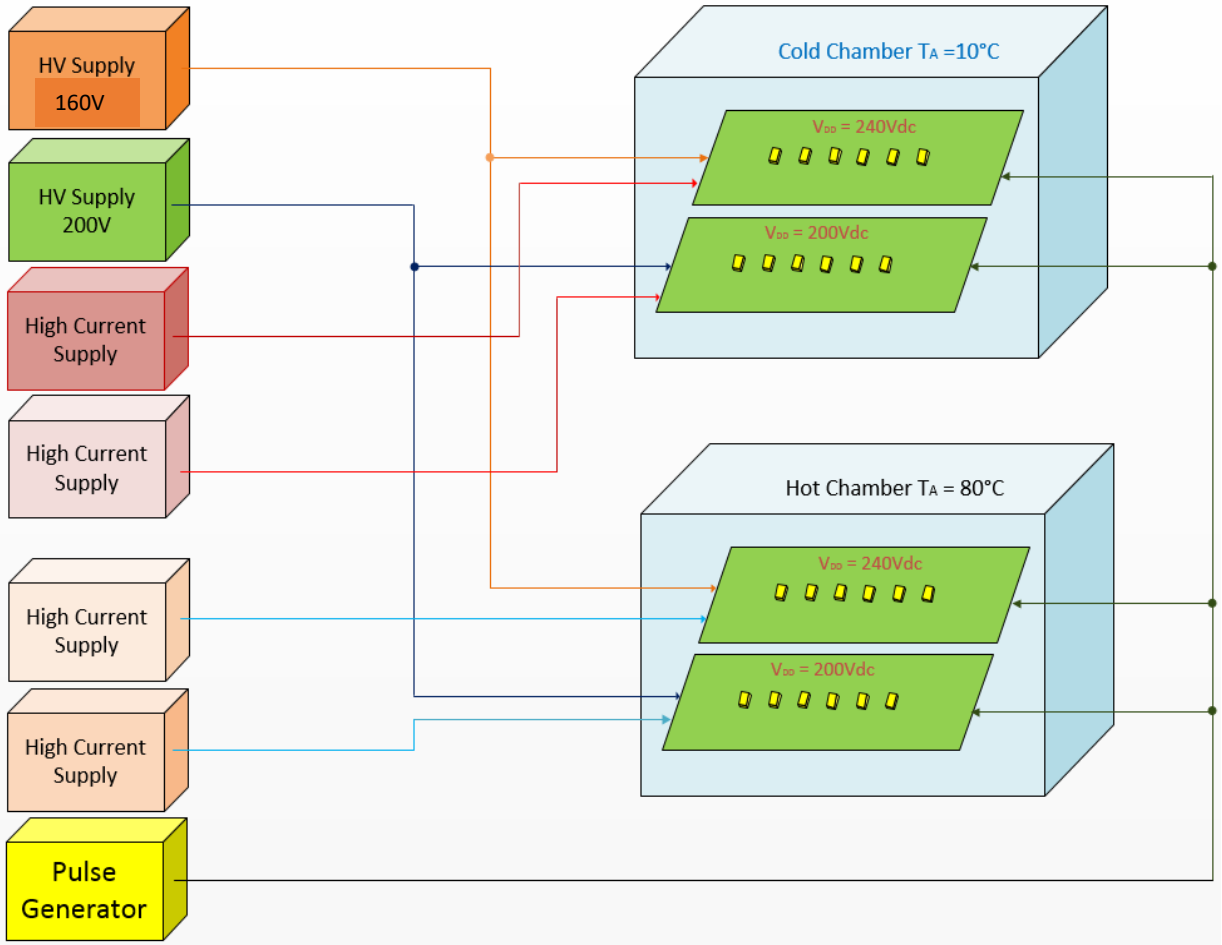
Initial eGaN Burn-In Block Diagram

Stress specimens consisted of two groups of 12 devices, with simultaneous stress on 4 sets of devices (2 from each group). Note, 200Vdc and 160Vds are the absolute and recommended maximum ratings of the device, respectively.

Group One:
- Stressed at T_A = 10°C
- 6 devices biased at V_{DS} = 200Vdc
- 6 devices biased at V_{DS} = 160Vdc*

Group Two:
- Stressed at T_A = 80°C
- 6 devices biased at V_{DS} = 200Vdc
- 6 devices biased at V_{DS} = 160Vdc*

* Stress voltage for 2 sets of devices was lowered from 240Vdc to 160Vdc after initial burn-in tests

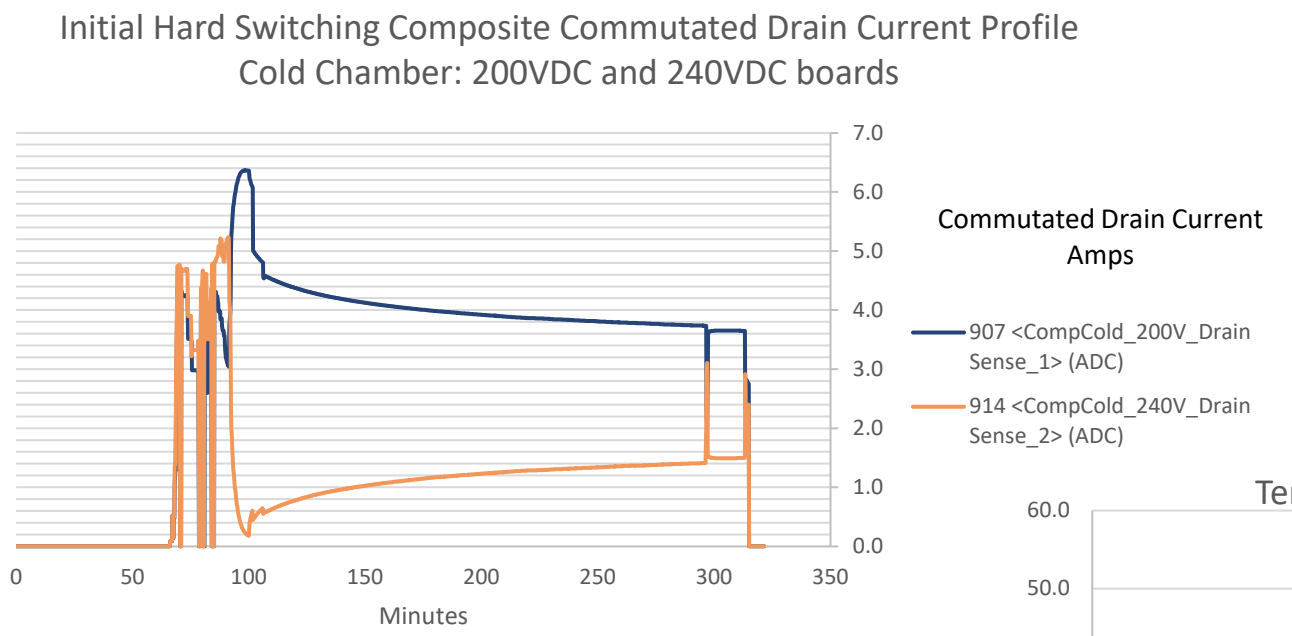


Initial Burn-In Bias Configuration

During the initial start-up, the 160V devices were biased at 240V

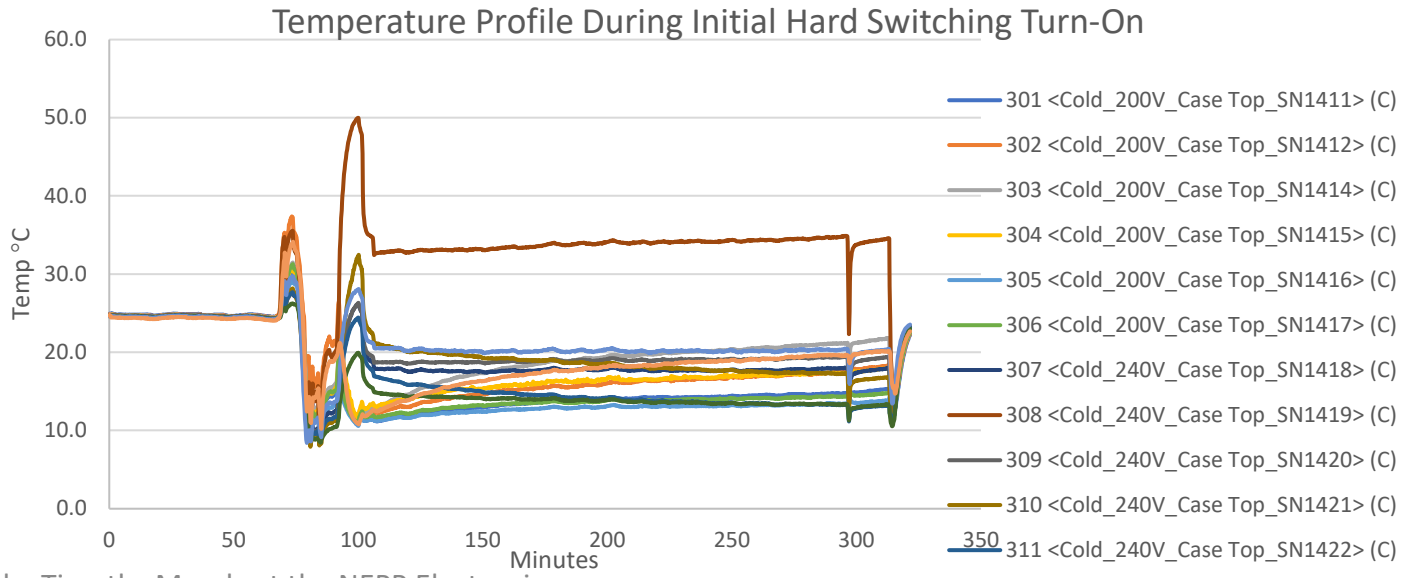
- The intent was to accelerate the failure mechanisms by introducing V_{DS} stress 20% above the absolute maximum rating of 200V.
- Two boards in each chamber were wired for current sharing.
- At 240V the devices were operating hotter than expected.
- The bias was reduced to 200V.
- The test was terminated after a short period.
- Subsequent testing was performed at 160V.

Initial Turn On – Hard Switch COLD Chamber

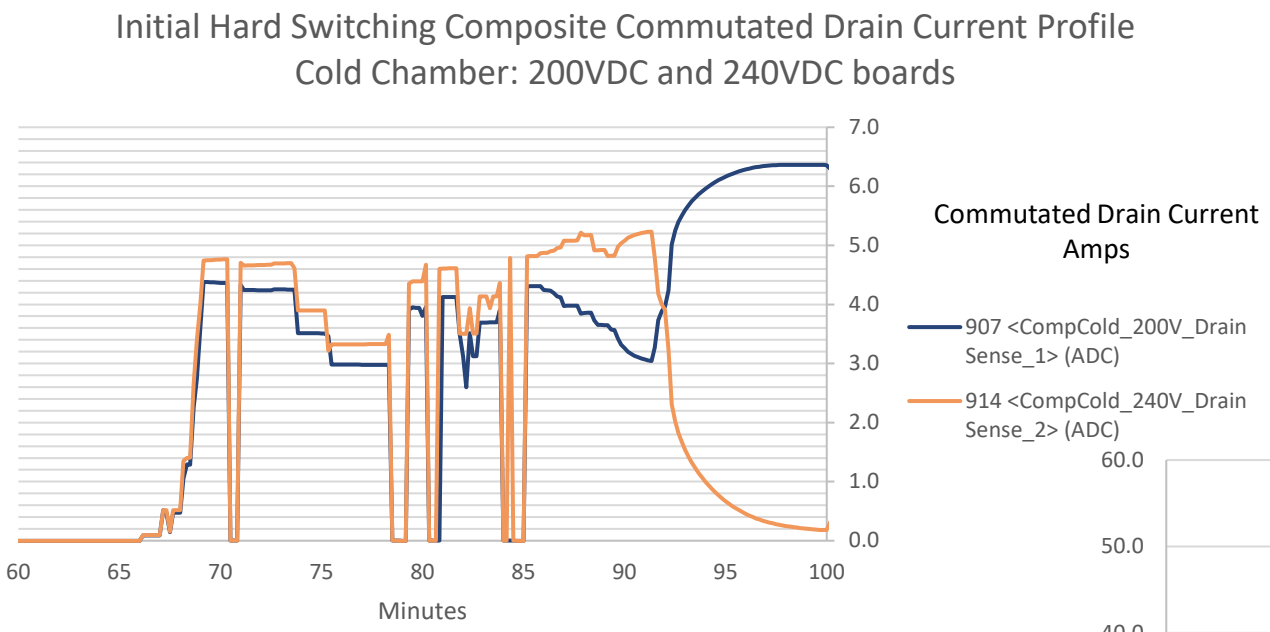


The plot above shows the composite commutated current sharing profile for the Cold 200V and 240V boards during the initial start-up. The chamber is transitioning from 25°C to 10°C as the power supply was adjusted to obtain a peak commutated current of approximately 5 Amp.

The plot below show the case temperature profile of each device measured at the top for the package and single temperature point measure at a central DUT/ board interface.

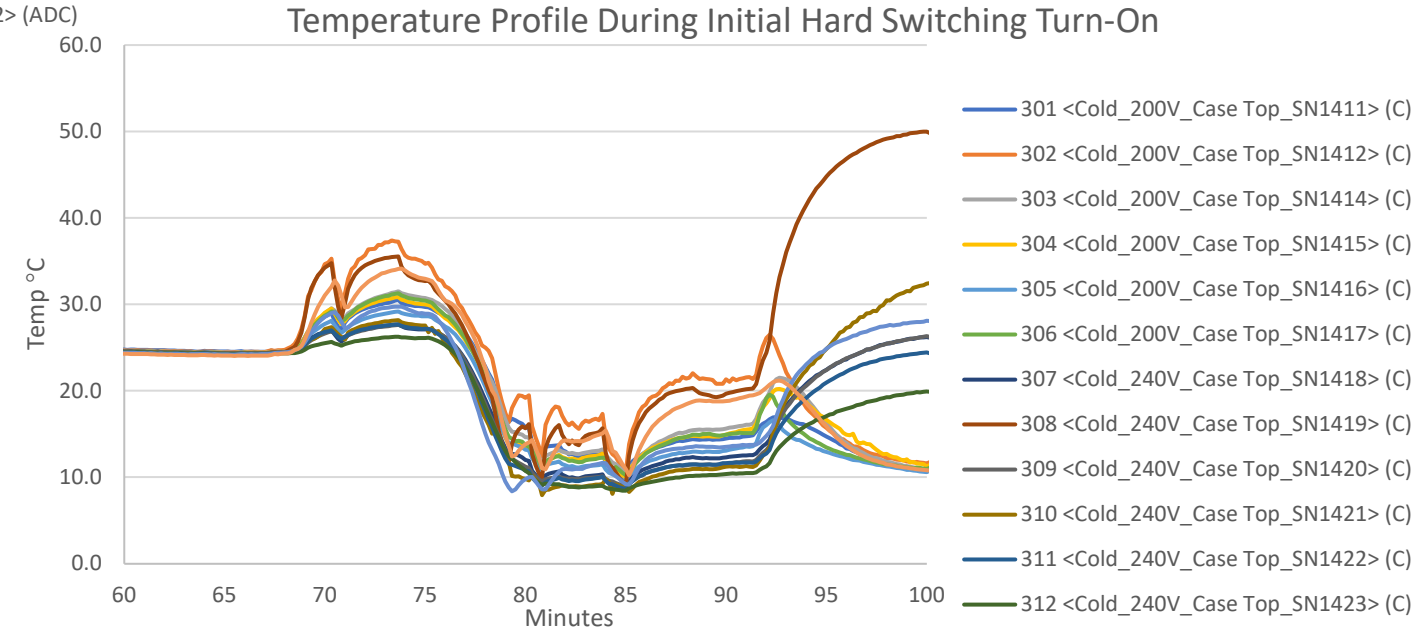


Initial Turn On – Hard Switch COLD Chamber

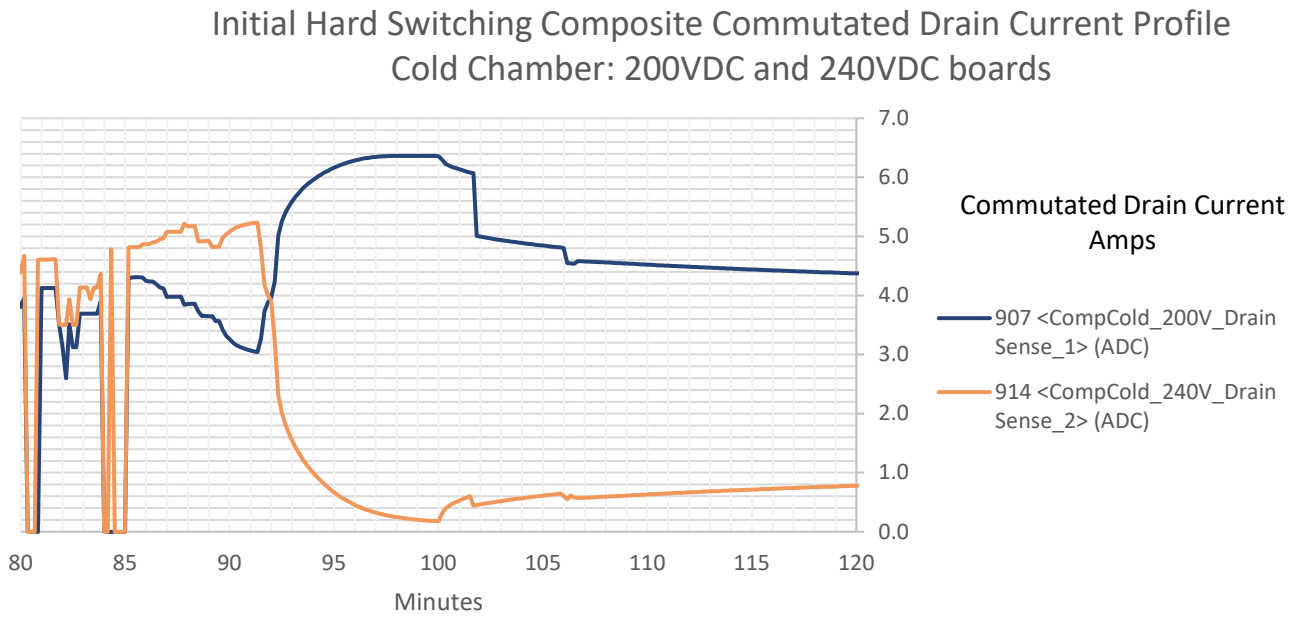


At the 85-minute mark, the current was set to the appropriate level: 4.8A for the 240V board and 4.3A for the 200V Board. At this point the case temperature of all 12 devices was at 10°C.

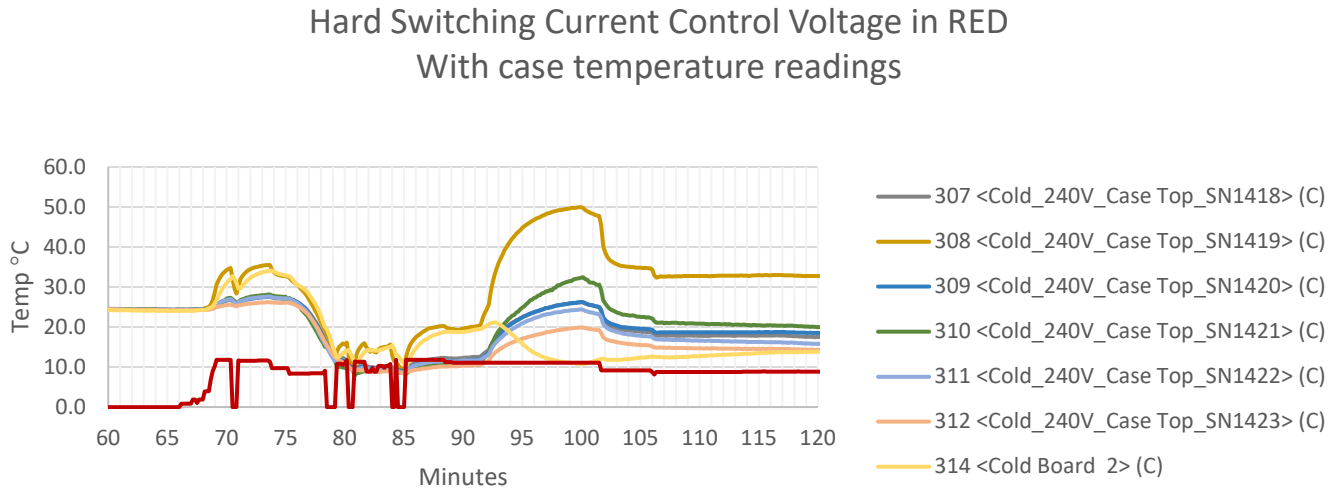
The plot below shows the case temperature of the 240V devices to be increasing with one device SN: 1419 increasing more rapidly than the others



Initial Turn On – Hard Switch COLD Chamber



The plot below shows case temperature of the 240V devices rising until the commutation current was scaled back to 3 Amps and the 240V adjusted to 200V at the 100-minute mark.



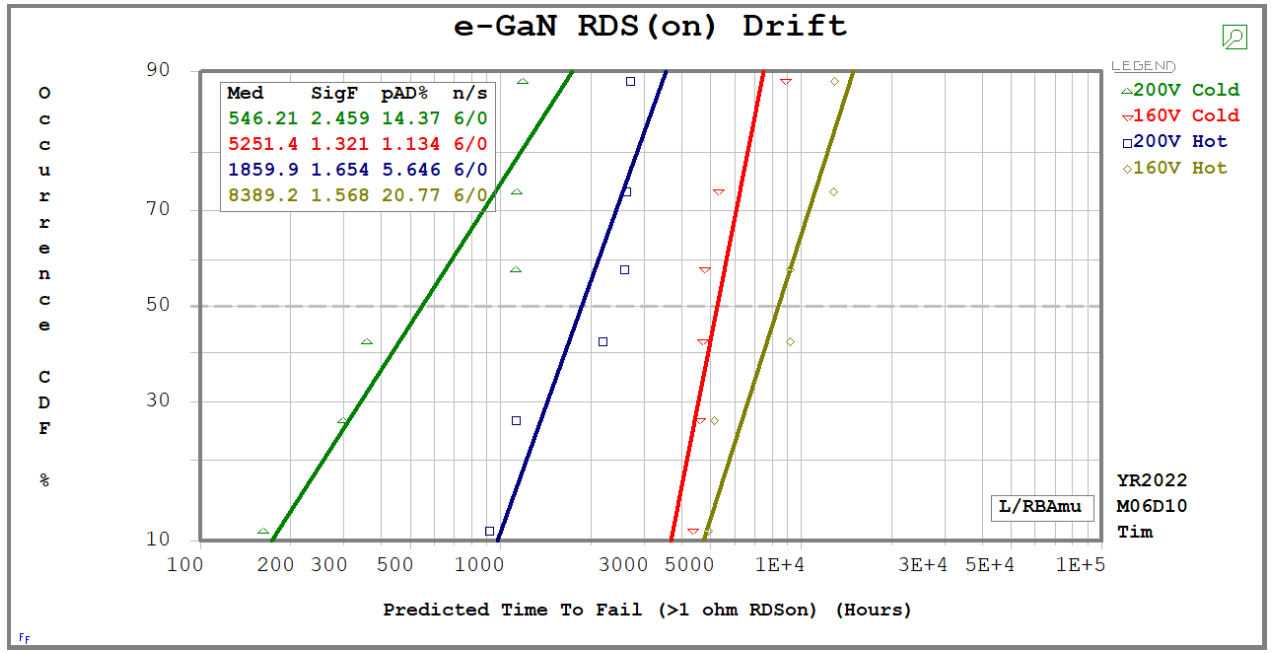
After the 85-minute mark the current sharing between boards 1 and 2 starts to diverge. The 240V board current draw as well as case temperature increases. Then after 90 minutes the current sharing transitions from the 240V devices to the 200V devices. This phenomena is called current collapse which results when the $R_{DS(on)}$ increases significantly with time.

Dynamic $R_{DS(on)}$ Drift

Drain current measurements displayed signs that the applied stress was affecting the dynamic $R_{DS(on)}$ performance of the devices.

- Oscilloscope displays indicated that various device capacity to sink current was diminishing over time.
- The effect was most pronounced for the 200V specimens.
- The devices in the hot chamber were less affected than those in the cold chamber.
- Required an Active Clamping Circuit [3].

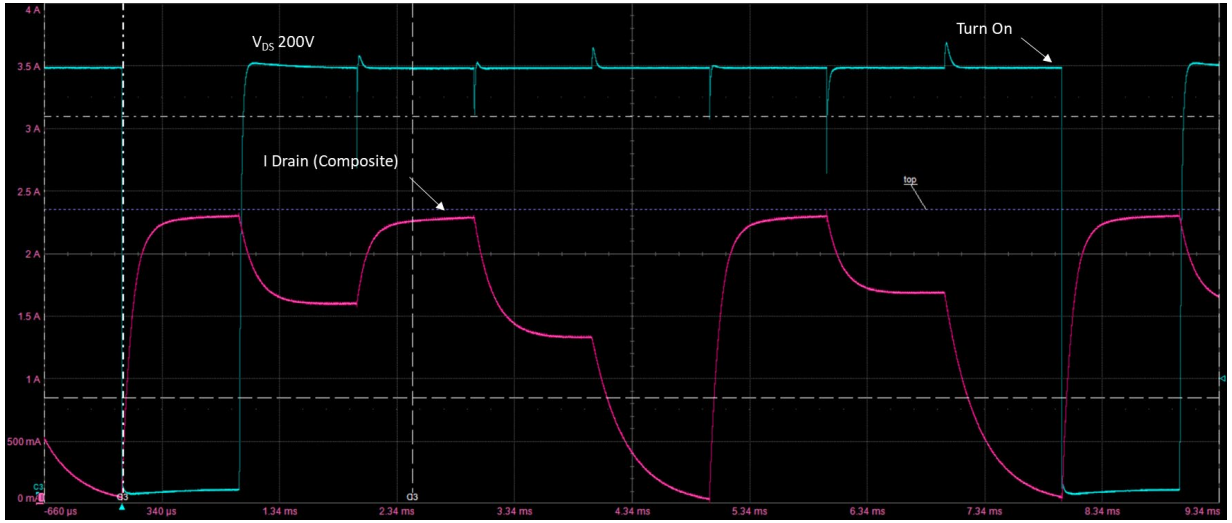
Rds(on) Drift After 337 Hours of Stress



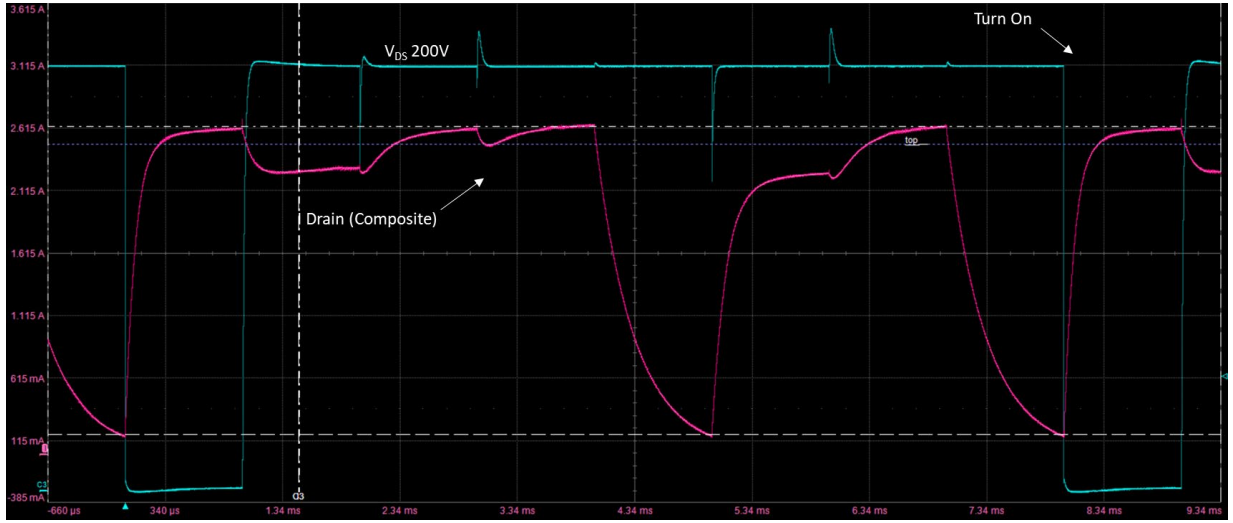
Hard Switching 200V, Degradation after 337 Hours

Scope display showing substantial commutated current variations for all six devices on boards 1 and 3:

Cold Chamber

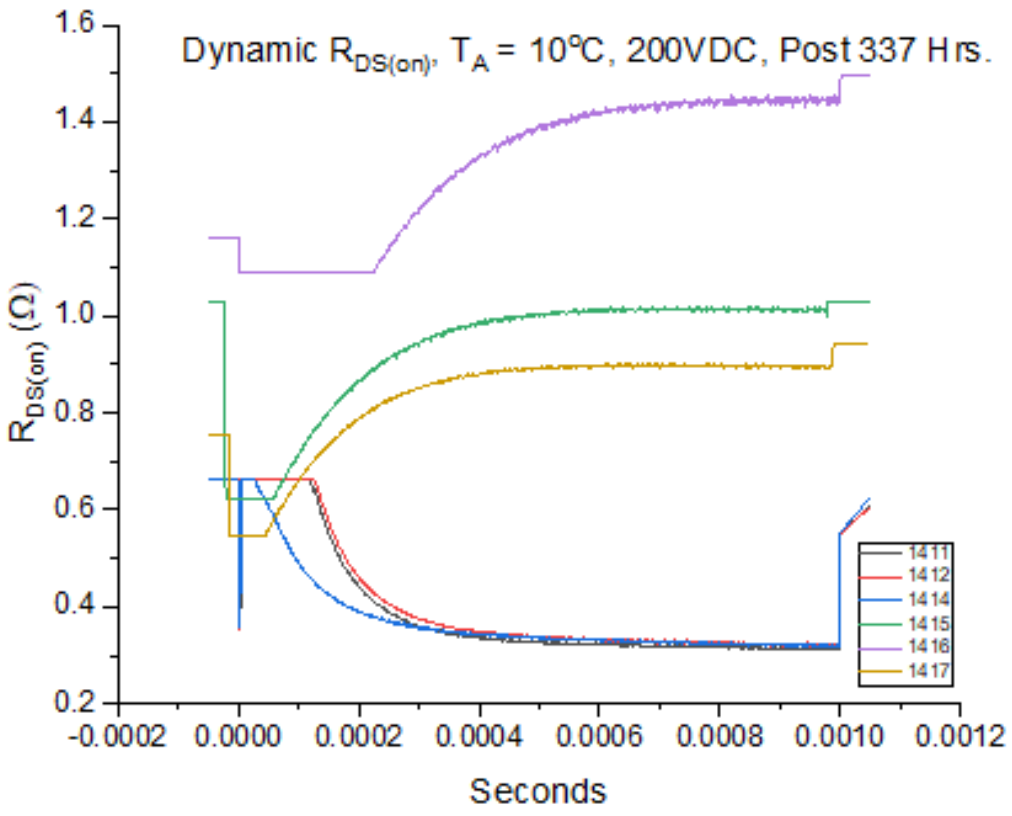


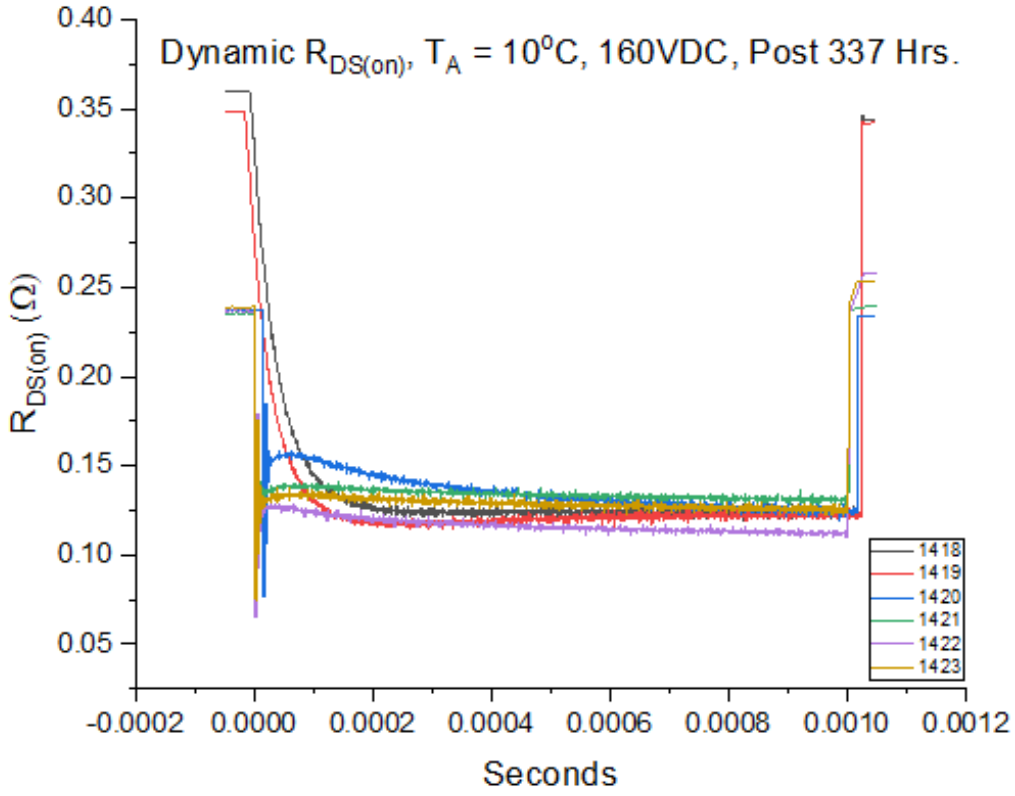
Hot Chamber



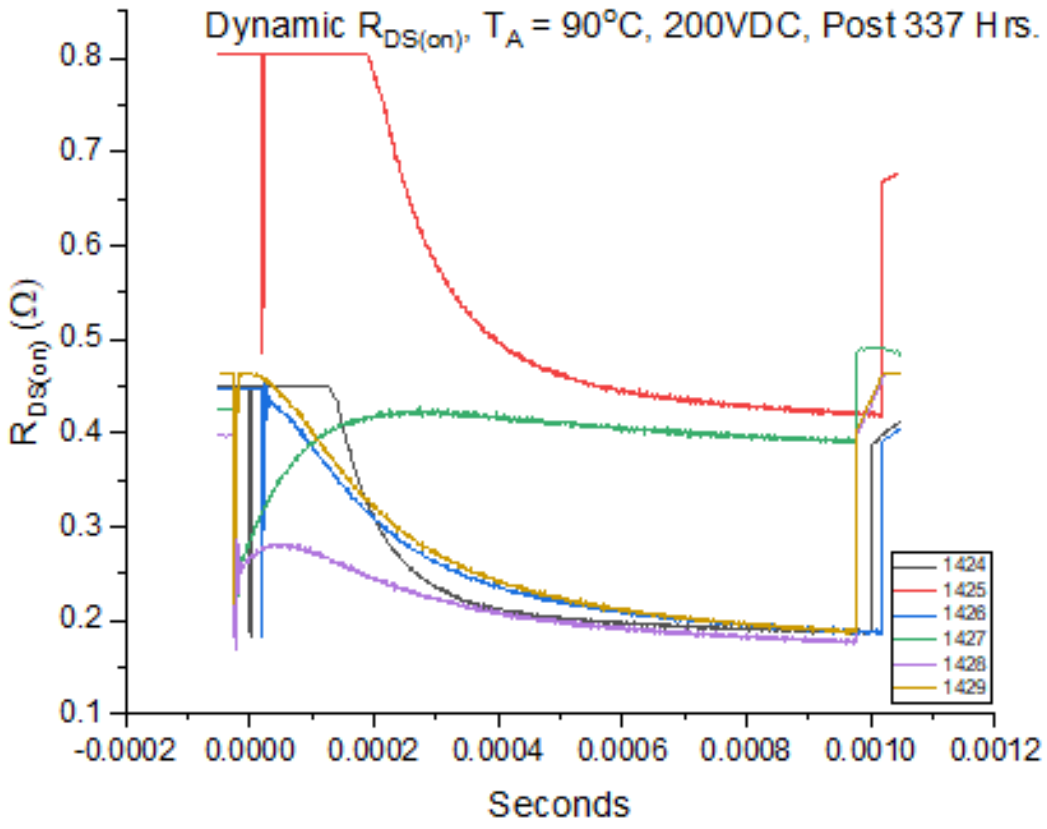
Note difference in peak to peak between the cold chamber and the hot chamber, indicating the sensitivity of Rds(on) drift to temperature.

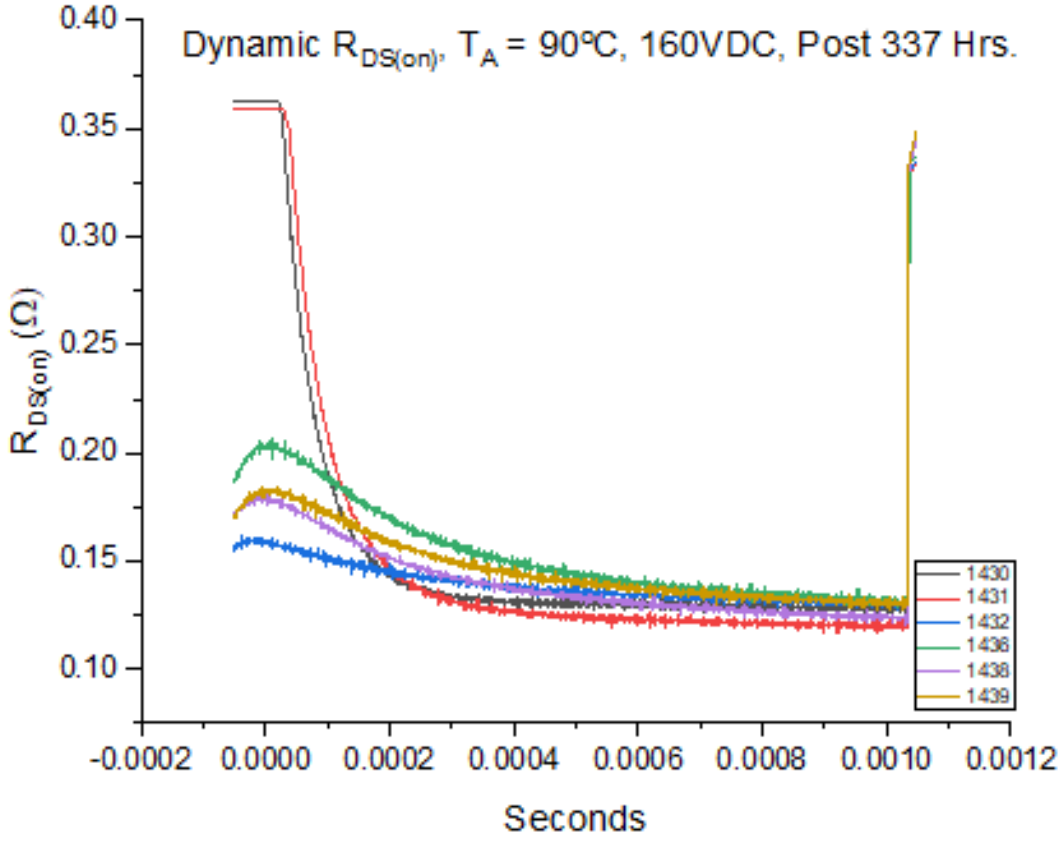
Dynamic $R_{DS(on)}$ Post 337 Hours



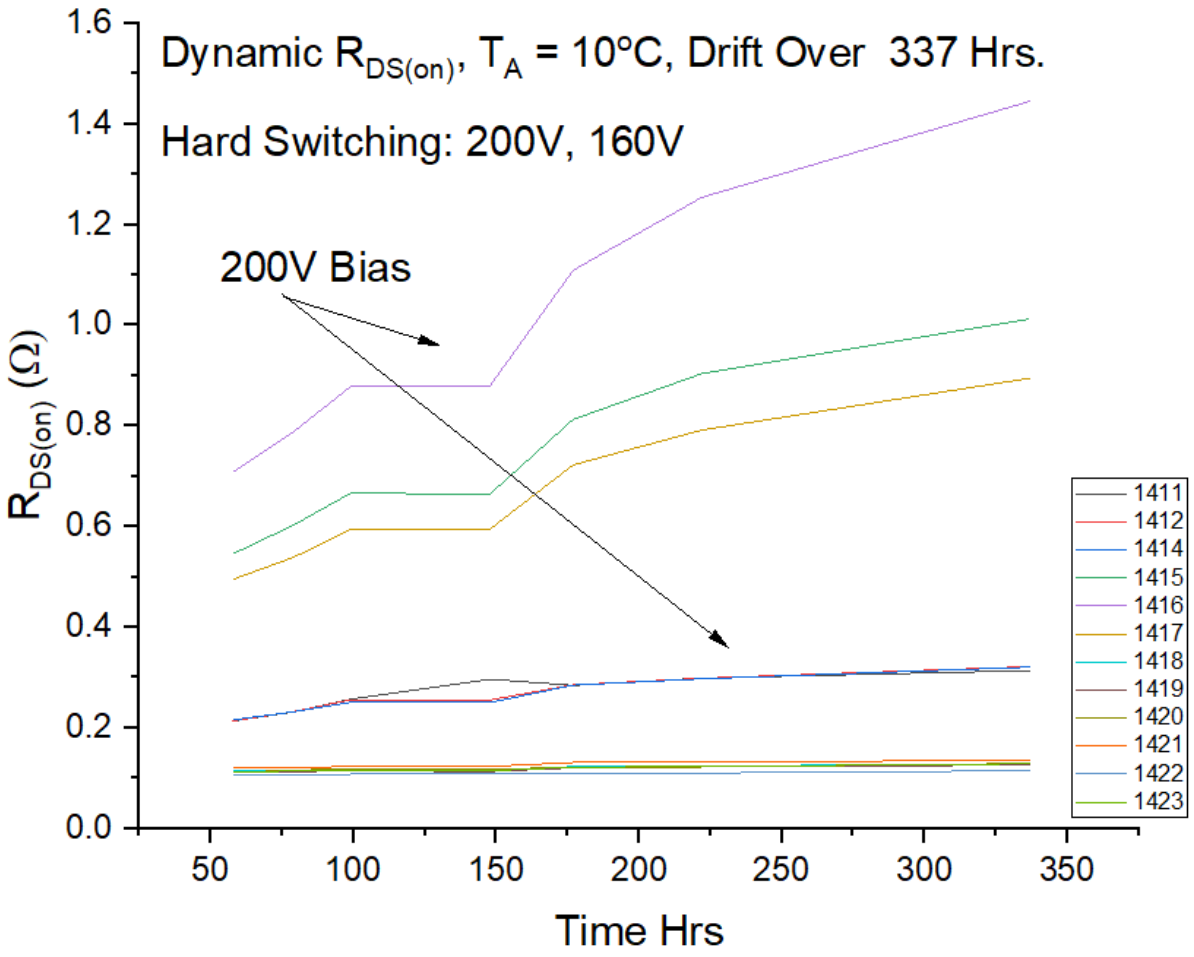


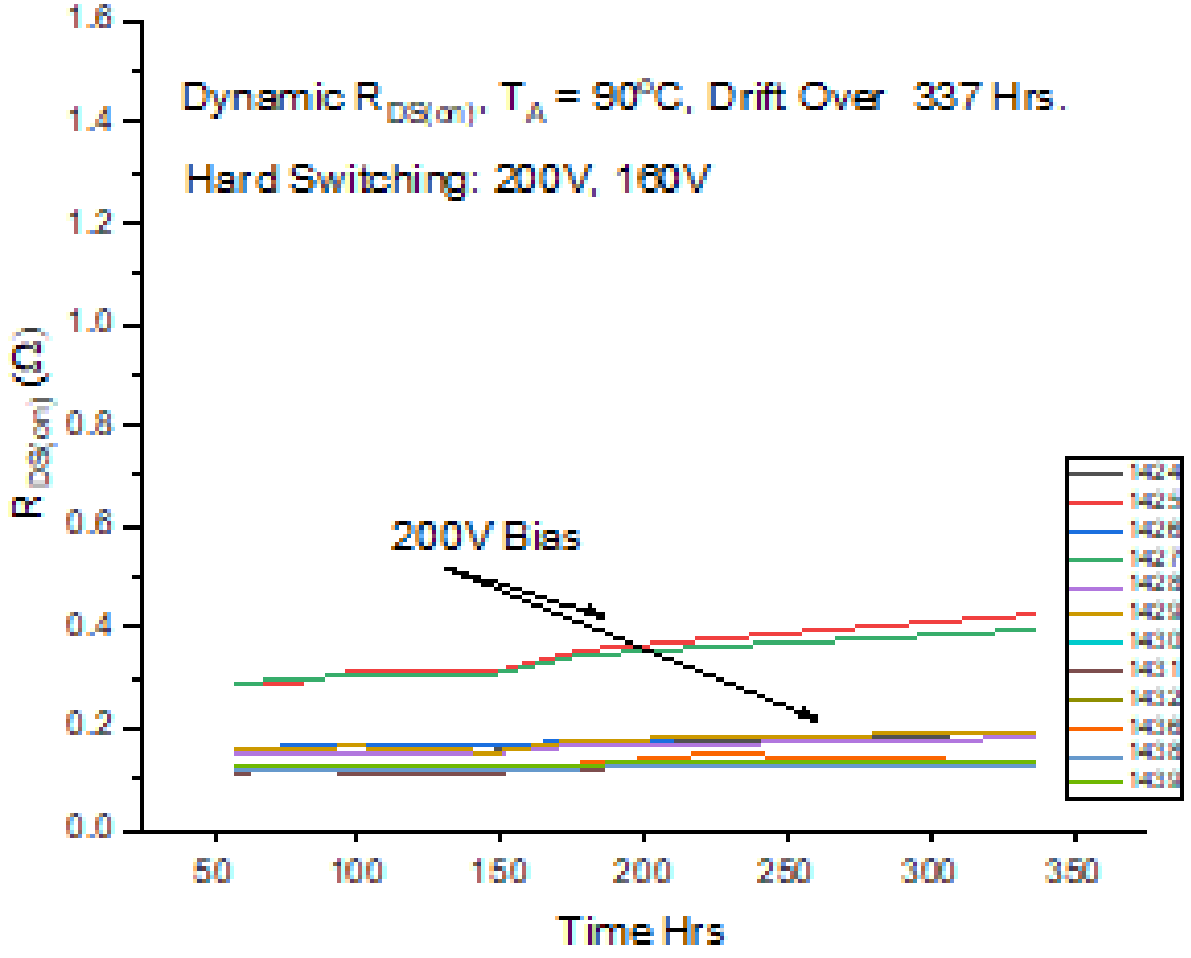
Dynamic $R_{DS(on)}$ Post 337 Hours





Dynamic $R_{DS(on)}$ Drift Over 337 Hours of Stress





Conclusions

- These devices did not display any worrisome signs of degradation in terms of leakage current, dielectric breakdown or catastrophic failure during the 337 hours of stress.

- At 200V (absolute maximum rating for V_{DS}) the dynamic $R_{DS(on)}$ increased dramatically, the rate of drift was less at 90°C compared to 10°C.

Additional Considerations

- To realize the performance gains from using eGaN devices, appropriate design techniques must be employed. For example, the gate drive requirements of an eGaN device is not compatible with a MOS FET. The gate voltage must be limited to +6V,-4V(GaN FET) compared to +/- 20V (MOS FET), including transients.

- Since eGaN FETs are piezo electric devices, their sensitivity to vibration and thermal expansion should be considered.

References

[1] Alejandro Pozo Ph.D., Shengke Zhang Ph.D., Gordon Stecklein Ph.D., Ricardo Garcia, John Glaser Ph.D., Zhikai Tang Ph.D., and Robert Strittmatter Ph.D., “GaN Reliability and Lifetime Projections: Phase 14,” EPC Corp., El Segundo, CA, USA, Reliability Report. [Online]. Available: Reliability Report Phase 14 (epc-co.com)

[2]Alejandro Pozo Ph.D., Shengke Zhang Ph.D., Gordon Stecklein Ph.D., Ricardo Garcia, John Glaser Ph.D., Zhikai Tang Ph.D., and Robert Strittmatter Ph.D., “EPC eGaN® Device Reliability Testing: Phase 12” EPC Corp., El Segundo, CA, USA, Reliability Report. [Online]. Available: Reliability Report Phase 12 (epc-co.com)

[3] Edward A. Jones, Alejandro Pozo, “Hard-Switching Dynamic Rdson Characterization of a GaN FET with an Active GaN-Based Clamping Circuit”, 2019 IEEE Applied Power Electronics Conference and Exposition (APEC).

[4] F. Yang, C. Xu, E. Ugur, S. Pu, B. Akin, “Design of a fast dynamic on resistance measurement circuit for GaN power HEMTs, in Proc. IEE

[5] Dynamic On-Resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices, Version 1.0, JEDEC Standard JEP173, 2019.

Team Acknowledgements

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Tiu, Christopher

Weachock, Ronald James

Backup Slides

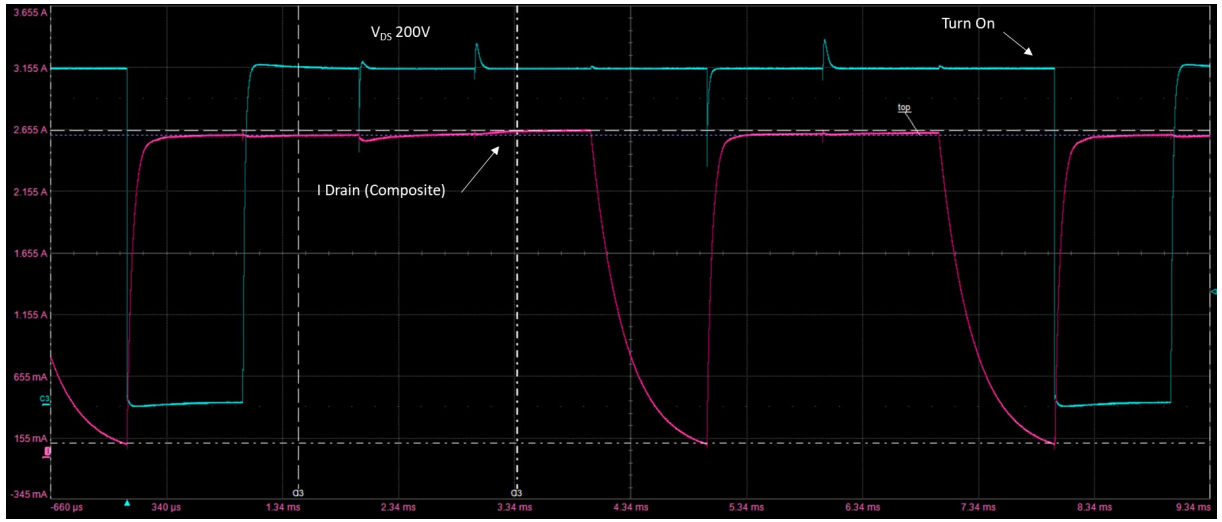
Stressor Schedule

Stressor	Temp (°C)	Duration (Hrs)	Total (Hrs)
Leakage	25	0.63	0.63
Hard Switching	10,25	3.68	4.31
Leakage	25	0.49	4.80
Leakage	25	0.44	5.24
Leakage	25	4.05	9.30
Leakage	25	1.92	11.22
Hard Switching	10,25	6.18	17.40
Hard Switching	10,90	15.81	33.21
Leakage	25	1.93	35.14
Hard Switching	10,90	16.59	51.73
Leakage	10,90	1.79	53.52
Hard Switching	10,90	26.84	80.36
Leakage	10,90	0.88	81.24
Hard Switching	10,90	18.56	99.81
Leakage	10,90	0.47	100.28
Hard Switching	10,90	77.54	177.82
Leakage	10,90	0.31	178.13
Hard Switching	10,90	44.48	222.60
Hard Switching	10,90	114.60	337.20

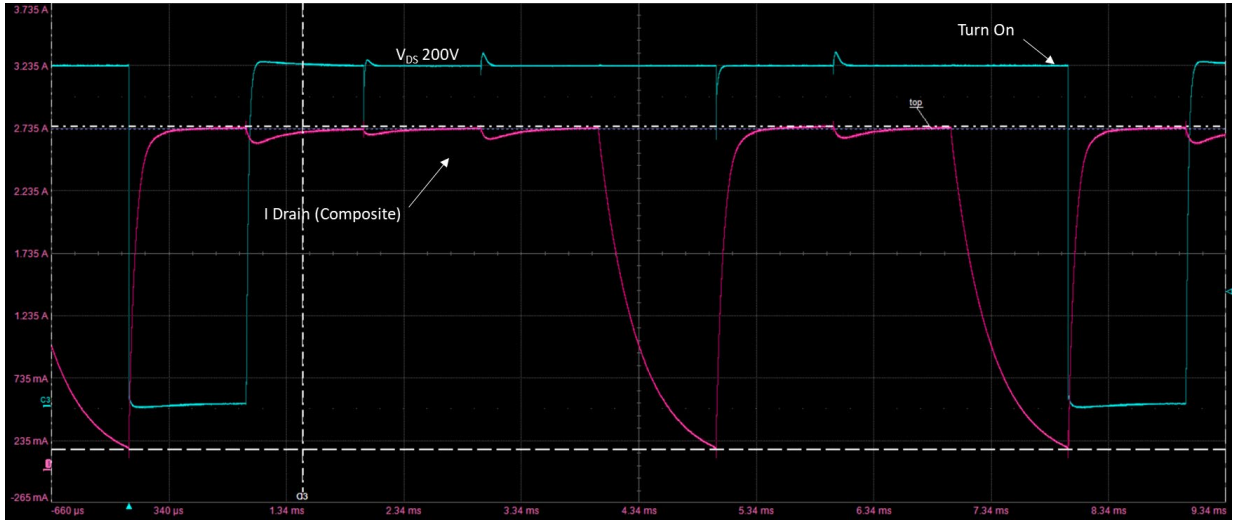
Hard Switching 160V, Degradation after 337 Hours

Scope display showing minimal commutated current variations for all six devices on board 2 and 4:

Cold Chamber



Hot Chamber



Modification of Hard Switching Test

- The Hard Switching Test was allowed to run on the cold samples only (T_A =10°C) at 200Vdc on both cards, 125us pulses at 3Amp with a pulse repetition rate of 8KHz.
- The samples in the hot chamber were operated with the high current supply disabled at 200V and T_A =25°C.
- The test ran for 227 minutes and was shut down.
- The current sharing scheme was incapable of limiting the current in the alternate board during the current collapse events.
- The voltage level of the 240Vdc group was lowered to 160Vdc.
- The burn-in circuit was modified so that each board could have its own independent current source.