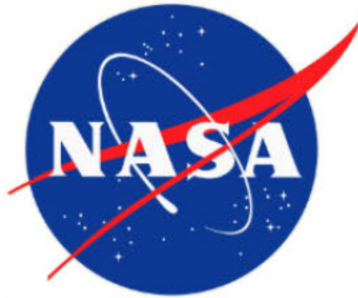

2.5/3D-Level Packaging Technology Materials, Assembly Process, and Reliability Challenges for Space Applications

Eric Jong-ook Suh, Ph.D.

Joseph Riendeau, Ph.D.

Jet Propulsion Laboratory, California Institute of Technology

NASA Electronic Parts and Packaging Program (NEPP)

2022 Annual NEPP Electronic Technology Workshop (ETW)

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2.5/3D / Heterogenous Integration Packaging

- Integrate multiple dies at the package level
  - Integrate pieces of a large die and enhance die yield
  - Heterogenous integration
    - Disparate semiconductor technologies.
  - Integrate IP blocks or functions difficult to build on the same chip
  - Avoid redesigning entire chip for advanced node
  - Quicker development for SoC
- Interconnection
  - Lateral : Line & IO density greater than organic substrate.
  - Vertical : TSV

2.5D

3D

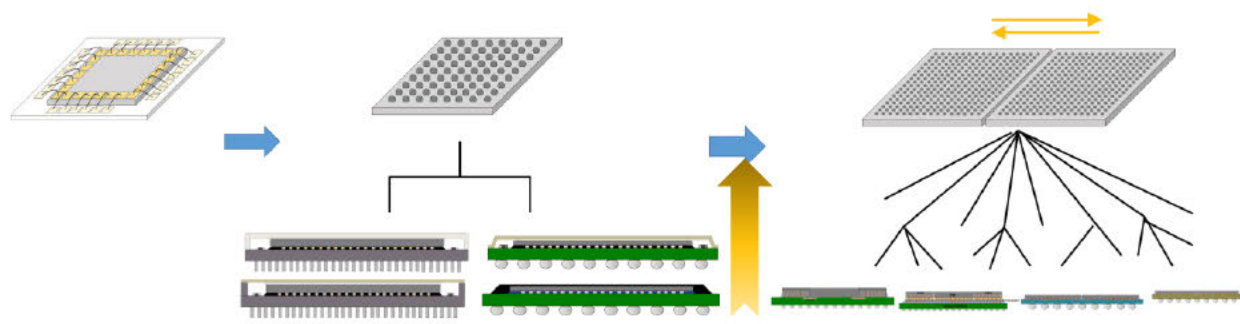
EMIB

HBM
Logic
HBM
Si Interposer
Organic Substrate

Si Bridge

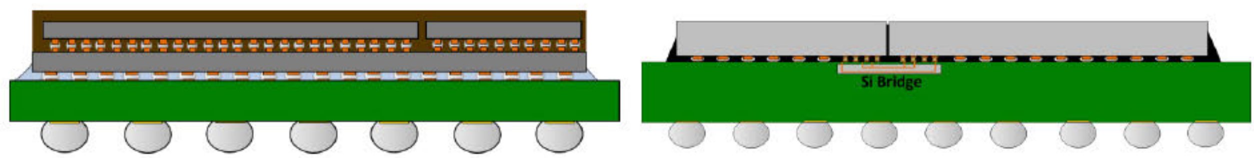
HBM
GPU
Si Bridge

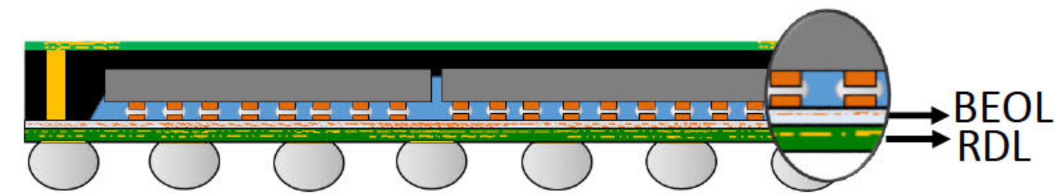
No Industry Common Packaging Architectures



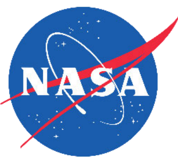
More technology building blocks (manufacturing technologies and materials)
- *Packaging technology (CSP, WLP, coreless substrate, embedded component, etc)*
- *Evolution in other technologies that can be leveraged (flat panel display, MEMS,etc)*

Name	Stands for	Description	Company
CoWoS	Chip-on-Wafer-on-Substrate	Si Interposer	TSMC
EMIB	Embedded Multi-die Interconnect Bridge	Si Bridge	Intel
FOCoS	Fan-Out Chip on Substrate	Fan-out	ASE
FO-EB	Fan-Out Embedded Bridge	Fan-out	SPIL
FO-MCM	Fan-Out Multi-Chip Module	Fan-out	SPIL
Foveros		Heterogenous 3D dies connected with EMIB	Intel
Glass Substrate		Line & via built on glass core	Absolics (SKC)
InFO	InFO (Integrated Fan-Out)	Fan-out	TMSC
RDL Interposer	Redistribution Layer Interposer	Bare RDL as interposer	Samsung
SLIM	Silicon-Less Integrated Module	BEOL layer as substrate	Amkor
SoIC	System on Integrated Chip	Heterogenous 3D dies connected with Si interposer	TSMC
SWIFT	Silicon Wafer Integrated Fan-out Technology	Fan-out	Amkor





- 2.5/3D / heterogenous integration packaging
  - Unlike previous generations of packaging technology:
    - No industry common architecture.
    - Each architecture is offered by only about 1~2 companies
    - Same or similar packaging architecture can have different assembly process flow and materials
    - New packaging architectures are constantly being introduced.
      - Often it is not clear if they are ready for production.
    - Existing architectures also evolve or discontinue
    - Technology seems to evolve faster over time
- A Mil-spec working group exists.



NEPP Task Scope Challenge

- No industry common architecture
  - Are there common features or materials?
    - What are the ones within our capability to study?
    - What are the aspects relevant to mil/space component?
- Difficult to obtain samples. Need to understand SoA industry practice better.
  - Partnered with GaTech

Name	Stands for	Description	Company
CoWoS	Chip-on-Wafer-on-Substrate	Si Interposer ("2.5D")	TSMC
EMIB	Embedded Multi-die Interconnect Bridge	Si Bridge	Intel
FOCoS	Fan-Out Chip on Substrate	Fan-out	ASE
FO-EB	Fan-Out Embedded Bridge	Fan-out	SPIL
FO-MCM	Fan-Out Multi-Chip Module	Fan-out	SPIL
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RDL Interposer	Redistribution Layer Interposer	RDL as interposer	Samsung
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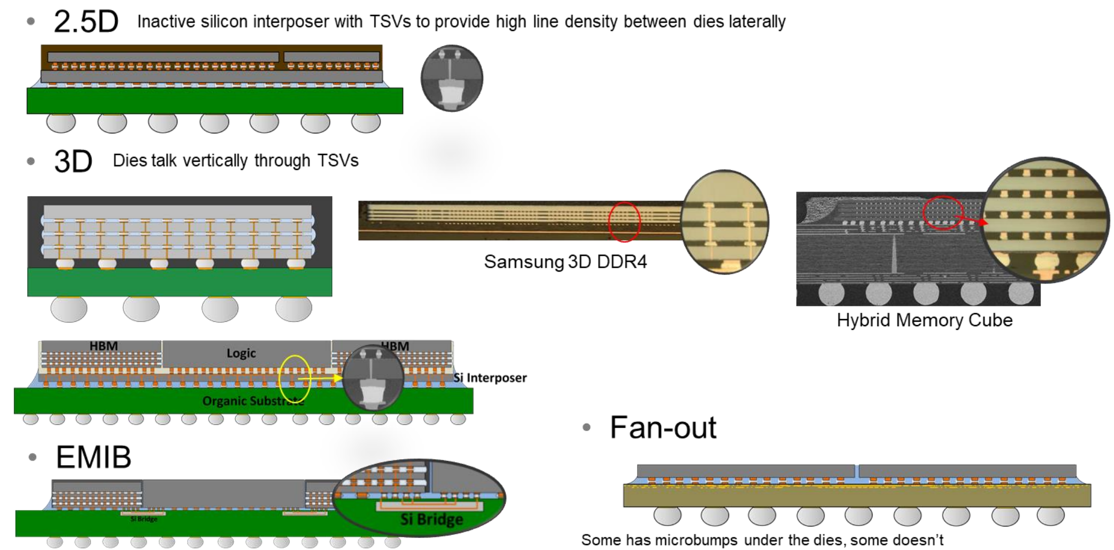
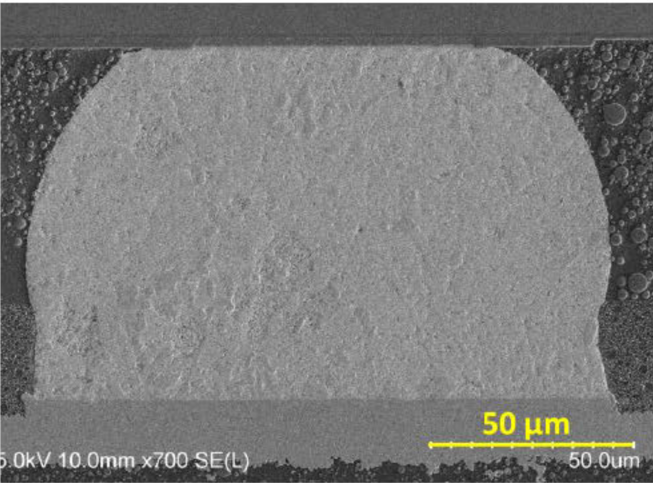
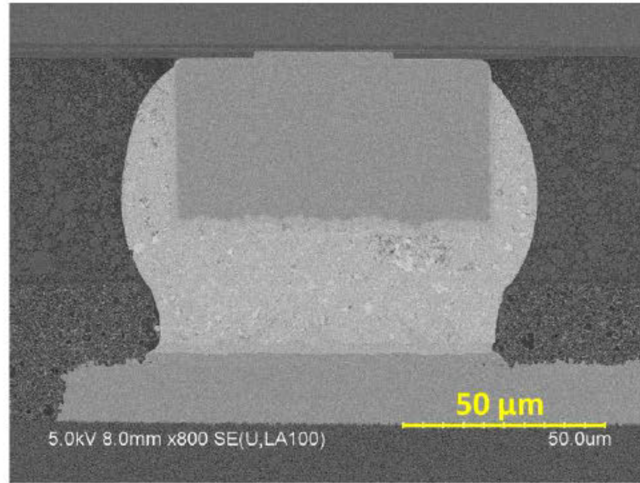


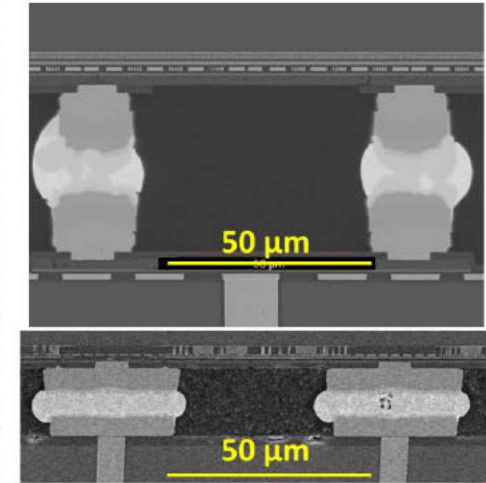
Microbumps

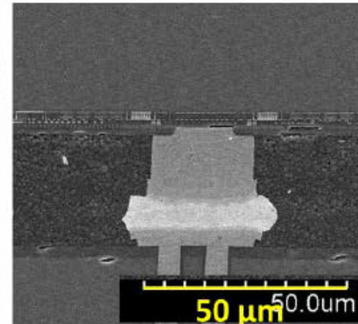


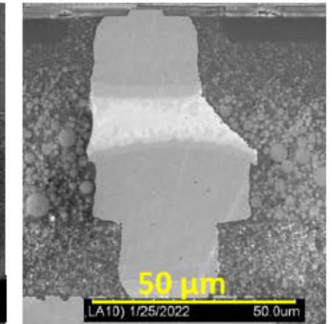
C4



C4 Cu Pillar

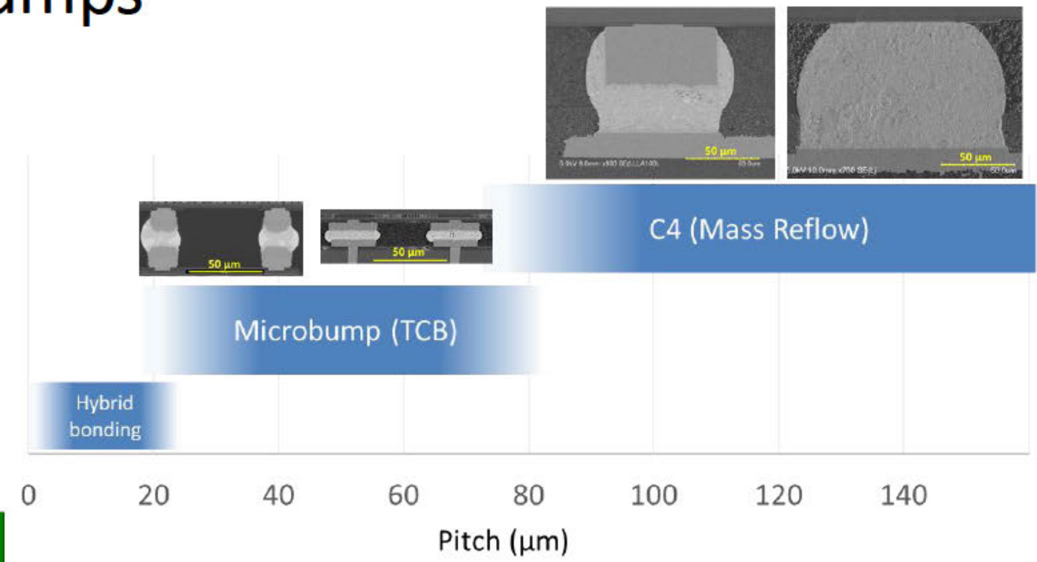


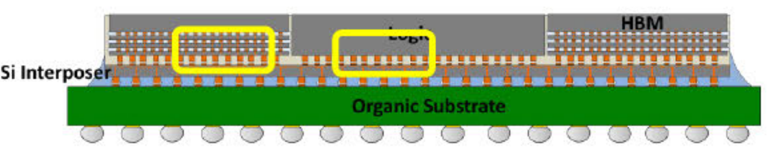


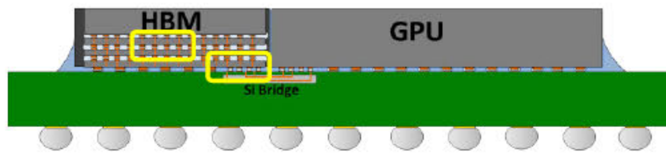


Fan-outs: some has microbump, some doesn't

- Microbumps are different from existing C4 bumps
  - Metallurgy
  - Assembly process





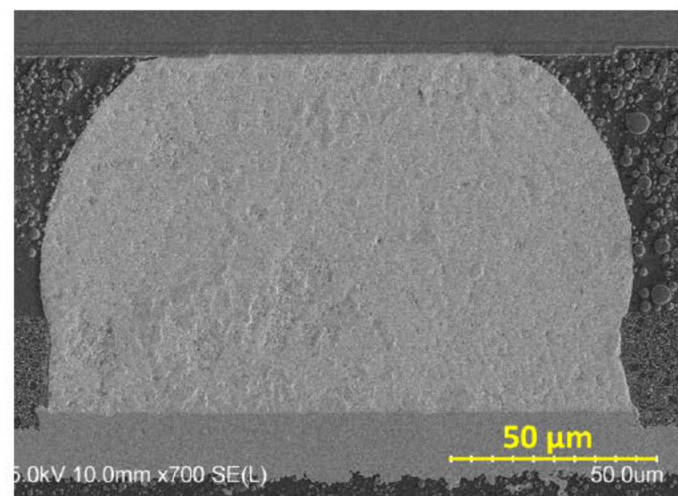


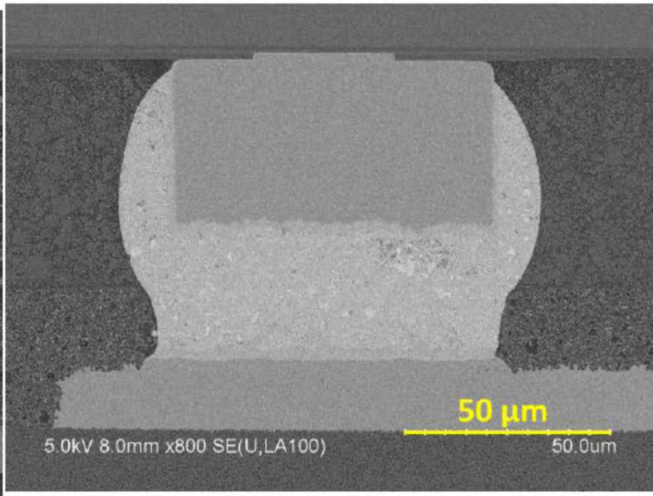
Microbump Metallurgy

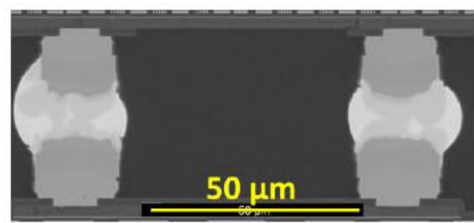
NEPP

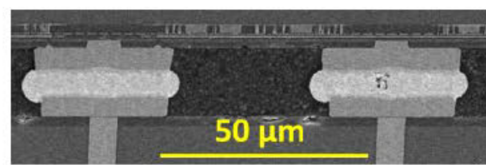
- Pb-free : This is now a reality we have to accept.
- Small solder volume
  - Effects of Sn consumption during reflow and thermal aging.
  - Increased volume fraction intermetallic compound (IMC) in solder joint.
- Not the main focus of current NEPP task
  - The field has a long history
    - Recent updates in the subject and trends will be reviewed.
- Examples of industry solutions
  - Solder composition optimization
    - Control of Ag_3Sn precipitate morphology and amount
    - Liquidus temperature less impacted by Sn consumption
  - Column/bump pad metallurgy optimization
    - Limit the growth of IMC. Control the growth of less preferred type of IMC.
- Potential overtesting
  - Depending on the package design, it is possible to demonstrate accelerated failure by promoting diffusion.

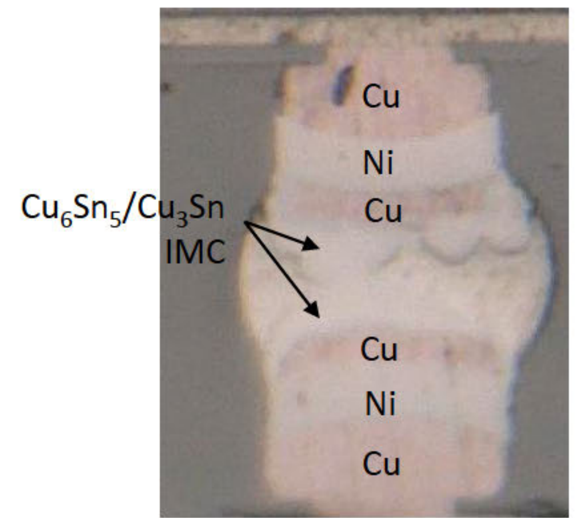
    ex) HTS → TC or long dwell at hot temperature during TC





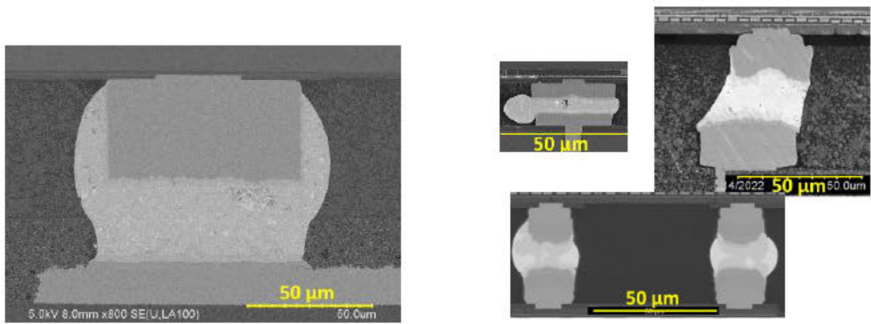


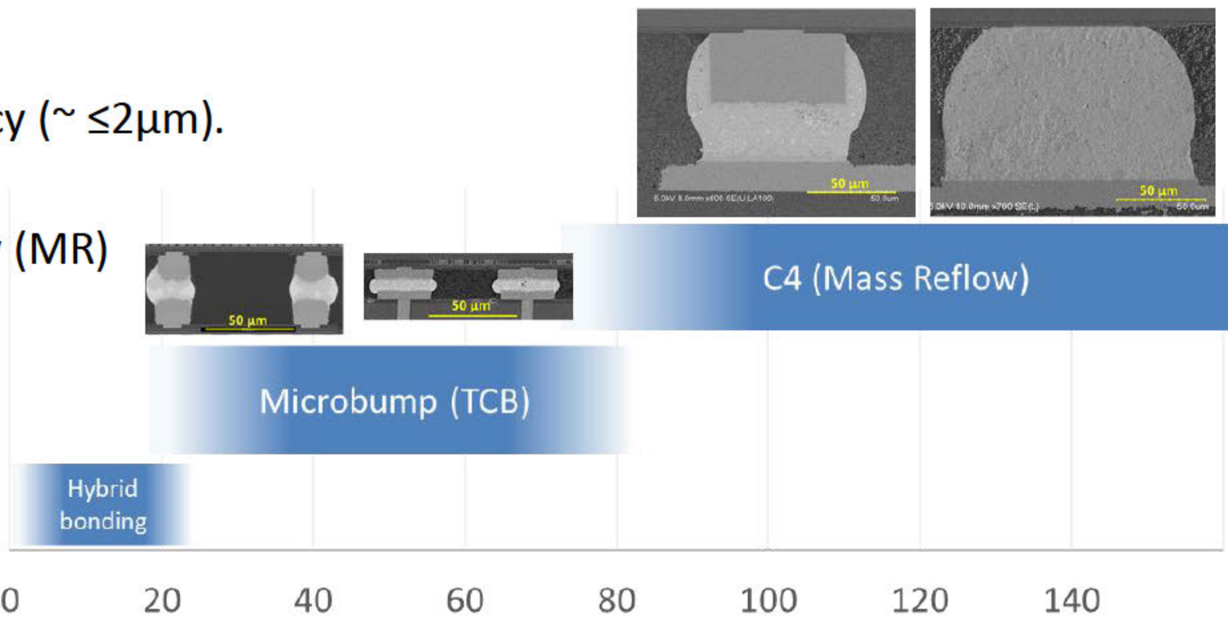


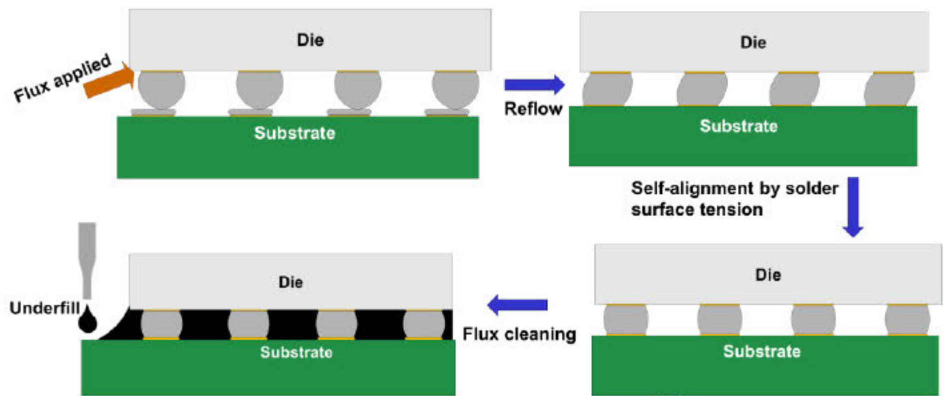


Microbump Assembly Process

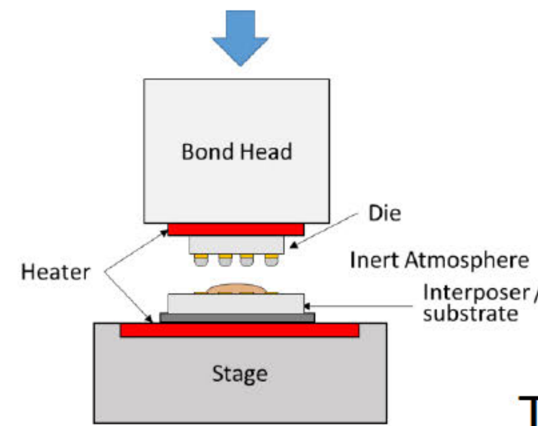
- Thermocompression bonding (TCB)
  - Temperature & force
  - Die can't self align by solder surface tension
  - Down to ~20µm pitch with greater die placement accuracy (~ ≤2µm).
  - Can better accommodate thinned dies.
  - Far greater number of process variables than mass reflow (MR)
  - Process duration is only a few seconds

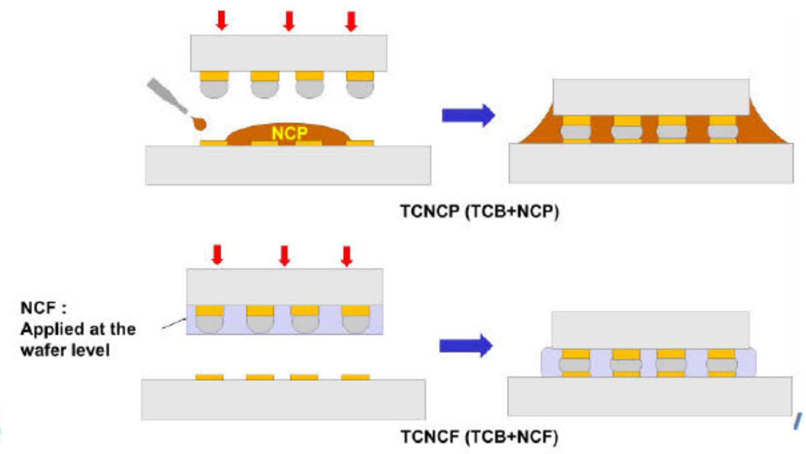




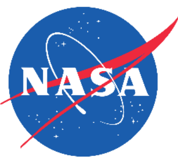


Mass Reflow



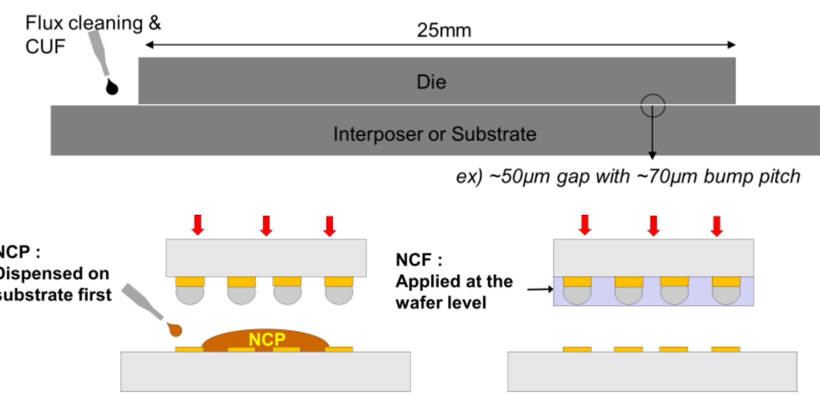


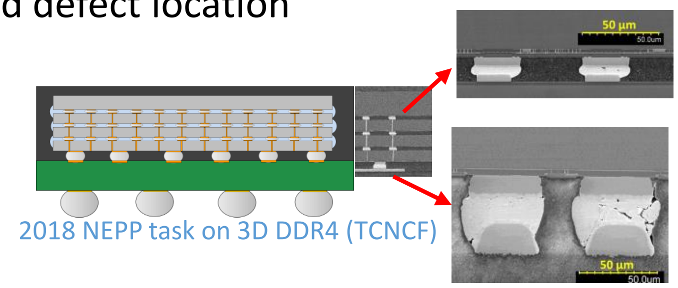
TCB



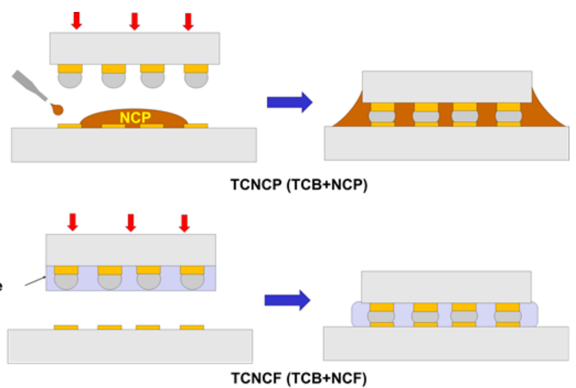
Thermocompression Bonding Process

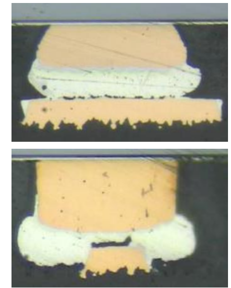
- TCB process & materials
  - More sophisticated than traditional mass reflow
  - Underfill challenges
    - Capillary underfill (CUF)
      - Increased voiding issue
      - Difficulty begins at ~100µm pitch, increasing as pitch approaches 50µm.
    - Non-conductive paste (NCP) : Defects
    - Non-conductive film (NCF) : Defects, Die shelf life (B-stage material applied at wafer level)
  - Defects during NCP / NCF attach.
    - Low-volume manufacturers can have difficulty in optimizing assembly process
    - Defects can't be detected by typical NDT
    - Defects may pass 38535 screening condition but cause early failure, depending on design and defect location
- NEPP focus
  - TCNCP bump reliability and screening.
    - Also microbumps with CUF



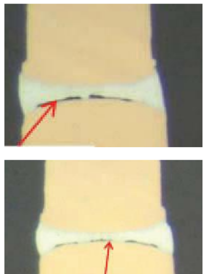


2018 NEPP task on 3D DDR4 (TCNCF)

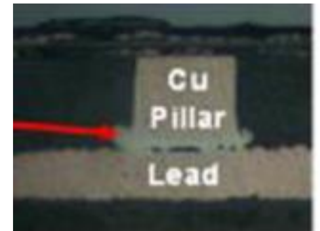




Y.M. Cheung, D Tian, Giuseppe Y. Mak, and Ming Li, EMAP 2013



L Yang, D Tian, YM Cheung, M. Li, EPTC 2015

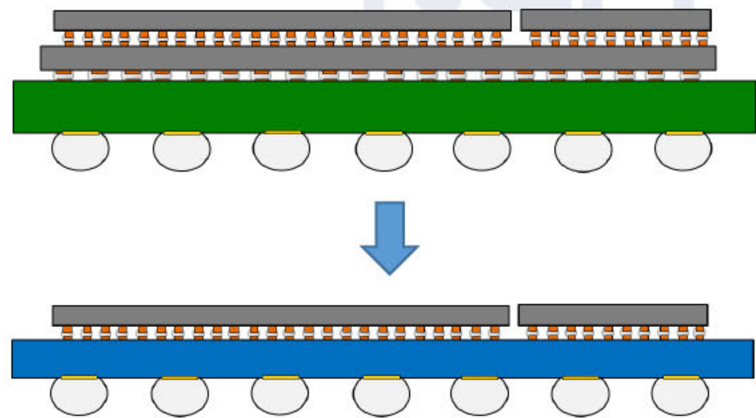


TCNCP bump in a commercial AP

John Lau, "Semiconductor Advanced Packaging", 2021, pp358

	MR	TCB
Main process variables	Reflow profile	Stage temperature, bond head time-temperature profile (ramp, contact, peak, release, cool), contact & bond force, bond head displacement, dwell time, etc.
Ramp rate	<1°C/sec average	~100~200°C/sec
Process duration	A few minutes	A few seconds
Underfill Cure	Typically 10s of minutes to hours	A few seconds for NCP or NCF

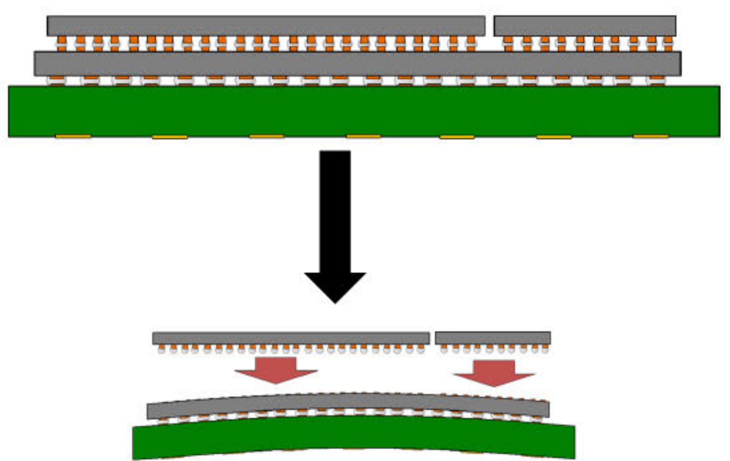
NEPP & GaTech Collaboration



- Challenges in defining NEPP task for 2.5/3D level-packaging
  - No industry common architecture
    - Focus the scope to thermocompression bonded microbumps
      - TCB process & materials
  - Difficult to obtain sample
    - Assembly process and materials are far more sophisticated than previous technologies
      - Need better visibility on how the samples are built, learn practical issues during manufacturing.
  - Need expert consultation to quickly identify industry common SoA practice
- GaTech Packaging Research Center consortium
  - International consortium
  - R&D scale SoA prototyping capability with visiting engineers from industry
  - Connection to packaging, equipment, and materials companies through international consortium
- GaTech Packaging Research Center's current focus is on glass substrate technology
  - ex) Heterogenous integration on glass substrate, RF, embedded component, photonics, ≤1 or ≤1.5 μm line width/spacing
  - There are companies (ex: SKC) about to release glass substrates to the market.
  - GaTech professors : Suresh Sitaraman and Vanessa Smet

Advanced Substrates and Space Component

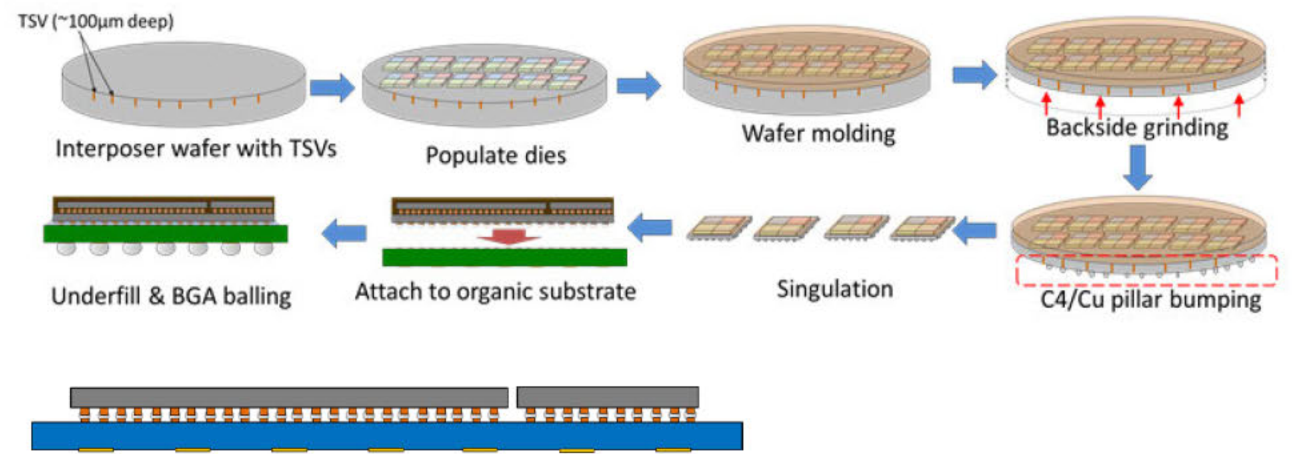
- Supply chain issue for mil/space component business
  - Actual issue according to industry people
  - Low-volume, high mix applications
- Advanced substrates can enable production in-house or at average size packaging companies

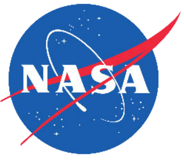


ex) 100µm thick, 40mm wide interposer

Assembling individual Si interposer and dies on organic substrate :
A lot of engineering might be required per product and lot, especially when mixing dies with different die and bump geometry.

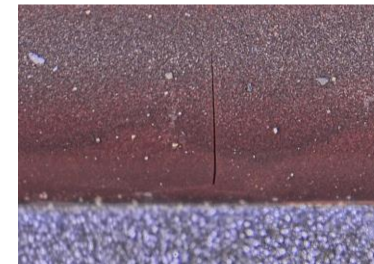
Advanced Substrates
(No interposer needed)



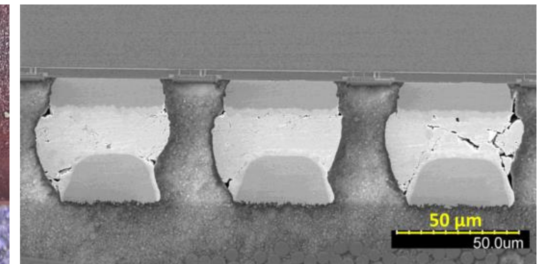


Current NEPP Task Scope

- Study quality and reliability of 2.5/3D-level packaging, in focus of microbump interconnection and underfill.
  - Impact of materials and assembly process
- Learn commercial industry common SoA practice and issues
- Design and build test articles
  - Interconnections representative of actual 2.5/3D-level packages
  - Learn practical challenges in package assembly
    - GaTech to share detailed progress in process optimization during sample manufacturing
- Reliability study
  - Perform reliability tests and FEA
  - Study dominant failure mechanism
    - Depends on design, material, & process.
    - Useful in developing/reviewing PIDTP.
    - How things fail eventually, what happens if design or material changes
- Longer term goals
  - How should PIDTP be structured?
  - Screening? Lot qual?
    - Defects passing 38535 screening condition but causing early failure



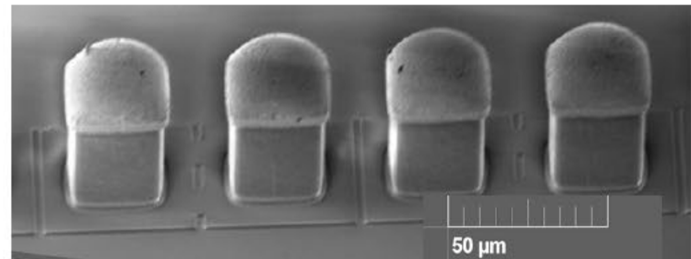
Underfill crack/delamination

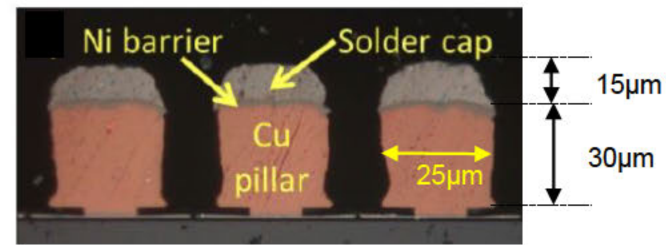


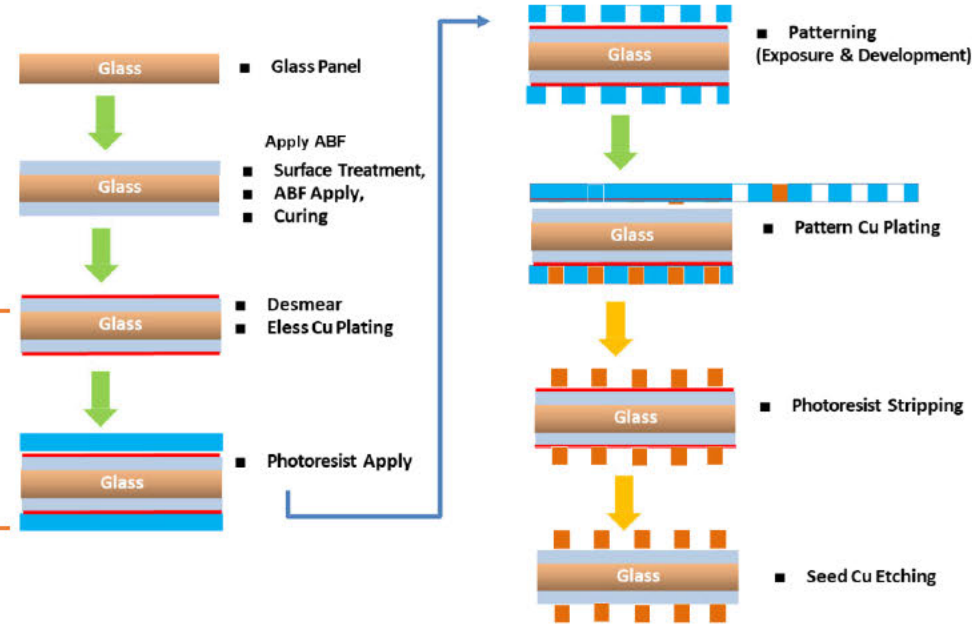
Solder joint fatigue

Current Phase Test Vehicle

- 50µm pitch Sn2.5Ag bump
- Glass substrate
    - Glass core
    - ENEPIG finish for the current phase. 50-100nm Pd, 50nm Au
    - Fabricated at GaTech
    - Industry production substrate in upcoming phases



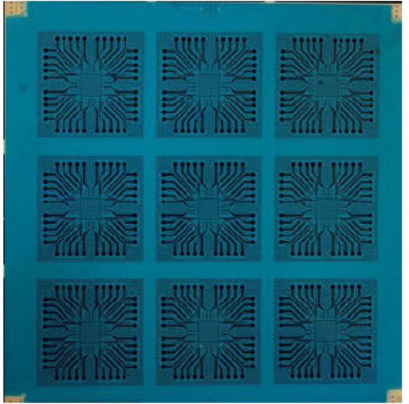


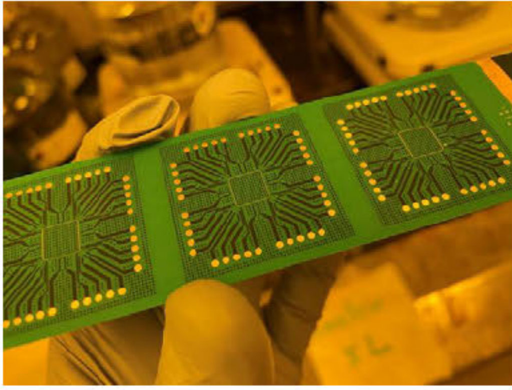


Solder resist	~15µm	SR-FA
Copper pattern	~8µm	Copper
Dielectric	~15µm	ABF GX-92
Glass Core	300 µm	7.8 ppm/C CTE glass
Dielectric	~15µm	ABF GX-92
Copper pattern	~8µm	Copper
Solder resist	~15µm	SR-FA

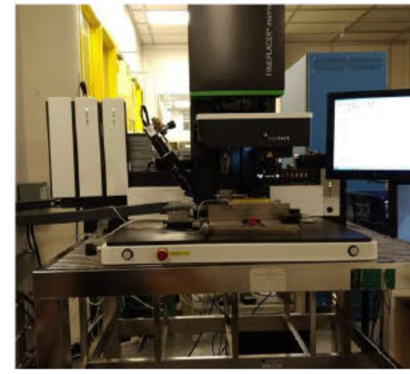
Bump pitch	50 µm
Bump	Cu with solder cap (Cu: φ25µm)
Bump height	Cu 30µm+Sn2.5Ag 15µm
Die dimension	7.3mm x 7.3mm x 725µm

Sample Assembly



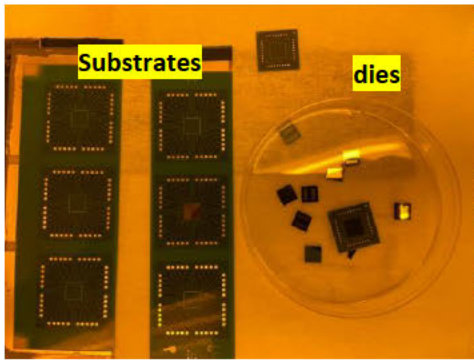


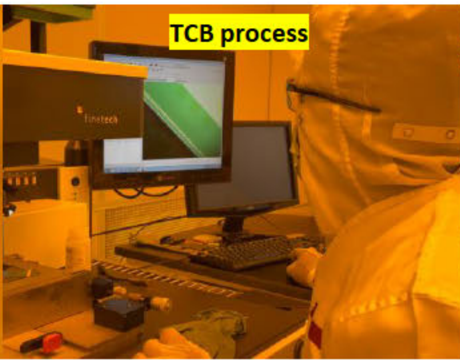
Sub-micron Flip-chip Bonder (Finetech)

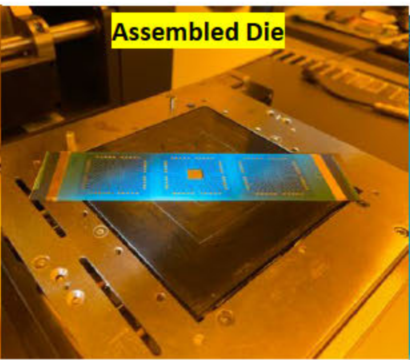


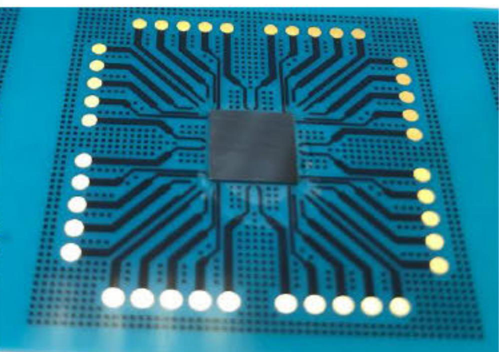
Semi-Automatic Flip Chip Bonder (Finetech)

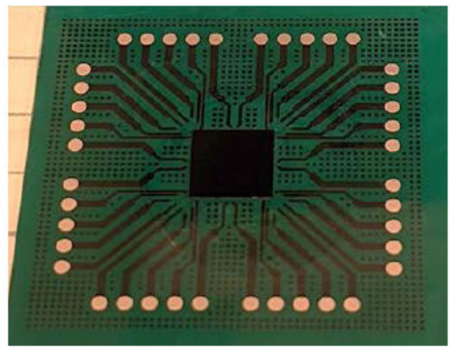
APAMA C2S (K&S)

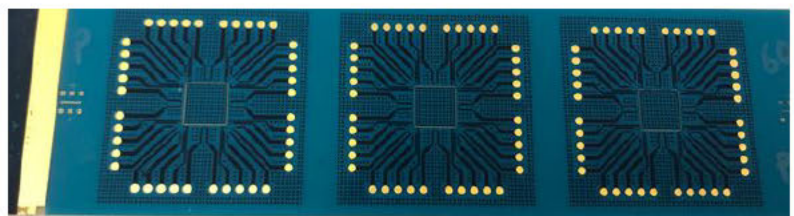


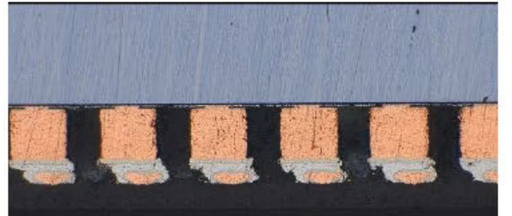






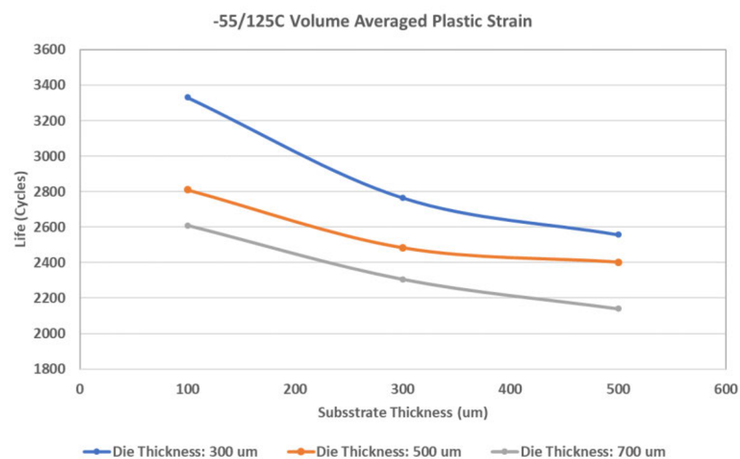


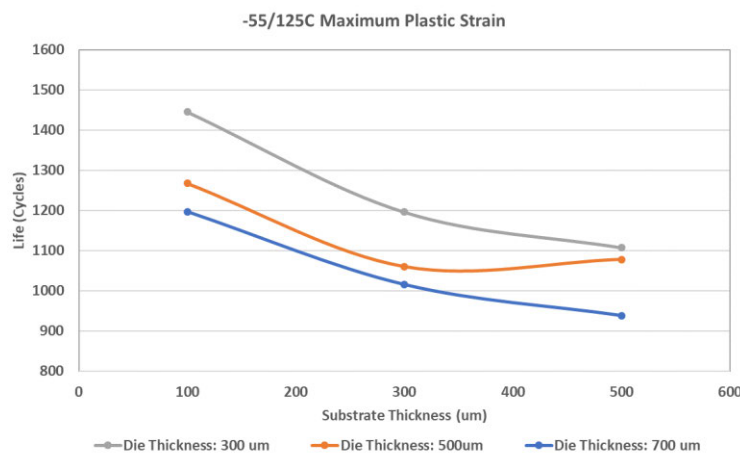


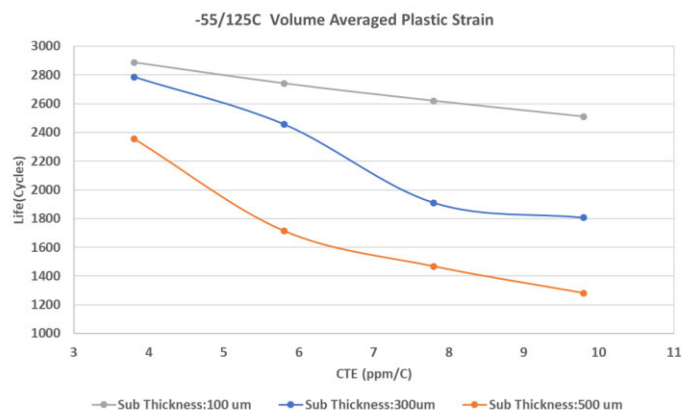


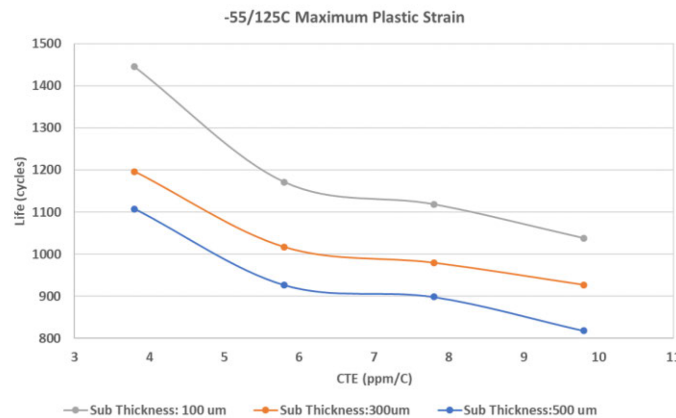
FEA

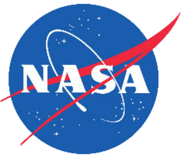
- Non-linear analysis with solder viscoplastic behavior and hysteresis.
- Assembly process cycles and IMC growth are also factored in.
- Effects on design parameters on temperature cycling life were modeled.







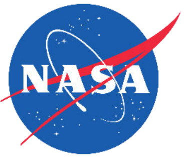




Reliability Test Condition

NEPP

- -55/125°C temperature cycling
- Humidity temperature bias or autoclave
  - THB : 130°C/85%RH or 85°C/85%RH
  - Autoclave : 121°C, 2atm
- Failure analysis
- Projected duration of test & failure analysis is 3.5 months.



Summary

- The current NEPP task focuses:
  - Reliability of microbump interconnection and underfill in 2.5/3D-level packaging.
  - Advanced substrate technologies are a viable option for low-volume, high mix application.
- The initial sets of samples are manufactured.
  - Reliability tests and failure analysis will follow.

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