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2022 NEPP ETW

ARM Radiation Testing Update

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Special Acknowledgement to: Chuck Corley (UT Austin/LANL CSES Fellow), Heather Quinn (LANL), and David Hansen (SpaceMicro)

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Outline

- ARM Update
  - Task Overview
  - Current Focus on A53
  - Raspberry Pi & Freescale MX8M for A53
  - Future Work
- Raspberry Pi Guideline Update
  - Overview of Guideline
  - Samples from Guideline
- Conclusion

ARM Processor Testing Overview

- Understanding processor testing for space
  - What's it going to do with radiation
    - Calculation errors – possible incorrect operation
    - In fact, falling on its face is more likely, requiring reset
    - May permanently fail
  - Test approaches
    - Low-level structures – the old approach, and still used for RHBD devices
    - Application based
- Build collaborations
  - Maximize budget impact by covering more of the space
  - Identify key mission needs – reliability, cost, performance, relevant data
  - Develop better metrics to enable comparison of devices
    - For example, the entire SWAP required to implement a system
    - Dissimilar processor architectures should not always be compared
- Key issues
  - Limited documentation, expensive evaluation equipment, complex system design and complex error modes, potential severely limited hardware options (partner chips, etc.)

*Task Partnering

- Engaging in collaborative efforts: Updated for 2022
  - Heather Quinn, LANL, and other members of the Microprocessor and FPGA Mitigation Working Group
    - Including Chuck Corley (UT, Austin/LANL CSES Fellow)
  - David Hansen SpaceMicro (Added for 2022)
  - Paolo Rech – GPU/Applications, UFRGS, ARM Collaboration
  - Carl Szabo, Ed Wyrwas, Ted Wilcox, and Ken LaBel, GSFC
  - Larry Clark, ASU
  - Sergeh Vartanian, Andrew Daniel, and Greg Allen, JPL
  - Vorago Technologies – collaborating on hardware/plans
  - ARM collaboration – realigning based on A5 efforts

- Looking for additional collaborators
  - Tester side – are you testing processors?
  - Manufacturer side – knowledge or hardware support
  - Application side – specific applications…

What are We Really Trying to Do?

- The key question revolves around: is the A53 (or other target) core intrinsically “better” than some other core?
  - ARM cores, and RISC-V cores, as well as other architectures.
- To answer this question involves many facets:
  - Implementation of Fault Tolerance Features
  - Process node
  - Operating system/system configuration and operation (even privilege level)
- This testing of Raspberry Pi and MX8M is intended to highlight if there is a critical difference between these two cores, and
  - Can the difference be chased to the caches?
  - Is any difference potentially masked by system architecture (SOC)?
  - Or are the differences essentially no more than anticipated from process?
- Why: Because the non-space sectors are making better and better systems for fault handling, and if we’re smart, we can pick units that may work well for us.

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Why A53

- A53 focus for NEPP serves three purposes
  - Popular 64-bit processor core
  - Implementations may chose to implement fault tolerance
  - Good vehicle to branch into other ARM cores (such as 7x and 9x, etc)
- Readily-available evaluation systems.

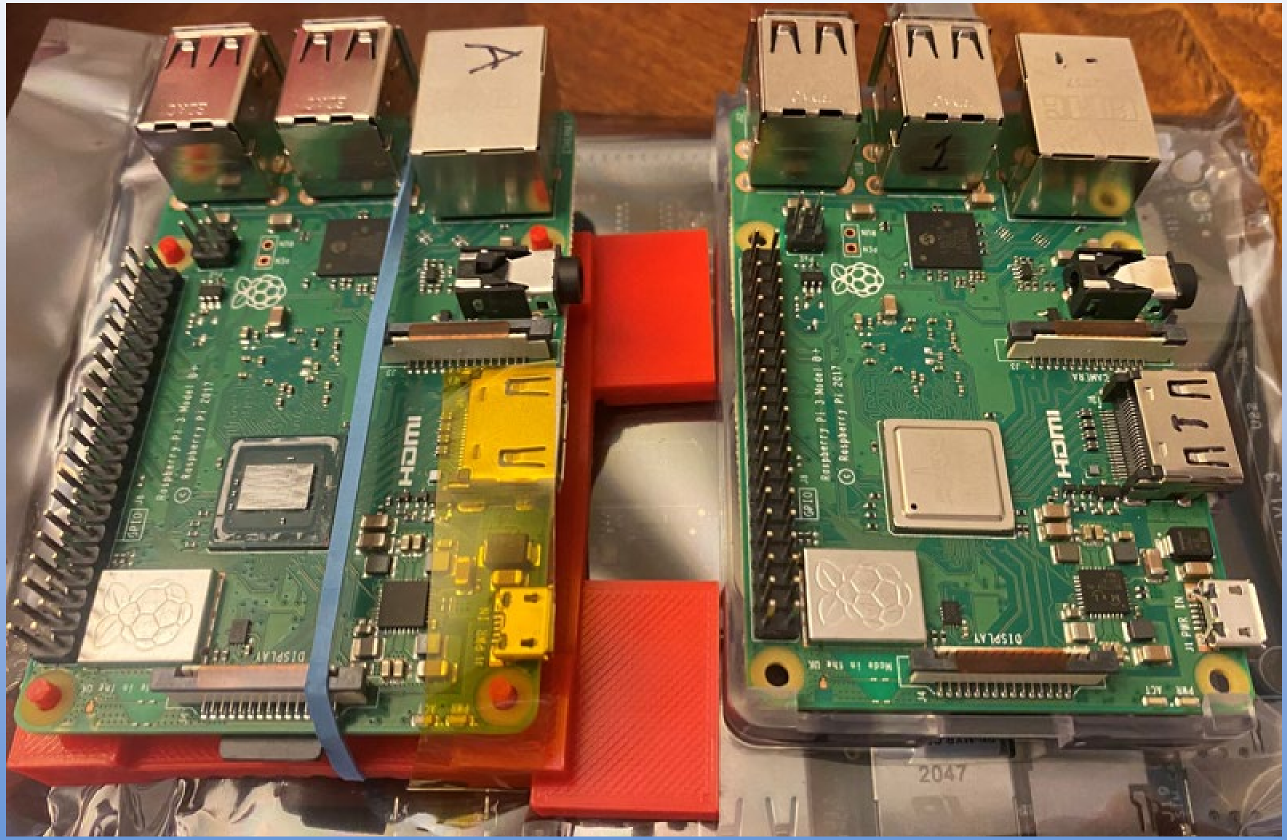
- But it is getting long in the tooth (old).
  - This has pros and cons
    - Many dev boards, lots of documentation, lots of hardware support
    - Less implemented FT, not recommended for new (high performance) developments (like HPSC)
- Big step up over A5 – but minimal detailed design support

Raspberry Pi for A53

- Raspberry Pi 3B+ has quad-core A53
  - Lots of community support
  - There's even an 11-hour online course on making your own operating system for Raspberry Pi
- Initial indication was that caches support error correction, but detailed review (and pulling on chip configuration registers) resulted in conclusion there is no error correction.
  - Test results (still in analysis) (seem to) confirm this.
- Some testing has been done (both for ARM effort, and for Raspberry Pi Guideline)
  - More schedule – for next week!

Raspberry Pi Prep

- Raspberry Pi Prep
  - Remove heat spreader
  - Thin DUT
  - Thermal control limited to convection (working)
    - Impacts test approach
- For NEPP, goal is A53 testing (not full Raspberry Pi)
  - Reduced thermal load



Testing Earlier this CY

- Preliminary testing of Raspberry Pis in April gave promising results.
  - Obtained about 30 crash runs across 5 operating modes.
- Test Codes/Operating Modes
  - #CPUs = 0 vs. 4 – allows Raspberry Pi to run single or multi-core
  - "Cache Test Codes"
    - 400 bytes – only uses small portion of L1 cache, allows OS to retain data in cache
    - 32000 bytes – try to use all of L1 data cache
    - 12.8M bytes – try to force all memory off chip
  - Sleep test – 99% inactive
- One obvious question – what if the cache test size fits in L2?

Analysis of Pi Codes - April

- Looking at KUtrace report:

	Version	Trace ID	IRQ	Trap	Syscall	KU spans	user	system	idle
	CPU=0								
32k	Original	march_2	812,324	6,469	116,758	2,483,386	68%	4%	28%
400	Small	march_4	684,724	4,783	109,781	1,890,926	80%	3%	17%
12.8M	Large	march_3	798,050	19,399	113,374	2,371,649	70%	4%	26%
	Sleep	march_5	632,220	6,748	84,081	3,052,935	1%	6%	93%
	CPU=4								
	Original	march_9	909,088	6,614	89,729	2,642,621	71%	1%	27%
	Small	march_10	912,244	7,692	108,446	2,702,008	71%	1%	28%
	Large	march_11	956,758	22,234	82,966	2,530,810	72%	2%	26%
	Sleep	march_13	814,639	6,623	87,966	3,867,787	0%	2%	98%

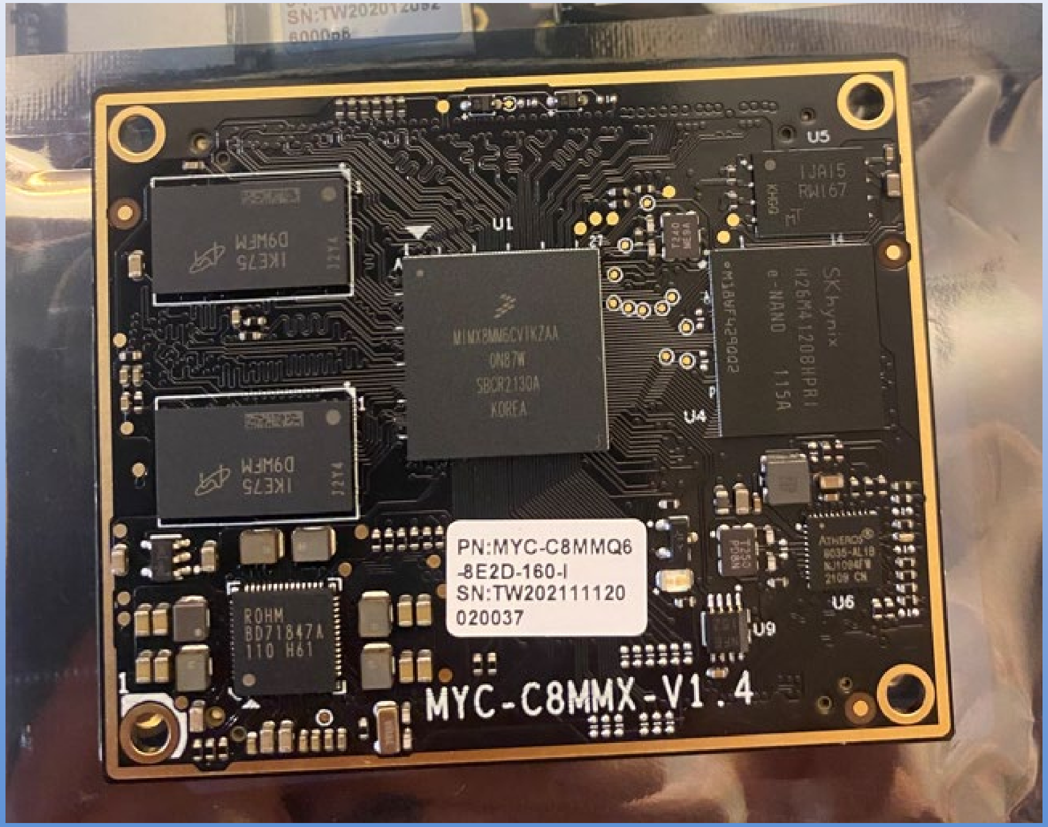
- KUtrace analysis by Chuck Corley (UT, Austin/LANL CSES Fellow)
- Page faults (shown in Trap heading) much more common with off-chip size.

Results

- Only quantitative results we have are with boron. LET is about 3 MeV-cm^2/mg after going through about 500 µm of Si.
- Cross section for crashes all conditions was about 1.2×10^{-4}cm^2
  - This result is consistent with sleep, where there were 5 events in 5.5×10^{4}cm^2, for a cross section of ~0.9×10^{-4}cm^2.
  - This result may be consistent with 1-core operation, where there were 8 observed crashes in 1.4×10^{5} ions/cm^2, for a cross section of (0.25-1.1) $\times10^{-4}$cm^2.

MX8M Compute Module

- MX8MM6CVTKZAA, Quad-Core A53
  - https://www.nxp.com/part/MIMX8MM6CVTKZAA#/
  - Developing configuration data and test plans now.
  - A53 Cores have SECDED on L1 Data Cache and L2 Cache (L1 Instruction Cache protection not needed).
- Preparing DUTs now
- Collaborating with Dave Hansen (SpaceMicro) on test approach.



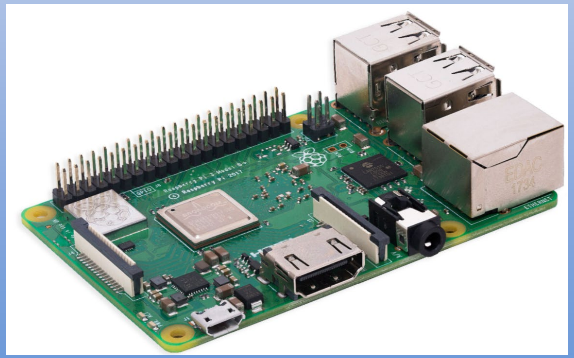
Upcoming Testing

- Expect to have Raspberry Pi and MX8M at LBL for testing soon (exact date is TBD… but next week).
- Focus is on "crash testing", but using codes targeting different amounts of cache usage.
  - Previous testing showed cache errors… but can we detect anything else before crash?
  - Might be limited because of unprotected cache.
- Approach right now is to run codes on both platforms, using Linux (Raspbian on the Raspberry Pis, Yocto on the MX8M).
  - Some question about how to directly compare these. But cache results and certain types of code errors will be obvious.

Guideline Development for NEPP

- Primary goal: deliver a brief guideline on recommendations for use of Raspberry Pi for flight. – Delivered in 2021.
  - https://nepp.nasa.gov/docs/papers/2021-Guertin-Raspberry-Pi-Guideline-CL-21-5641.pdf
  - Key info for rad hard alternates – depending on use
  - Tailored to key issues of:
    - Environment
    - Applicability of test results and prior history of other Pi's
- Driven by architecture review and available data on flight use
- Support existing data this with key radiation testing
  - Existing data highlights a lot of potential issues.
  - Some key questions regarding Pi-to-Pi, and operating mode sensitivity were addressed.
  - Possible augmentation with additional testing in the future
    - This is an "as of now" document. But this space is changing quickly.

Raspberry Pi Compute Module 4



Raspberry Pi 3 B+ (in Astro Pi as of Sept. 17, 2017 upgrade)

Raspberry Pi's in Space

- These are just the ones that reported (Thank You!) and were relatively easy to find.
- Opal CubeSat, GASPACS CubeSat, Utah State
- PiSat PES University (GSFC)
- Surrey Satellite Technology DoT-1
- CisLunar Explorer's CubeSat Cornell
- AAReST (Caltech/University of Surrey)

(Unclear how many of these launched and/or delivered flight data.)

Obligatory photo of Raspberry Pis floating in space!

(Luca Parmitano) https://www.raspberrypi.org

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Typical Uses for Raspberry Pi

- There are a set of things that are often done with Pis.
- Some of these line up well with off-loading spacecraft workload.
- So, they clearly have some potential value in spacecraft.
  - Need to use smartly.
  - Identify better alternates.

Application/ Description	Enet/Wifi	Quad Core	GPIO	Camera	USB	SATA	Other
Sensor Monitor Log and control remote sensors	Yes	-	Yes	-	?	-	?
Remote Operations/Actuator Translate network to hardware to operate devices	Yes	-	Yes	-	?	-	?
Desktop PC Use Raspberry Pi as desktop PC	Yes	Yes	-	-	Yes	Yes	AV Connections
File Server/Storage File system/repository	Yes	?	-	-	Yes	Yes	-
RC/Robot Control Remote operation of car/robot	WiFi Only	?	Yes	Yes	?	-	May use AI/Automation
Data/Image Analysis Run classification or AI offline	Yes	Yes	-	-	?	?	-
Camera Use as camera/record & transmit images; can be used for stop motion or timelapse	Yes	?	-	Yes	Yes	Yes	-
System/Network Monitor Use Raspberry Pi to monitor system/network and issue maintenance commands	Yes	-	?	-	?	-	-

Guideline discusses alternatives to Raspberry Pi for some of these use cases

Radiation Eval for Pi Guideline

- Key question: What is a good test for Raspberry Pi (not A53 specifc) radiation sensitivity?
  - Typical application? Worst Case application? Which interfaces (Ethernet)? Which resources (GPU)?
- Total Ionizing Dose
  - Several studies: NEPP previous evaluated Raspberry Pi B finding they worked to above 40 krad[Si]. Decena's work on Opal Cubesat showed >100 krad[Si] on Raspberry Pi Zero. Toumbus found similar performance on Raspberry Pi compute module 3.
  - Testing for this guideline focused on: Irradiating the entire board (flash memory isolated), characterizing operations between dose steps.
- SEE
  - There are not a lot of SEE tests of Raspberry Pis – no viable information was found to include in the guildeline.
  - We tested raspberry pis using Lawrence Berkeley National Laboratory (LBL) 16 AMeV beams – note that these are NOT sufficient to expose all components of the Raspberry Pi.

Radiation Data Problems

- The simple truth is, nobody has the appropriate parts traceability on Raspberry Pis to be able to apply any test data to any particular flight unit.
  - This is the typical flight lot/lot traceability, issue.
  - So… it's a shot in the dark. Maybe your board performs beyond 10krad[Si], and maybe its LEO SEFI rate is ~1/1000 days. Maybe it is worse.
- The other problem is the Flash memory.
  - This topic is out of scope here. Generally, larger SD cards will have worse SEE and TID performance.
  - But, even brand-new, "good" manufacturers might give you a dud Flash drive.
  - And if not… there is just no good way to establish radiation performance of the card without a good parts program.
- All the tests have some limitations regarding potential use case.
  - It is not reasonable to expect Raspberry Pi radiation testers to be able to cover all of the portions of the Pi that might be used.
  - But, the effort is typically to cover as much as possible, while limiting beam charges.

Conclusion

- NEPP is developing a knowledge base on ARM processor core intrinsic SEE performance.
  - This is primarily driven by configuration choices (especially FT).
  - There is an impact due to process and operating mode.
  - Currently exploring A53 in Raspberry Pi and NXP MX8M
- Recent testing has shown the Raspberry Pi A53s are likely driven by L1 data cache errors causing crashes.
  - Not significantly improved by running in sleep mode. But single-core operation may give some reduction.
  - Unclear how the rest of the chip may contribute to error rate.
- Additional A53 test data will be developed over the next few months.
- Raspberry Pi Guideline has been released and is available for download.
  - Gives overview of risks due to SEE and TID, and how those risks relate to operating environments.
  - Explores applications and alternatives in various price ranges for users.

Processor Enclave Biweekly Call

- Please let us know if you are interested in participating
  - Looking for other doing testing of commercial devices and next-generation RHBD devices
  - Primary goal of the call is to try to minimize overlap and maximize testing and effectiveness of testing within NASA and participating government programs
  - Assistance is helpful from: testers, manufacturers (including ARM, RISC V, etc.), and applications designers (what do you guys really need?)
  - Or if you have a program and are looking for data or are interested in helping shape upcoming testing
- Next call is 7/1/2022

END