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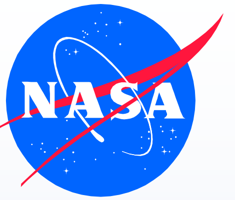

2022 NEPP ETW

HPSC 22FDX Radiation Update

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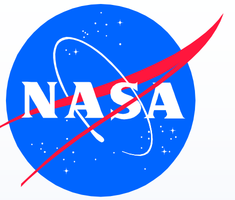
Outline



- 22FDX Programmatic Overview
- Current Status of HPSC
- Current Activities in 22FDX
- Forward Plans for 22FDX
- Review of 22FDX Data Products
- Conclusion

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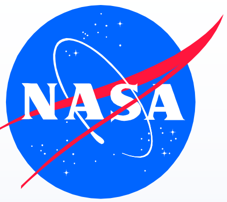
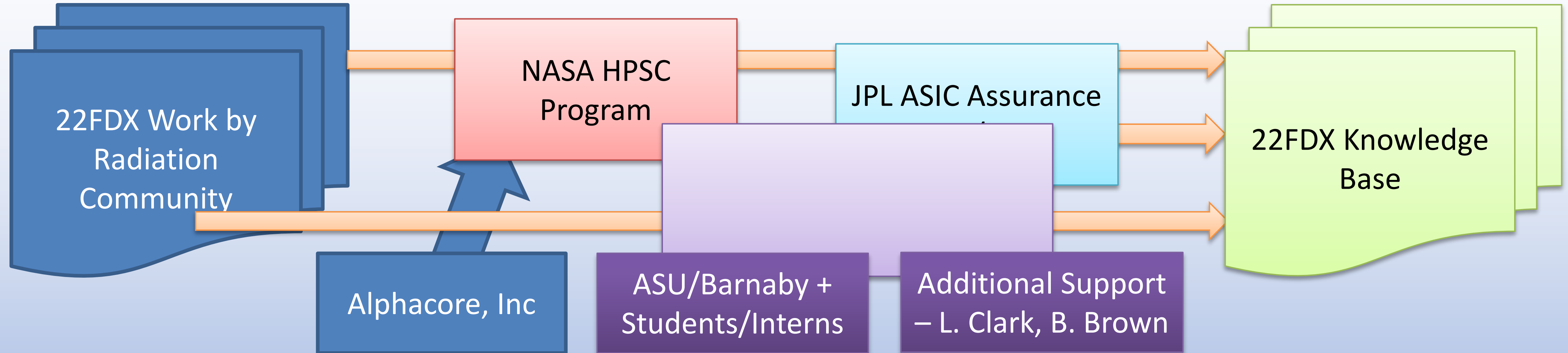
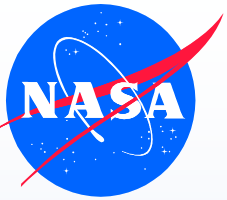


22FDX Programmatic



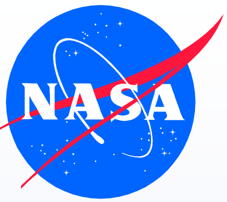
- Promising initial data on 22FDX – still looks “good”
- HPSC Program augmented existing data (+hard IP, production library data)
  - No further 22FDX data plans, but 22FDX is viable
  - General finding: As long as recommended practices are followed, 22FDX can meet TID and SEE requirements for HPSC (and HPSC-like) mission profile.
- JPL ASIC Assurance internal research
  - Expand on some key gaps in 22FDX data (analog, other SRAM configurations, improved transistor curves, possible expansion of dose and SEE hardening options)
  - Focus on developing technology level assurance methodology, assessing technology, foundry interface/tool, & use of test structures to fill in gaps to ensure success of ASIC for flight implementation. Method is transferrable to any technology of choice

Overview of 22FDX Work



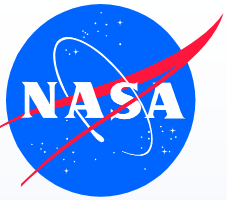
- Prior/External to HPSC
  - Reviewed and consulted with several groups, including GSFC, ASU, Cern, and GlobalFoundaries regarding existing data an efforts.
  - Critical issues found with limited TID capability, but these deemed to be likely acceptable for most NASA work (i.e. >100 krad[Si])
- HPSC Results (final test chip evaluation “completed” 3/31/2022)
  - Full review of most critical elements of approach to build ASICs on 22FDX for NASA use.
- Extended HPSC Results (some analysis still being completed)
  - Extended review of SRAM annealing.
  - 3rd party IP extended evaluation, such as “minimal use” or annealing configuration.
- ASIC Assurance Efforts
  - Initial transistor curves quantifying TID impact from GF transistor chip
  - Additional test chip being worked
  - (Experimental circuit) May significantly improve transistor response curves
  - Explores different SRAM options in more detail
  - Some alternate gate chain configurations will be explored.

22FDX Data Topics/Test Chips



TID	Transistors	Leakage, Vt, Slope	Basic Response
	Gate Chain / Ring Oscillator	Leakage, Frequency	Operation, Transistor Models, Support Circuits
	SRAM	Leakage, Bit Failures, Pattern Dependence	Cell & Peripheral Config
SEE	SRAM	Cells, Decode, Bit & Word Line Errors	Intrinsic SEE before ECC
	FF / Dynamic	SETs	Models
	FF / Static	Gate Structures, DICE	Impact on SEE/SEU

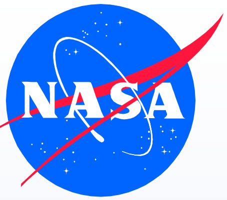
HPSC Requirements*



- Context: Meet the needs of a majority of NASA missions without over-designing on elements that are hard to achieve.

Radiation Tolerance Metric	HPSC
TID	200Krad (Si)
DD	$10e^{10}$ MeV/g-Si
SEL	75 MeV-cm^2/mg
SEE SoC configuration controller and all HPSC resources required for its access to memory, I/O, and SoC status and control registers	$1e^{-5}$ uncorrected errors/device-day (Adam's 90% worst-case GEO environment)
SEE SoC configuration controller and all HPSC resources required for its access to memory, I/O, and SoC status and control registers	$1e^{-3}$ uncorrected errors/device-minute, for the worst 5-minute period of the October 1989 design case flare in CRÈME 96

Phase 1 General Findings



- Vendors proposed 22FDX, 12LP, and 12LP+.
- 22FDX will meet all requirements for all basic device elements except 3rd party IP which may require annealing or other consideration to meet TID.
- 22FDX appears to slightly outperform 12LP and 12LP+ for SEE, while 12LP and 12LP+ significantly outperform 22FDX for TID.
  - Note that SEE result might be related to unverified angular effect where FinFETs perform much worse at normal incidence.
- **All technologies considered viable for HPSC down select.**

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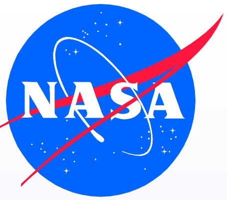
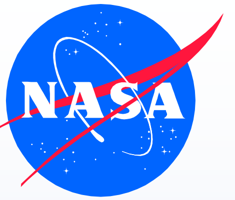
Phase 2 Selection



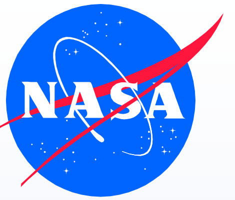
- HPSC will use 12LP+, with additional radiation data to be provided.
  - Will need verification that SEE risks are mitigated.
  - Uses a high reliability controller portion of the chip.
  - Additional details on implementation of SEE/fault tolerance/redundancy required to ensure meeting SEE requirements.
  - Will verify TID exceeds 200 krad[Si] before production, and in post-production verification tests.

Expected Design for Phase 2



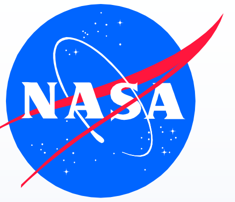
- High reliability core architecture, with lower reliability requirements for high performance application processors
- Multi-Core RISC-V System
  - Supporting NMR and DCLS
- ASIL-D rated on-chip networks

Timeline for HPSC Phase 2



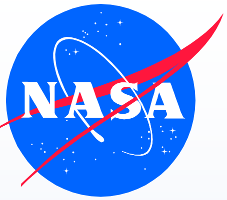
- HPSC is expecting to execute an 11-quarter effort.
- Initial delivery of SoC on an evaluation board is expected by Q3 2024.
- Validation/qualification testing will be conducted in late 2024 into 2025.
- Chips will be broadly available for bench use by Q1 2025.
- Space qualified parts available from storefront Q3 2025

Where does this leave 22FDX



- HPSC phase 2 will use 12LP+.
  - There are tradeoffs between 22FDX and 12LP+
  - 22FDX meets the design requirements for HPSC as does 12LP+
- But, the devil might be in the details.
  - Most of 22FDX will work fine to well over 200krad, but some 3rd party IP may have issues at 150krad.
  - 22FDX does have higher leakage and faster response to TID, so corner cases and operating envelope considerations are required.
  - 22FDX will "test better" for SEE relative to 12LP/+, but this may be because 12LP/+ is intrinsically "bad" at normal incidence.
    - 12LP/+ overall angular response might still be better than 22FDX.
    - 12LP/+ may also have increased issues with multi-node hits where 22FDX is more resilient.
  - 22FDX is much less expensive and easier to execute for designs/design teams.
- **22FDX characterization will be continued by the JPL ASIC Assurance Task**

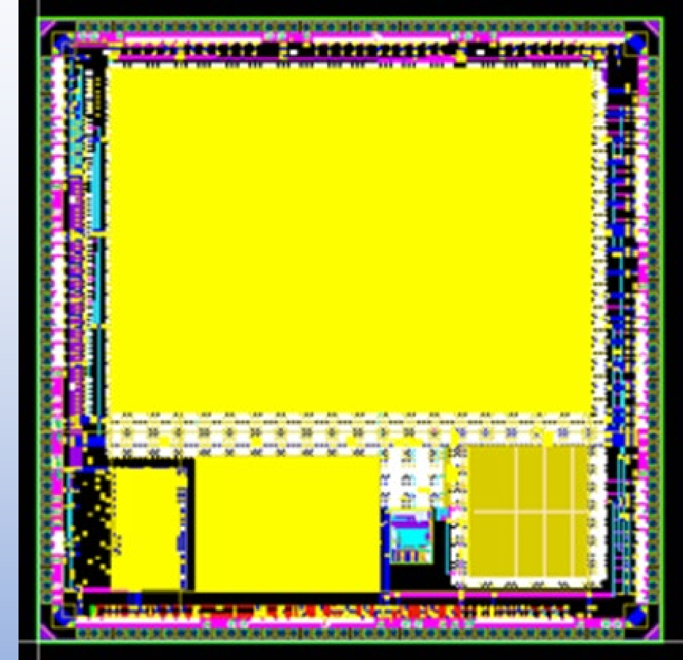
Current State of 22FDX



- TID – The following are expected to function well, with minor increases in leakage current (below 200%) up to 200 krad[Si].
  - LVT, SLVT, RVT, and HVT have been carefully studied.
    - Individual transistors curves taken, relatively large uncertainty.
    - Ring oscillators reviewed with models for TID performance. All indicate good theory predictions.
  - SRAM works well to much higher than 200 krad[Si] if all production settings are used as intended.
    - First bit cells are likely to have errors by around 250 krad[Si], but very few. And easily corrected with ECC.
  - 3rd party IP, which may depend on analog or mixed signal, or other sensitivity to small Vt shifts maybe fail around 150 krad[Si]. Evaluated IP that failed this way annealed, leaving questions regarding "nominal use" vs. worst case irradiation conditions.

- SEE – All tested circuits behaved as expected. Attempts to identify or evaluate circuits that should have better SEE performance limited.
  - Cross sections/onset LET for bit errors in SRAMs are as expected – which is good.
  - Stacked transistors and DICE cells expected to have better SEE performance, but this has eluded verification (likely test chip issues, but may indicate spatial proximity issues).

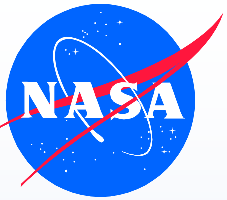
22FDX Test Chips/Plans



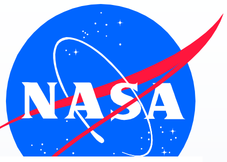
HPSC/Alphacore TC2

- GF test chips
  - Initial and continued transistor studies. Largely complete.
- Rufus & process monitor chips
  - Initial data on SRAM performance, but intended for process evaluation.
- HPSC TC2
  - Made by Alphacore Inc. Includes ring oscillators/gate chains, SET/FF test structures, SRAM.
  - Tested and have report. HPSC is working to release this information.
- ASIC Assurance TCB
  - JPL internal effort on 22FDX – currently working to expand certain efforts/test structure data, such as a comprehensive transistor TID dataset, and in-depth SRAM tests.
- ASIC Assurance TCC Plan
  - JPL is working on a follow-on chip to show effectiveness of 22FDX assurance approach.

22FDX Publication Plan



- 2022 IEEE Aerospace – two papers on ASIC Assurance and HPSC approaches.
- 2022 SEE/MAPLD – paper on HPSC's SRAM SEE evaluation.
- 2022 NEPP ETW – this meeting.
- 2022 NSREC – Two papers from ASU – transistor TID results, and back bias evaluation.
- 2022 RADECS – SRAM TID performance, multiple operating modes/etc.
- 2022 IEEE Electron Device Letters – Ring Oscillator/TID studies – including effectiveness of TID models for transistors.
- Open access publication planned for spreadsheet-type data release. Unknown timeframe.
- 2023 – intend to publish at: IEEE Aerospace, GOMACTech, SEE/MAPLD, NSREC, RADECS
  - Expect to have 2-4 additional academic partner papers on 22FDX publishing in the 2023-2024 timeframe.



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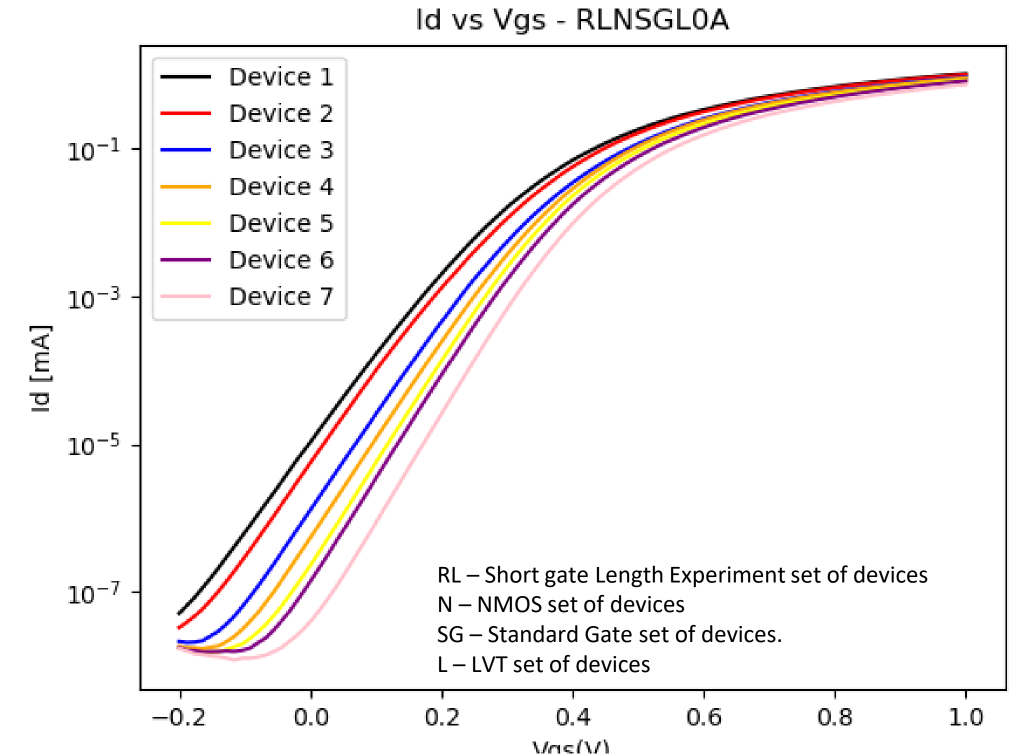
Transistor TID Data 1 of 2

- Transistor evaluation has been conducted using test chips from GlobalFoundries.
- Data indicate mostly parallel I-V curve shifts
- Testing to 300krad(Si)
- ARACOR dosimetry calibrated by Co60 testing performed at JPL
- This set of TID data at the transistor level will be important to the community as basis to modeling TID for the entire 22FDX technology and to compare TID data of test structures.



#	drawnW	drawnL	numFingers	total W	W/L	gate area
Units						
1	1.000	0.018	1	1.000	55.556	0.018
2	1.000	0.020	1	1.000	50.000	0.020
3	1.000	0.022	1	1.000	45.455	0.022
4	1.000	0.024	1	1.000	41.667	0.024
5	1.000	0.028	1	1.000	35.714	0.028
6	1.000	0.032	1	1.000	31.250	0.032
7	1.000	0.040	1	1.000	25.000	0.040

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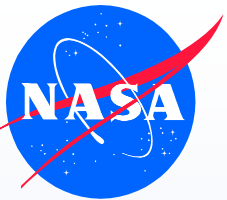
Transistor TID Data 2 of 2



- Transistor performance measured for various transistor types vs. dose.
- Device designs can take advantage of this information to achieve 200 krad[Si] performance with known circuit degradation.

NMOS_RVT_d1 (W/L = 0.08/0.02 um)

Vth=Vg @ Id=3e-7 A
Vds = 0.8 V
VB = 0 V

C4_"ON" state
C8_"OFF" state
C14_"TG" state

Threshold Voltage (V)
Total Ionizing Dose
0 krad, 50 krad, 100 krad, 300 krad

NMOS_SLVT_d1 (W/L = 0.08/0.02 um)

Vth=Vg @ Id=3e-7 A
Vds = 0.8 V
VB = 0 V

C4_"ON" state
C8_"OFF" state
C14_"TG" state

Threshold Voltage (V)
Total Ionizing Dose
0 krad, 50 krad, 100 krad, 300 krad

PMOS_RVT_d1 (W/L = 0.08/0.02 um)

Vth = Vg@Id = 3e-7 A
Vds = - 0.8 V
VB = 0 V

C4_"ON" state
C8_"OFF" state
C14_"TG" state

Threshold Voltage (V)
Total Ionizing Dose
0 krad, 50 krad, 100 krad, 300 krad, 600 krad

PMOS_SLVT_d1 (W/L = 0.08/0.02 um)

Vth = Vg@Id = 3e-7 A
Vds = - 0.8 V
VB = 0 V

C4_"ON" state
C8_"OFF" state
C14_"TG" state

Threshold Voltage (V)
Total Ionizing Dose
0 krad, 50 krad, 100 krad, 300 krad, 600 krad

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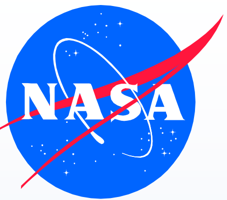
Gate Chain/RO TID Performance 1 of 2



GC Static Leakage Current vs. Dose

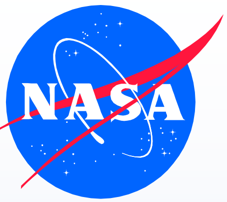
Current (A)

Dose (krad)

GC_1, GC_2, GC_3, GC_4, GC_5, GC_6, GC_7, GC_8, GC_9, GC_10, GC_11, GC_12, GC_13, GC_14, GC_15, GC_16, GC_17, GC_18, GC_19, GC_20, GC_21, GC_22, GC_23, GC_24, GC_25, GC_26, GC_27, GC_28, GC_29, GC_30

- Raw performance measured for 30 different gate chains.
- These data have been collected and analyzed to separate out the different structures and technology.
  - i.e. LVT, SLVT, RVT
  - NAND, NOR, etc.

Gate Chain/RO TID Performance 2 of 2



LVT_INV_20
LVT_INV_20_2X
LVT_NANDT2_20
LVT_NANDB2_20
LVT_NANDT3_20
LVT_NANDB3_20
LVT_NORT2_20
LVT_NORB2_20
LVT_NORT3_20
LVT_INV_28
LVT_INV_28_2X
LVT_INV_36
LVT_INV_36_2X

Relative leakage current change

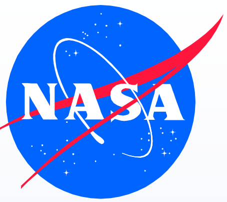
2100%
1900%
1700%
1500%
1300%
1100%
900%
700%
500%
300%
100%
-100%

0
End of Rad
3
30
60

Days of annealing

- Ring Oscillators made with many different gates.
- Tested for response to beyond 2x the target TID.
- Working out modeling details to predict behavior of arbitrary circuits.
- Minimal annealing observed. (Room temp.)

SRAM TID Performance



- Repeated earlier TID observations with process-monitor-like settings.
- Additional testing, using nominal design rules and operation for production SRAMs:
  - Very minimal (a few) bit failures by 200krad.
  - No significant increase up to 400krad.
  - Easily handled by typical EDAC.

0.6V All 0
0.6V Address
0.7V All 0
0.7V Address
0.8V All 0
0.8V Address

Failing Bits
100
10
1

0
50
100
150
200
250
300
350
400
450
Dose krad[Si]

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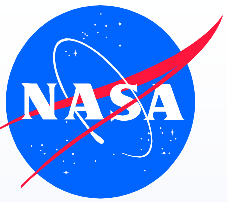

SRAM SEE Performance 1 of 3

- As expected
  - Match prior work with same SRAM cell by Casey (2020/2021)
- No difference between different data patterns

Bit Cross Section (cm²)
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
0 10 20 30 40 50 60 70
LET (MeV/mg/cm²)

All 0s Pattern

Bit Cross Section (cm²)
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
0 10 20 30 40 50 60 70
LET (MeV/mg/cm²)

Address Pattern

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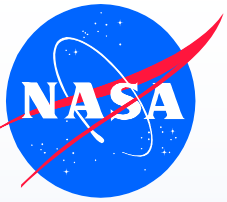
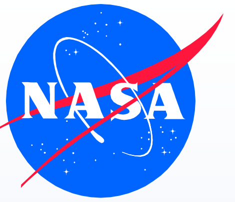
SRAM SEE Performance 2 of 3



- Address pattern
  - Nearly equal one and zero upsets over time
  - No evident WL error
    - Would have been at least 8 bits incorrect
    - Not perfect since patterns do repeat
- Data Details:
  - V (LET~11 MeV-cm^2/mg)
  - Running up to 7×10^7cm^{-2}
  - 0.8V
  - ~4×10^{-11}cm^2 (combined)



Upset bit map time lapse

- 15-minute beam exposure in 30s
- Video of capture to right
- These were analyzed for momentary error signatures
  - None seen
  - @LET 11, $\sigma<1\times10^{-8}cm^2/$

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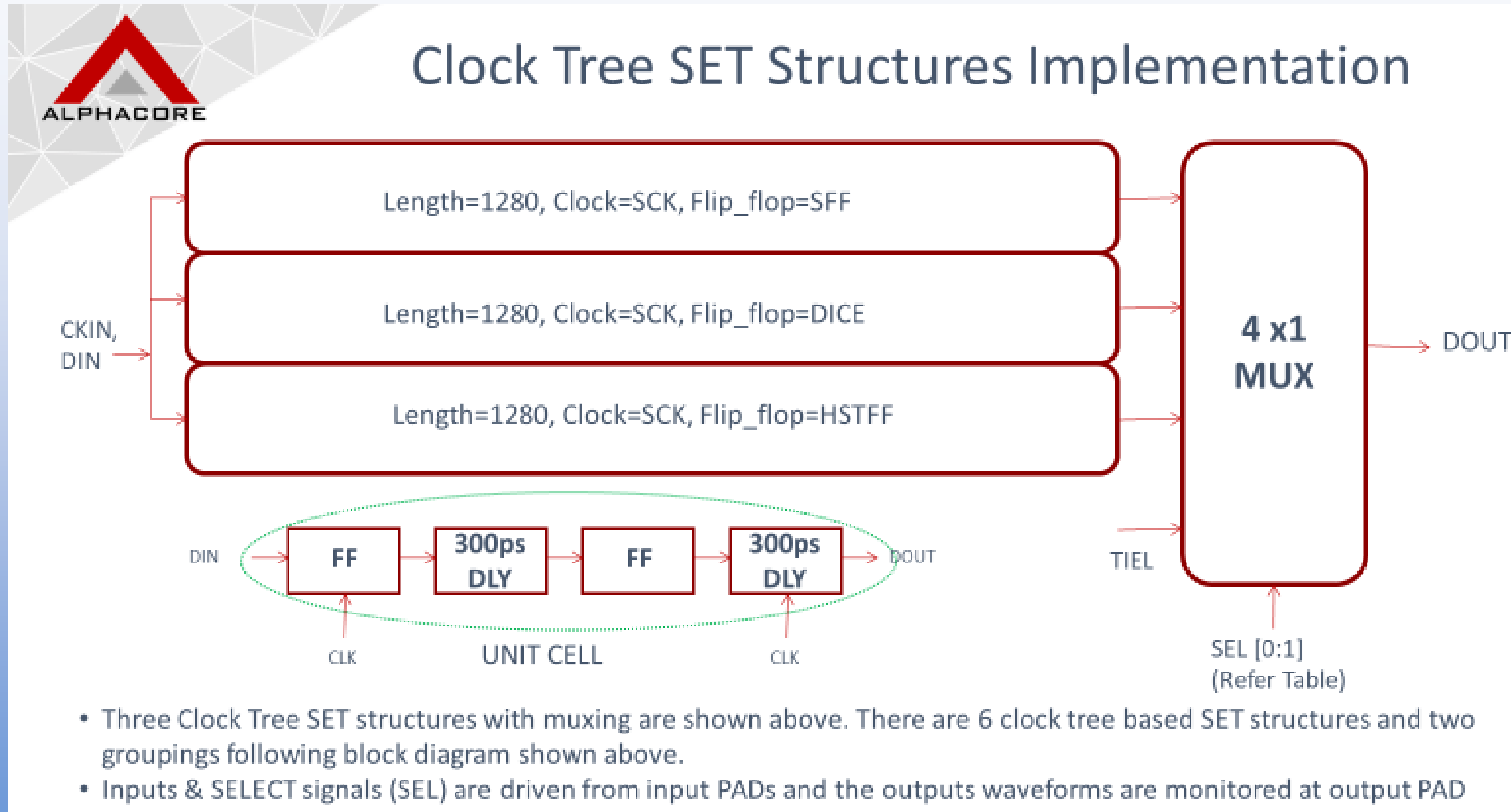
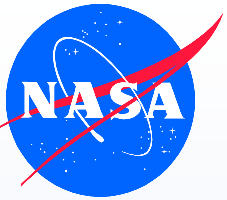
SET/SEU FF Performance 1 of 2

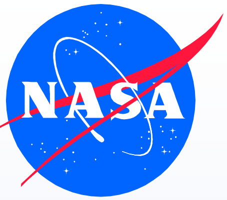


- SET structures were combinations of RH and non-RH Flip Flops and clock trees allowing comparison of RH vs. non-RH options.

SET/SEU FF Performance 2 of 2



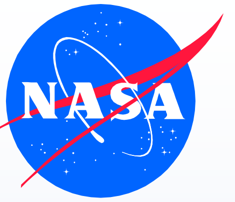
- Basic FF performance has been evaluated.
- Still working to extract RH vs. non-RH signal from FF and SET data.
- Unhardened FF SEE sensitivity is similar to expectation (plots being worked)
  - Issues with selector might be hiding results.
- It can't be understated how much exposure is required to get data from this structure while other items give results with much lower exposure.
  - 1×10^9/cm^2 vs. 1×10^7/cm^2 makes for very different exposures, and resulting localized TID risk. Especially at high LET.



Conclusion

- 22FDX is a viable technology/fabrication node for a majority of NASA missions.
  - >200 krad[Si] capable (higher is achievable, but there are some gotchas)
  - SEE performance is very good
  - Like all other nodes, it will require ECC/redundancy for critical SEE items
- HPSC has down-selected away from 22FDX for programmatic reasons.
  - Design for phase 2 will be in 12LP+, per vendor's preference
- HPSC and JPL's ASIC assurance program are closing out current 22FDX research and augmenting with additional JPL data
  - HPSC has a global publication plan for 22FDX with >6 planned or already delivered papers.
  - At least 3 additional papers (including RADECS and NSREC 2023) are expected on HPSC data being worked now.
- JPL's ASIC Assurance task will take additional data over the next year for JPL22TCB and the demo chip planned for FY23
  - We expect at least 4 more papers on 22FDX out of JPL's ASIC assurance effort.

Acknowledgement



Thanks to Megan Casey, and NASA support for 22FDX efforts.

Thanks to GlobalFoundries for support on SRAM macros and test chip development.

Thanks to LBL for heavy ion services in support of this work.