Modification of MIL-STD-883 TM1019 for rapid COTS path-to-flight

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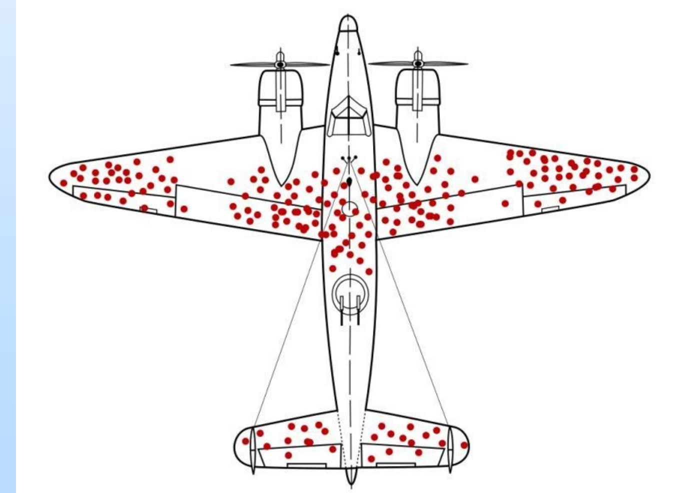
Classical WCA is cost prohibitive to smaller projects

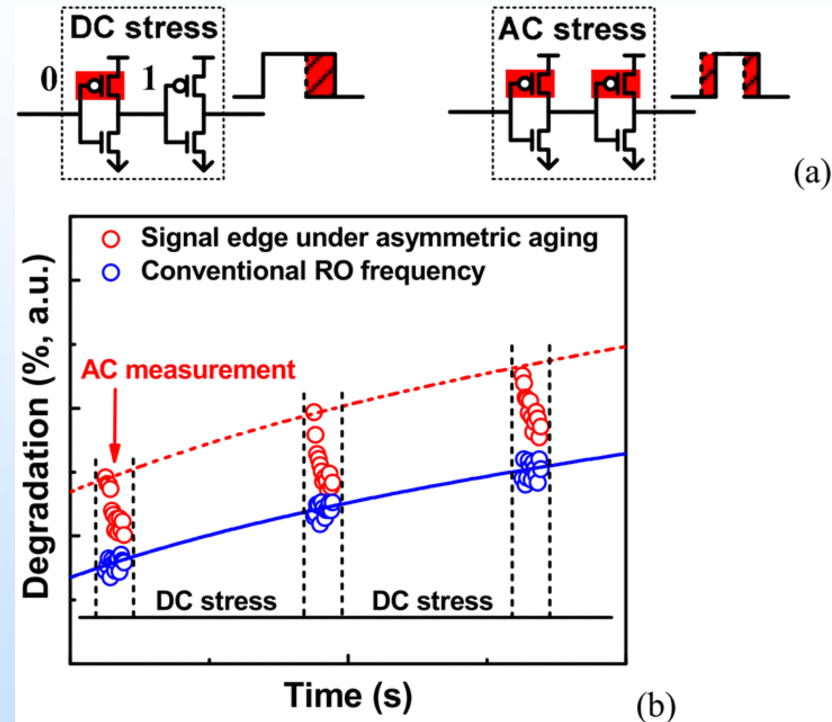
- Multiple steps
  - Raw data/report -> Application formatting -> Software macro for WCRDs -> 5x factor for non-RLAT WCRDs -> making PDF to send to Cog-Es of all parameters -> determining which parameters to ask Cog-Es for specific feedback
- SEE testing can scope to mission, why not TID?
  - Down select of circuit mode like SEL or SEFI
  - Loose guideline for process based on expansive historical data and engineer insight
- JPL has a deep bench for TID
  - Similar process can be developed using 1019 as baseline
  - Tailored plan based on known technology trends



Abraham Wald's Work on Aircraft Survivability, June 1984, Journal of the American Statistical Association 79(386):259-267

Plan

- Review historical data and test plans
- Review application of data to missions
  - WCBD et al
  - Aging and other failure modes can be leveraged
- Identification of serial vulnerabilities
  - Part, circuit and system
- Develop plan to test only critical parameters
- Demonstrate on known parameters of interest (POI)



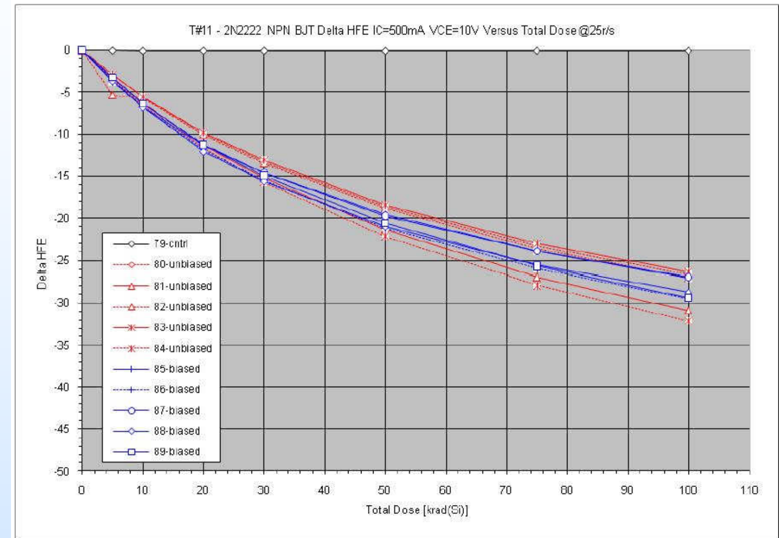
K. Sutaria, A. Ramkumar, R. Zhu and Y. Cao, "Where is the Achilles Heel under Circuit Aging," 2014 IEEE Computer Society Annual Symposium on VLSI, 2014, pp. 278-279, doi: 10.1109/ISVLSI.2014.106.

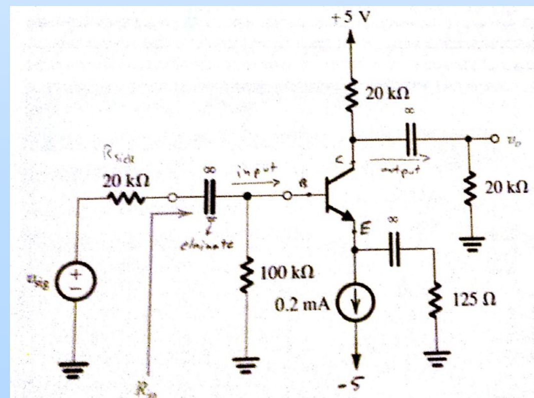
Current plan

- Compile all data on selected opamp/LREG/BJT.
- Identify high criticality parameters
- Define test plan for such
  - with infrastructure – quick test leveraged from available assets
  - without infrastructure - Eval cards come to mind.
- Case studies for guideline
- Develop a notional questionnaire to screen devices.
  - Can we mine RadFX for TRRs that triggered critical tests?

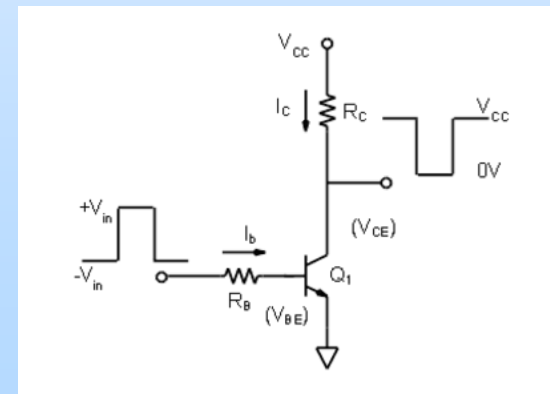
Chosen parts

- **OPAMPs**
  - **OP11, OP484, OP470, OP471**
  - **Well known part with a typical sensitivity – slew and Vos**
- **Linear regulators**
  - **LM137, LP2953, LM117**
  - **Industry wide application with recurring sensitivities – Vdropout, e.g.**
- **Bipolar junction transistors**
  - **2N2222, 2N2907, 2N3501**
  - **Easy lay-up for proof-of-concept**





VS



To be presented at he 13th Annual NASA Electronic Parts and Packaging (NEPP) Program's Electronics Technology Workshop (ETW), NASA GSFC, Greenbelt, MD.

Vulnerable Parameters - Bipolar Junction Transistors

JPL 10mR(Si)/S TO 100KRAD(Si)			RTS 10mr(Si)/s to 100krad(Si)			RTS 10mr(Si)/s to 100krad(Si)		
2N3501			2N2222			2N2907		
	biased	unbiased		biased	unbiased		biased	unbiased
HFE1 @ VCE=10V, IC=100uA	F	F	HFE1 @ VCE=10V, IC=100uA*	F	F	HFE1 @ VCE=10V, IC=100uA*	F	F
HFE2 @ VCE=10V, IC=1mA	F	F	HFE2 @ VCE=10V, IC=1mA	F	F	HFE2 @ VCE=10V, IC=1mA	F	F
HFE3 @ VCE=10V, IC=10mA	F	F	HFE3 @ VCE=10V, IC=10mA	F	F	HFE3 @ VCE=10V, IC=10mA	F	F
HFE4 @ VCE=10V, IC=50Ma	F	F	HFE4 @ VCE=10V, IC=150mA	F	F	HFE4 @ VCE=10V, IC=150mA	F	F
VCESAT1 @ IC=1mA, IB=.1mA	P	P	VCE(sat)1 @ IC=1mA, IB=0.1mA	P	P	VCE(sat)1 @ IC=1mA, IB=0.1mA	P	P
VCESAT2 @ IC=10mA, IB=1mA	P	P	VCE(sat)2 @ IC=10mA, IB=1mA	P	P	VCE(sat)2 @ IC=10mA, IB=1mA	P	P
VCESAT3 @ IC=150mA, IB=15mA	P	P	VBE(sat)1 @ IC=1mA, IB=0.1mA	P	P	VBE(sat)1 @ IC=1mA, IB=0.1mA	P	P
VBESAT @ IC=10mA, IB=1mA	P	P	VBE(sat)2 @ IC=10mA, IB=1mA	P	P	VBE(sat)2 @ IC=10mA, IB=1mA	P	P
VBSAT2 @ IC=50mA, IB=5mA	P	P						
Biased parts were slightly worse			Biased parts were slightly worse			Biased parts were slightly worse		
than unbiased.			than unbiased.			than unbiased.		

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Vulnerable parameters - Operational Amplifiers

JPL @ 10mR/s 100K		
OP11		
	biased	unbiased
VIO @ ±15V	P	F
IIO @ ±15V	F	F
IB+ @ ±15V	F	F
IB- @ ±15V	F	F
CMRR @ ±15V	F	F
AVO @ ±15V RL=2K	P	F
Unbiased were WC.		

JPL 10mR/s TO 50KRAD		
OP484		
	biased	unbiased
VOS @ ±15V	F*	F
IIO @ ±15V	F*	F
IB+ @ ±15V	F	F
IB - @ ±15V	F	F
CMRR @ ±15V	F*	F*
PSRR @ ±15V VS= ±2V > ±15V	F*	F*
AVS @ ±15V RL=2K VO=+/-10V	F*	F*
AVS @ ±15V RL=10K VO=+/-10V	F*	F*
Unbiased were WC.		
* 99/90 only		

JPL 10mR/S TO 50KRAD		
OP470		
	biased	unbiased
VOS @ ±15V	F*	F*
IIO @ ±15V	F*	F*
IB+ @ ±15V	F	F
IB- @ ±15V	F	F
CMRR @ ±15V VCM=+/-11V	F	F
AVS @ ±15V RL=2K	F*	F
AVS @ ±15V RL=10K	F	F
SR+ @ ±15V RL=2K	F*	F
SR- @ ±15V RL=2K	P	F*
PSRR VS=+/-2V > +/-15V	F* (CH 2)	F
Unbiased were WC.		
* 99/90 only		

RTS 10mR/S TO 100KRAD		
OP471		
	biased	unbiased
IB+ @ VS=+/-15V	F	F
IB- @ VS=+/-15V	F	F
AVO @ VS=+/-15V RL=10kΩ	F	F
CMRR @ VS=+/-15V, VCM=+/-11V	F*	F*
Unbiased were WC.		
* 99/90 only		

Vulnerable Parameters – Linear Regulators

JPL 10mR(Si)/s up to 15Krad(Si)			JPL 5mR(Si)/s TO 10.5KRAD(Si)			JPL 5mR(Si)/s TO 30KRAD(Si)		
LM137			LP2953 LDO Regulator			LM117 LDO Regulator	biased	unbiased
	biased	unbiased		biased	unbiased	Vref @ VD=5V IL=10mA	F	
VREF @ 10 mA (AL)	F	F	Vout @ Vin=6V	F	F	Vref VIN=5.50V IL=5.0mA, 500mA	F	
VREF VIN=-4.25V IL= 5mA	F	F	Vout @ VD=.3 thru 1V il=1Ma TO 200Ma	F	F	Vref VIN=30.00V IL=5.0mA, 72.7mA	F	
VR Line -4.25V to -30V	F	F	Dropout @ 1ma, 50mA, 100mA, 250mA	F	F	'VR Line Vdiff=3V to 28.75V	F	
Load Reg @ Vin=-6.25, IL=5mA to 500mA	F	F	Gnd Pin current @ 1ma, 50mA, 100mA, 250mA	F	F	'IADJ VIN=4.25V IL=5.0mA	F	
IBIAS VIN=-4.25V IL= 5mA	F	F	Vref @ 2.3V, 5V, 6V IL = 1mA thru 200mA	F	F	'IADJ VIN=4.25V IL=500.0mA	F	
IBIAS VIN=-6.25V IL= 5mA	F	F	Feedback Current	F	F	'IADJ vs Line	F	
Iadj Vin=4.25 V to 30V	F	F				'IADJ vx Load	F	
Iadj IL=5mA to 500mA	F	F				'Min Load VO=2.5V VIN=5.50V	F	
Min Load VIN=-4.25V	F	F				Vout VIN=5.00V IL= 25mA, 75mA	F	
Min Load VIN=-14.25V	F	F				Vout VIN=12.00V IL= 25mA, 75mA	F	
Min Load VIN=30V	F	F				Dropout IL= 5mA, 50mA, 100mA	F	
						Dropout IL=150mA, 200mA, 200mA, 250mA, 300mA	F	
LoadReg passes at lower current range or			The unbiased parts were more noticeable					
high Vin voltage and even lower current range			in terms of the degradation.					
The unbiased parts were more noticeable			Voltage and current levels played a part at what					
in terms of the degradation.			rad level they began to fail.					

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Identified vulnerable circuit and systems

Circuits

- High gain circuits
  - Used in instruments and communications
- Current monitoring
  - Sensitive to minor changes
- Low leakage circuits
  - Switches and power MOSFETs

Systems

- Instrumentation apps
  - Need precision
- Power modules and battery systems
  - Need precise current measurement and low leakage
- Radios and radars
  - Need high gain

Critical Paths and Readiness For Testing

- Convergent parameters for part, circuit and applications
- Assists in place can allow for quick turn testing
- Eval boards can extract parameters with minimal system engineering

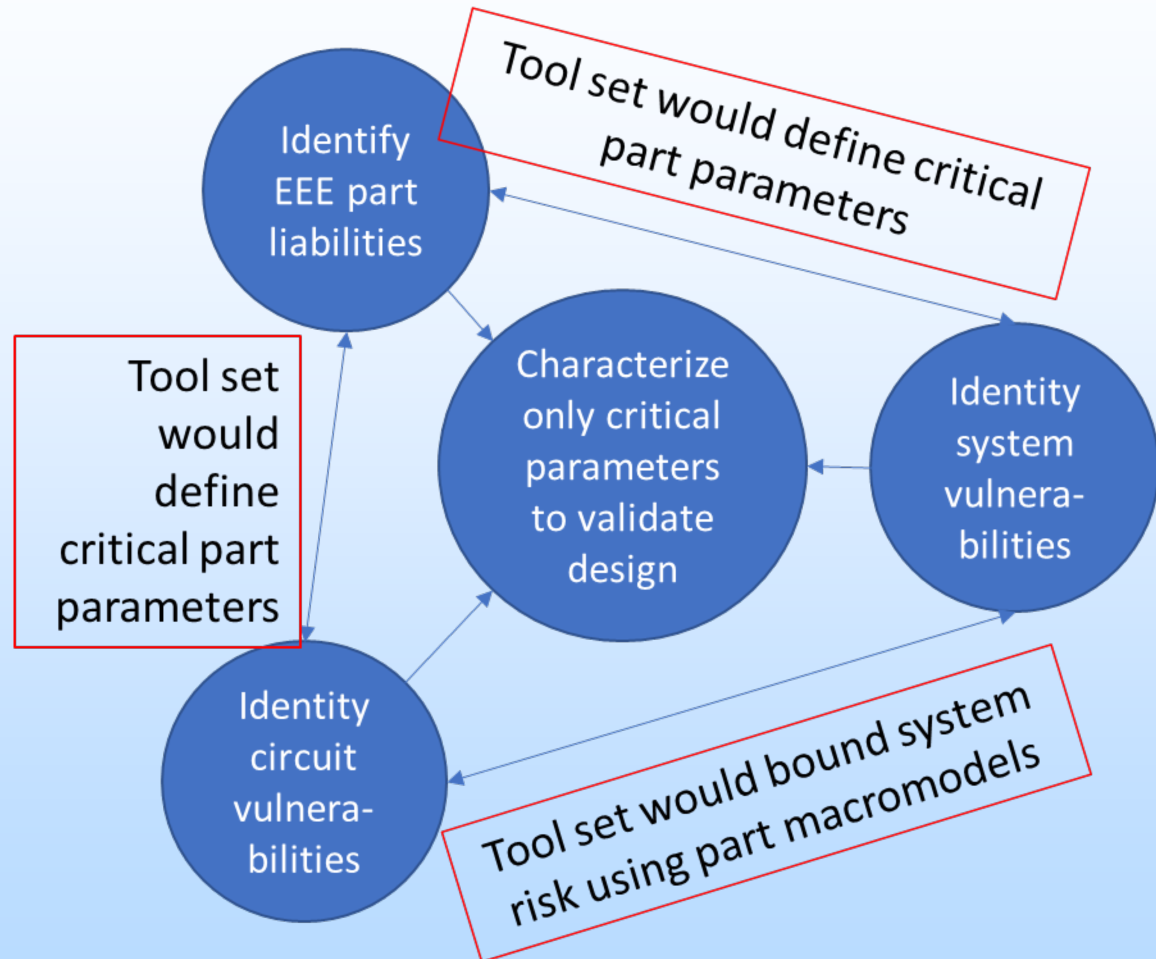
Worst Case Failures	CURRENT INFRASTRURE	WITHOUT CURRENT INFRASTRURE
Offset Voltage	LTS2020 W/2101 FB	Build Eval board w/feedback loop using
Offset Current	Unless part comes in odd	low noise Op-amps along with some
Input Bias current	package we should be fine	power supplies, DMMs, pico ammeters
Common Mode Rejection Ratio	with our existing hardware.	and scope.
Open Loop Gain		
	OpAmp	

WORST CASE FAILURES	Testing with Infrastructure	Testing without Infrastructure
HFE	Eagle 300, B1500, B1505, HP4256	Can be tested using the B1500 or B1505
		or the HP4256.
		If none of the above units are available
I would recommend testing		then we need 2 or 3 power supplies
the VCE(sat) parameter as well		several DMMs and a need to fab an
as the leakage parameters ex.	BJT	eval board, with sockets and a few
IEBO, ICBO		resistors

WC Parameters	Testing with Infrastructure		Testing without Infrastructure
VREF	Eagle 300		If the regulator is a 3 terminal device it can
Vout	LTS2020		be tested using the B1500, B1505 or the
IADJ			HP4256.
LINE REG			If the Regulator has multiple pins with
LOAD REG	LReg		various functions then we would require
Min Load			addition power supples, DMMs and a scope.
			A eval board would definitely need to be
			built.

Work to be done

- **Test plan and execution of only critical parameter**
  - **With and without infrastructure**
  - **Separate analysis of SE tools needed**
- **Cost and risk comparison**
  - **Including risk buydown “formula”**
- **Compare/contrast with other tools**
  - **SEAM (Systems Engineering and Assurance Modeling)**
  - **SPICE and derivatives**



Conclusion

- **Reduce test time and cost**
- **Increase use of COTS**
- **Develop IP for COTS fast track**

Comparing MEAN for Ib+
(Vcc = 5V, Vcm = 0V, OpAmp#2)

Input Bias Current (nA)

350
300
250
200
150
100
50
0

0 10 20 30 40 50 60

Total Dose (krad(Si))

LDR - Biased
LDR - Unbiased
HDR - B

BACK UP