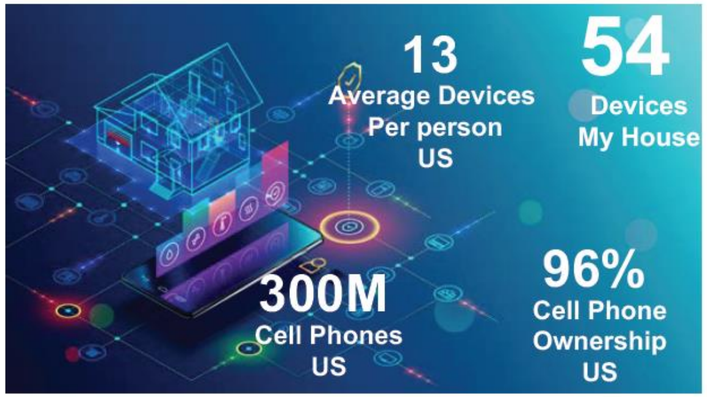

GlobalFoundries™
GF Foundry 101
June 16, 2022
Jeremy Muldavin

Outline

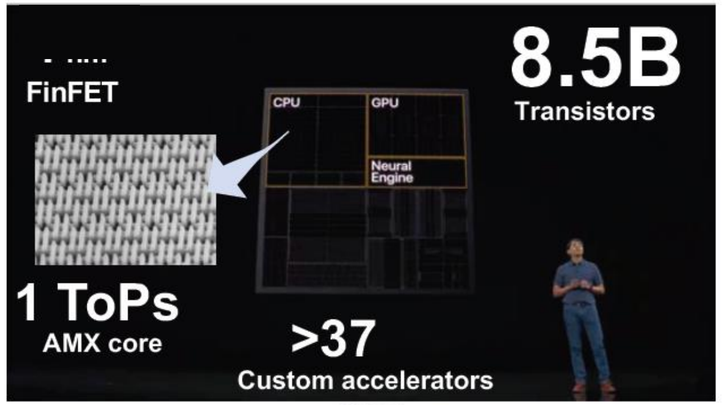
1. **Background**
2. **Foundry Overview**
3. **Customer Focus**
4. **Foundry Focus**
5. **Summary & Questions**

Background

We live in a world that is **connected**

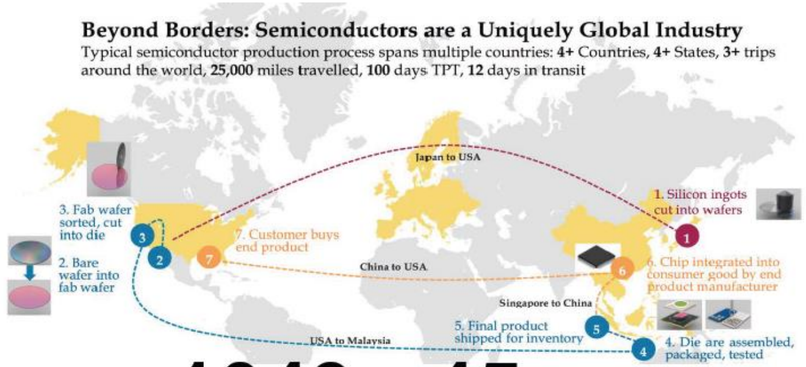


The technology we rely upon is **complex**



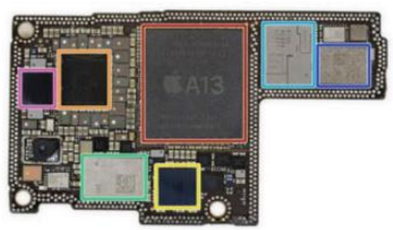
- Built-in GPS/GNSS
- Digital compass
- Wi-Fi
- Cellular
- iBeacon microlocation
- Accelerometers
- Temperature
- Ambient light, etc.
- Microphones

Technology supply is **distributed**

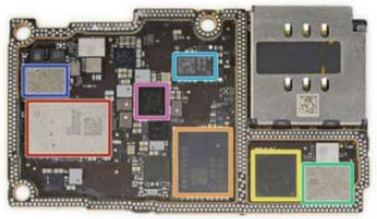


1049 Apple suppliers

45 countries



- Apple APL1W85 A13 Bionic SoC + SK Hynix LPDDR4X
- Apple APL1092 343S00355 PMIC
- Cirrus Logic 338S00509 audio codec
- Apple USI module—U1 ultra-wideband
- Avago 8100 Mid/High band PAMiD
- Skyworks 78221-17 low-band PAMiD
- STMicrolectronics STB601A0N power management IC



- Apple/USI 339S00648 WiFi/Bluetooth SoC
- Intel X927YD2Q modem
- Intel 5765 P10 A15 08B13 H1925 transceiver
- Skyworks 78223-17 PAM
- 81013 - Qorvo Envelope Tracking
- Skyworks 13797-19 DRx
- Intel 6840 P10 409 H1924 baseband PMIC

OUSD(RE) Muldavin 2019

Foundries are essential to global GDP

Market Size (2020)

$80.6T
Global GDP

$2T
Electronics

1,000s of companies

$466B
Semiconductors

+7.9%
CAGR growth (19-25)

100s of companies

$74B
Foundry[1]

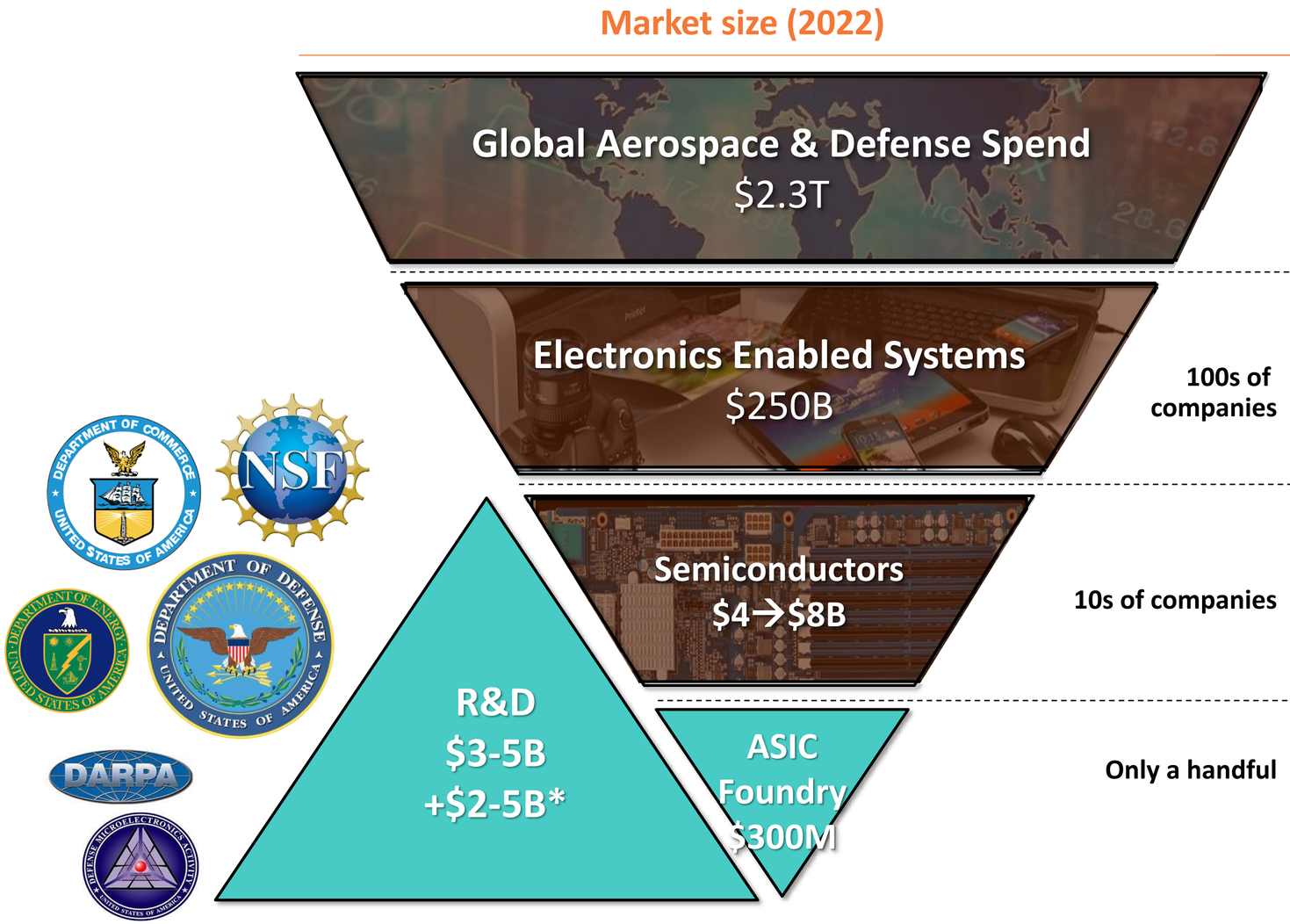
+10.1%
CAGR growth (19-25)[1]

Only 5 at scale[2]

Source: Derived from Gartner data. Gartner Forecast, Semiconductor Foundry Revenue Supply and Demand Worldwide 2Q21 Update, July 2021

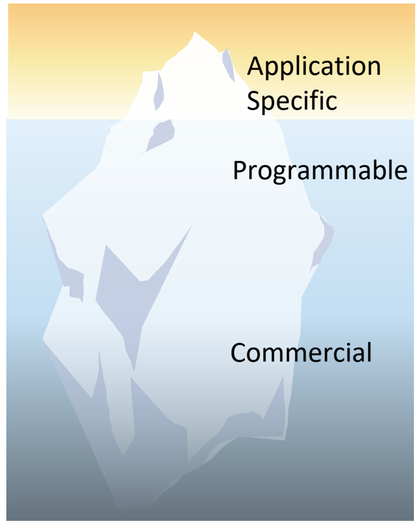
Notes:
(1) Excluding memory.
(2) Excludes smaller foundry players, defined as those with less than $2Bn of foundry revenue

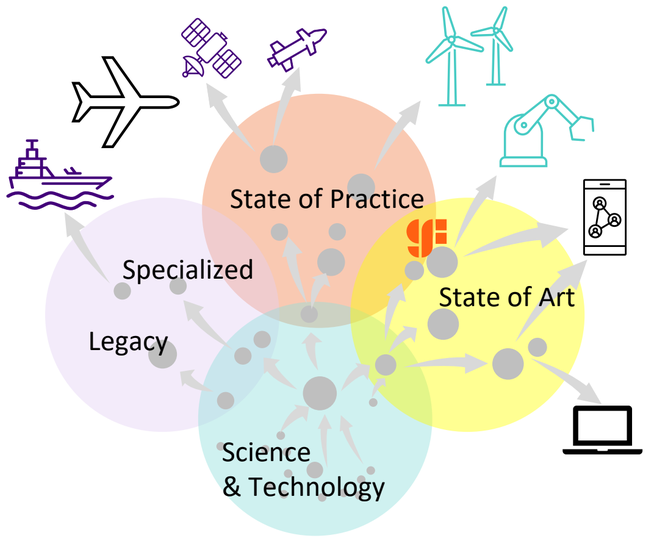
A handful of silicon foundries underpin the A&D semiconductor and electronics industry

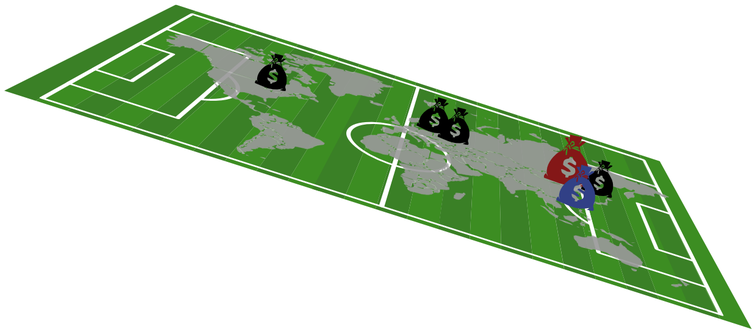


Source : Based on GF Internal Analysis

Our View of US Needs







Commercial Foundation

- **Advanced Technology** is needed across all production nodes for dual use
- GlobalFoundries is ideally suited to build an **onshore capability and capacity** to increase market share
- Commercial volume is necessary to sustain the IP, foundry, and packaging **ecosystem and requires market incentives**

Technology to Capability

- To address national interests R&D must enable **production in the US** for critical needs
- R&D must **leverage US foundry backbone** of production to capabilities for critical markets and national security
- Without the laws and **incentives to capture R&D in the US** our adversaries will be the first to benefit

Un-Level Playing Field

- Cost of building, equipment, labor, and development are being **subsidized heavily by Asia and Europe**
- USG has a chance to **change where R&D is ramped to production**
- The USG must have agile and potent tools to **incentivize domestic R&D capture** and transition to production in with **strong market preferences**

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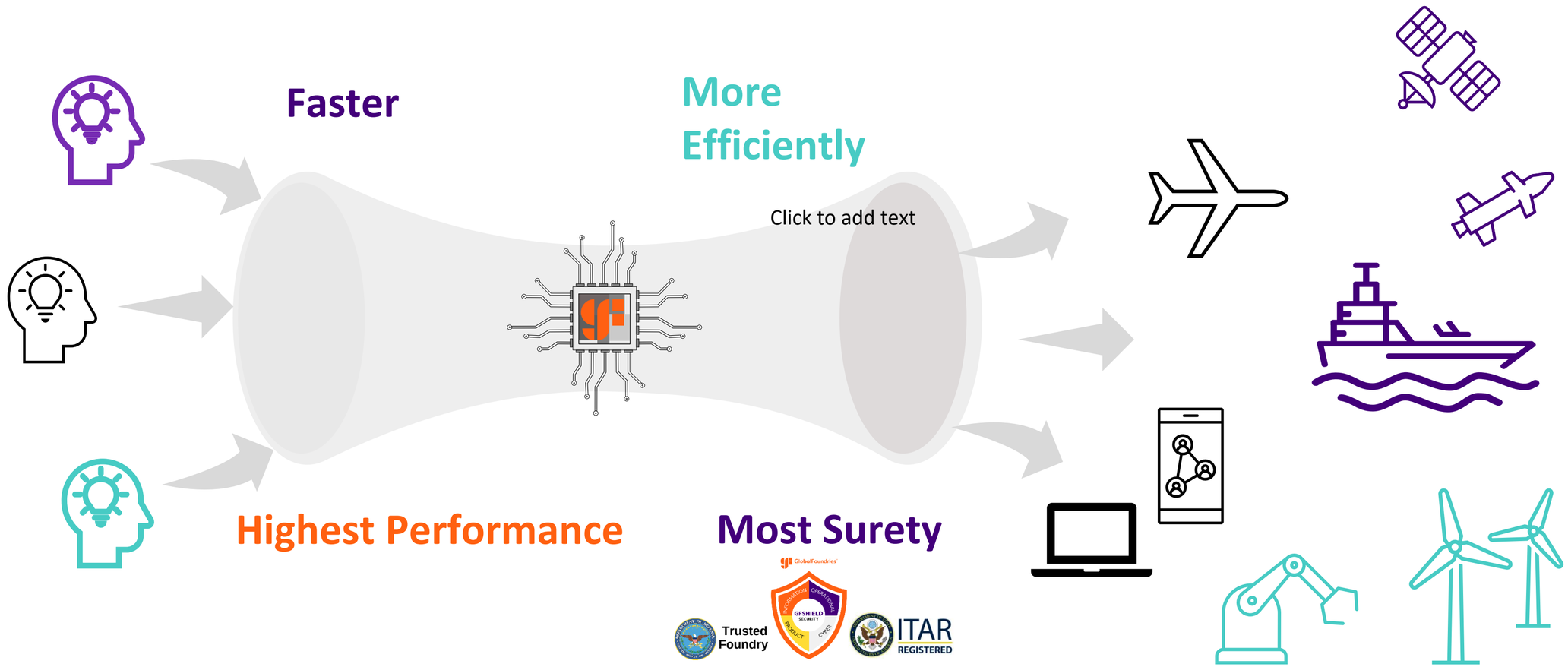
Ideas to Capabilities

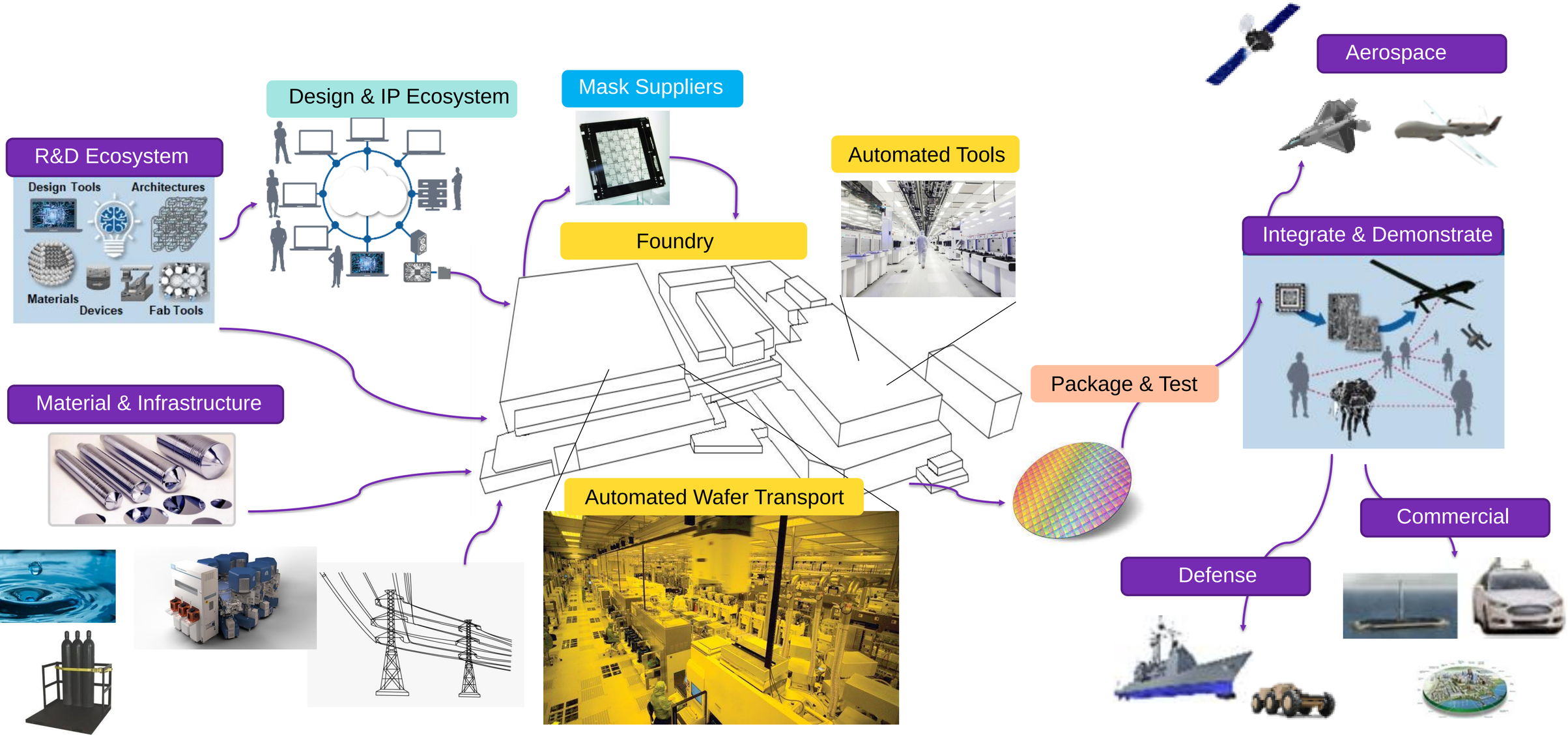
Foundry is the critical core and enabler for rapid innovation

Design → Release → Mask Fab → Wafer fab → Post Fab



Foundry Ecosystem

Design → Release → Mask Fab → Wafer fab → Post Fab



Sourced from across the internet

Foundries Deliver Capabilities

Offer to Customer

- **Variety of Advanced Technology**
- Device & Chip **Performance and reliability data** and **IP Ecosystem**
- **Rules for Design** and construction of Chips (PDK)
- **Time until 1st Product** in hand when designs received
- **Cost and Speed** of Production
- **Support** for design in our technology

Designs to Masks

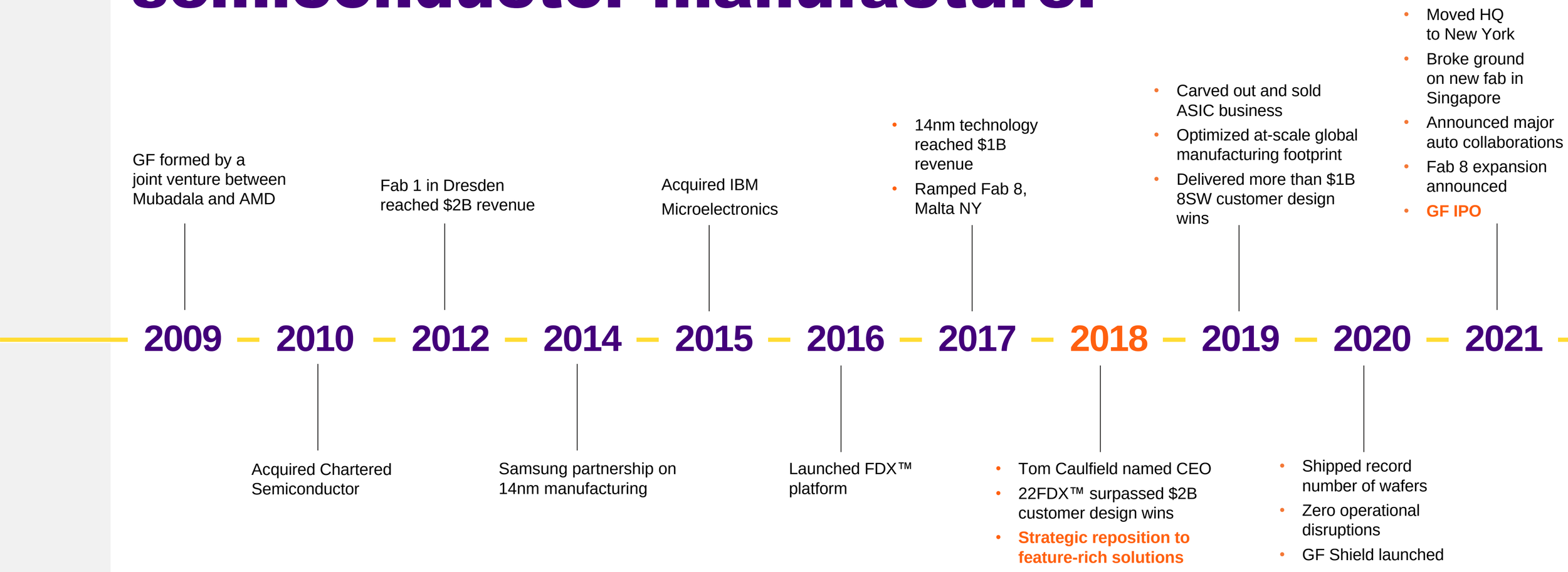
- **Receive and validate** customer designs
- **Confirm it meets Design Rules** for manufacturing
- **Refine shapes** to match our tooling (OPC)
- **Make the Masks** (chrome lines on glass) or send validated data to mask house

Masks to Wafers

- **Receive Maskset** from mask house
- **Identify materials** and **process steps**
- **Do Processing** Steps as outlined in the PDK (litho, etch, clean…)
- **Do Inspection** Steps to ensure yield and performance
- **Finish wafer processing and test** to validate yield and performance
- **Slice wafers into Die,** and **package** for sale / mounting to circuit boards

GlobalFoundries™

The making of a global semiconductor manufacturer



Global Manufacturing Footprint

Malta, NY, USA
Fab 8

Wafer size: 300mm
Capacity: 570 kwpa[1]
Technology: FinFET, NVM, RF SOI, SiPh

~3,000 employees

Malta, NY, USA
Fab 8.2- New Fab 2025

Wafer Size: 300mm
Capacity: 590 kwpa
Technology: FDX™, HV

~1,000 employees

Burlington, VT, USA
Fab 9

Wafer size: 200mm
Capacity: 620 kwpa
Technology: RF SOI, SiGe

~2,200 employees

~15,000 employees

>200 customers

2021 IPO

Singapore
Fab 7 / GIGA+

Wafer size: 300 & 200mm
Capacity: 720 & 720 kwpa
Technology: BCD/BCDLite®, HV, NVM, DDI, RF SOI, LP SiGe

~4,000 employees

Singapore
Fab 7h- New Fab 2023

Wafer size: 300mm
Capacity: 450 kwpa
Technology: BCD/BCDLite®, NVM, DDI, RF SOI

~ 800 employees

Dresden, Germany
Fab 1

Wafer size: 300mm
Capacity: 850 kwpa
Technology: FDX™, NVM, HV, BCDLite®

~3,000 employees

Notes:
*In Process
(1) Kwpa is defined as at-four-walls thousand wafers per annum..

How we innovate: market-centric approach to technology solutions

Market requirements

Smart Mobile Devices

Personal Computing

Communications Infrastructure & Datacenter

Home and Industrial IoT

Automotive

Technology requirements

Device performance

Power efficiency

Low latency

RF connectivity

Security elements

Reliability

Application-enabling IP

Extreme environments

GF Technology solutions

Platform

Transistor targets, ULP

Operating voltage

Features

RF & mmWave

Embedded memory

Automotive grade

BCD, HV

IP / Enablement

Foundation IP

Complex / application IP

PDK

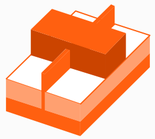
Differentiated technology platforms

Feature-Rich CMOS
Complementary Metal-Oxide Semiconductor

Mixed-Technologies for Power Management, High-Voltage, Embedded Memory

>3 billion high-end audio amp units (BCDLite) shipped

>150K DDIC wafers shipped



FinFET
Fin Field-Effect Transistor

High Performance, Power Efficient "Systems-on-a-Chip"

Scarce capacity – GF one of three foundries and adding unique features

FDX™
Fully-Depleted SOI

Enabling New High-Performance, Low-Power Applications

Supports two of top three 5G mmWave FEM design companies

RF SOI
RF Silicon-on-Insulator

Low Power/Low Noise/Low Latency/High Frequencies

1st fully qualified high-volume RF SOI Foundry solution on 300mm wafers

SiGe
Silicon Germanium

Power Amplifier and Very High Frequency Applications

Highest fmax SiGe BiCMOS foundry process in volume production at 400GHz with roadmap to 1THz

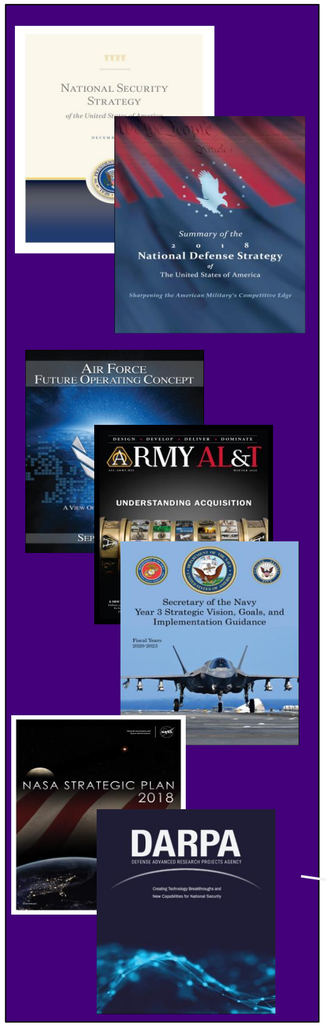
SiPh
Silicon Photonics

Higher Data Rates with Greater Power Efficiency

5-10x better power efficiency than long range electrical interconnect

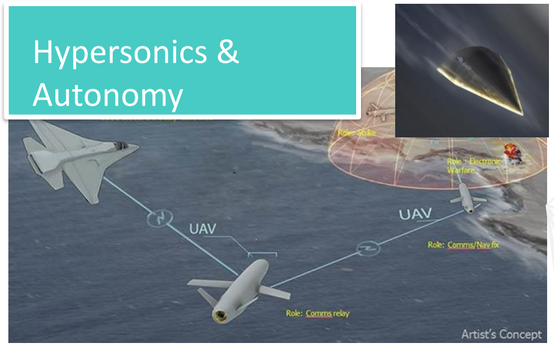
Strategic Market Analysis Flow (DoD)

Inputs

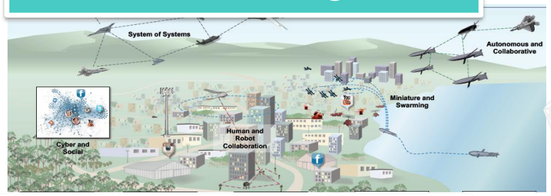


System Needs

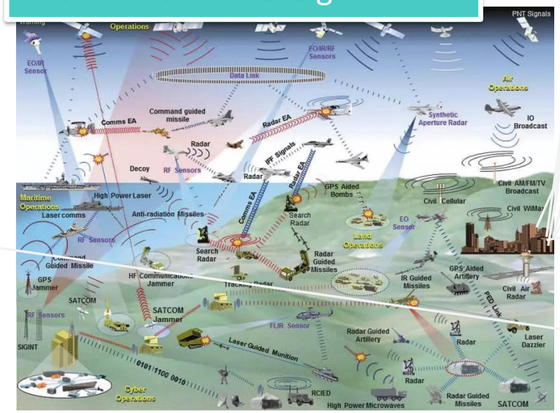
Hypersonics & Autonomy



Robust Comms & Edge AI



Networked EW & SigInt



Enabling Capabilities

- Harsh Environment/ Space & Rad-Hard
- RADAR and DE
- Wideband Comm/ Sigint/EW
- Multi-spectral Imagers/AI
- Edge AI/ FD-PED
- Global PNT
- High-perf. Compute + Quantum
- Trusted Fab & Packaging
- R&D Capture and Prototyping

GF Platforms

- 22-12FDx
- 45nm RF/CLO/SO
- 12LP+
- GaN on Si +CMOS
- Ge & BSI Platform
- Rad-Hard Platform
- eNVM Platform
- Cryo/Quantum Platform
- 3D dense stacking for AI & Imagers
- Post-fab Packaging

Targeted Development

- HPSC RH SoC
- Edge AI SoC
- GPS SoC
- RH/eNVM SoC (NASA\DoD\NSWC)
- Phased Array Platform (DARPA)
- Cryo Compute
- Smart Imaging Platform

GF offers a “Foundation of Trust” to build sustainable partnerships

Beneficial geopolitical landscape

During times of increasing international trade conflicts, GF benefits from the resilience of global scale of operations in stable low-risk geographies (United States, Germany and Singapore)

Pedigree of secure at-scale manufacturing

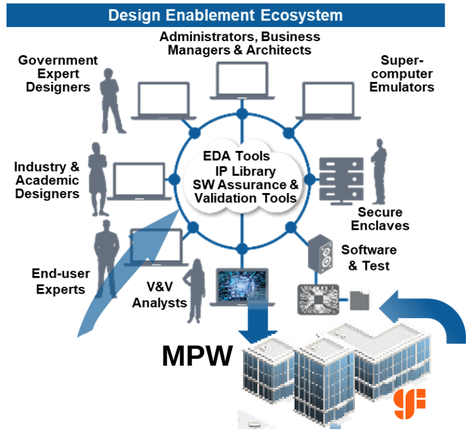
1. Only pure-play foundry in The United States Department of Defense Trusted Foundry Program
2. ISO 15408 Certification to manufacture Common Criteria Secure Products
3. ISO 27001 Certification for Information Security Management

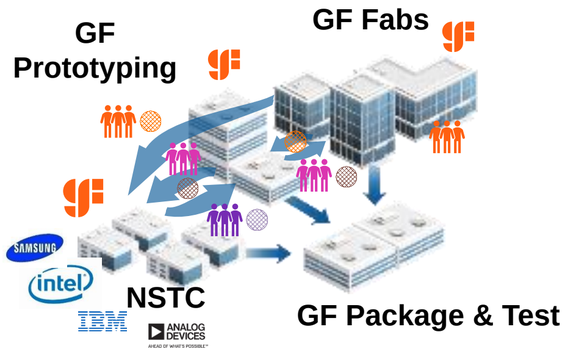
Intellectual Property (IP) protection

With an industry-leading track record protecting GF IP and customers' IP

In a world of escalating threats and risks in the technology sector, our “Foundation of Trust” offers a strong competitive edge

GF Delivers





Design Innovation

- Design environment with IP, EDA, Compute, PDK, emulation
- MPW guaranteed access and enablement
- Early access to developing platforms

Prototype Innovation

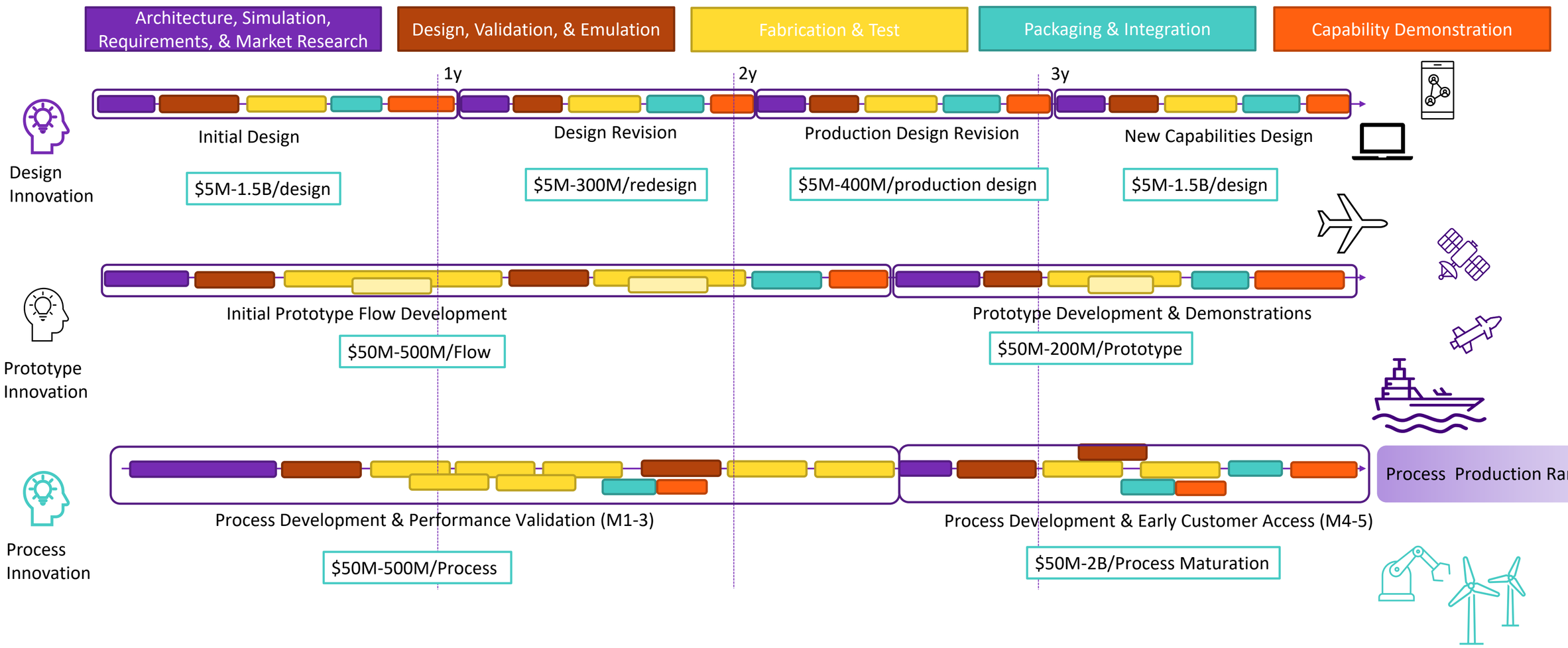
- Partial-flow wafers for external additions
- Split-flows to allow insertion of steps into production process
- Packaging enablement for 2.5-3D integration

Process Innovation

- Early access and embedded workforce to shape dual-use commercial platforms
- Process options built upon the production baseline for prototyping differentiation
- Alignment of USG R&D roadmaps with market needs and transition

Innovation Timelines

Ideas to Capabilities



Only Process innovation delivers new production capabilities requires significant investments

IMTR: Integrated Market-Technology Roadmap

Applications

Feature-Rich CMOS	FinFET	FDX™	RFSOI	SiPh	SiGe	GaN
Power	APU	SoC	RF FEM Sub 8GHz	Optical TRX	Wi-Fi	Fast Charging
Imaging & Display	Compute	Wireless	Ground station receiver	Optical C2C	RF Transceiver	EV / Power Conversion
MCU	RF Transceiver	RADAR	RF FEM mmWave	LIDAR	ReDriver	Infrastructure / Wi-Fi
Audio/ Haptics	MCU/DCU	Sensing	Cellular Transceiver	In Vehicle Networks	Cellular Transceiver	RF FEM Sub 8GHz
Battery mgmt	Chipset	Sat Comm.	Smart home devices	Photonic compute	Auto Radar	RF FEM mmWave

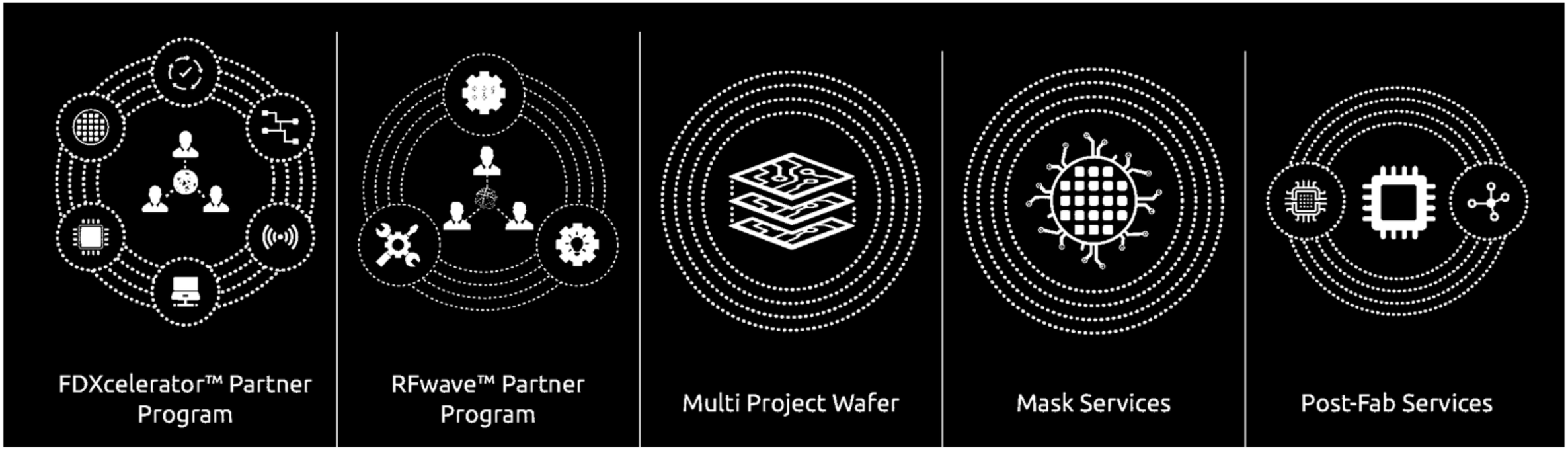
Platforms

Feature-Rich CMOS · FinFET · FDX™ · RFSOI · SiPh · SiGe · GaN

Operating model

>30	>1500	~$700m p.a.	>30K p.a.	>150
Universities, government partners and other research institutes partnered in collaborative efforts	Technologists in dedicated research team	$506m R&D NET opex & $186m NET capex in platform extensions, feature expansions and IP	Wafers per year dedicated to development	Differentiated programs built on world class platforms

Active enablement and Access programs



- Partnerships to promote and facilitate FDX adoption and R&D
- 50 service partners
- Broad IP portfolio tuned to FDX
- MPW service to lower cost and risk of production

- Partnerships to promote RF design and enablement
- >50 service partners
- Specialized RF validated IP portfolio
- MPW offerings

- MPW for early access, entrepreneurs, DIB, and academic partners
- DMEA TAPO MPW shuttles
- Commercial MPW shuttle
- Academic Partner shuttles

- Mask prep and production onshore and offshore
- Mask prep services to 12nm
- Mask Production Partnership onshore
- Global Mask flow for commercial

- Post-fab services and partnerships with OSATs
- OSAT partnerships
- Specialized packaging and test
- RF test for volume
- DMEA Trusted packaging partnerships

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Design Innovation: Ideas to Logic

System Design

Define Problem | Design & Simulate

Chip Fabrication

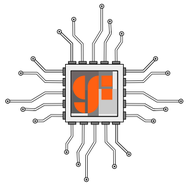
Mask Build | Fabricate

Provision and Test

Test | Firmware & Software

Algorithm

Logic (10110..)



Physical Circuit

Firmware & Software

Sense, Logic, Actuation

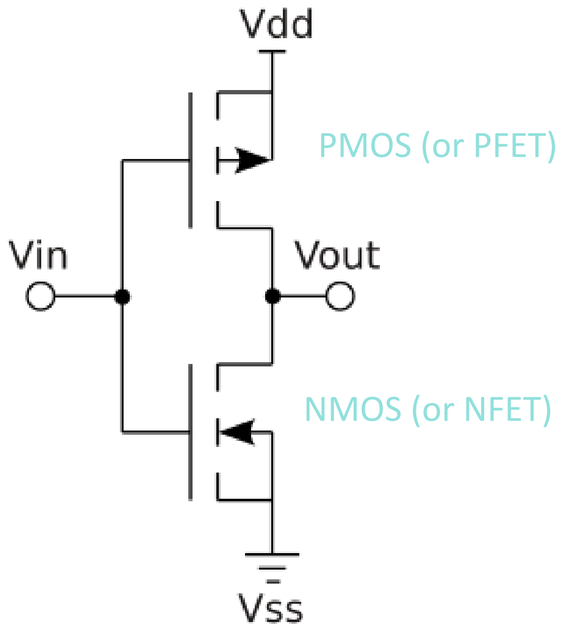
Logic 101

What is a Transistor?

A device used to create logic and analog circuits

- Logic circuits operate on 1's and 0's
  - 1 is a logic "high", or VDD (power supply voltage)
  - 0 is a logic "low", or GND (power supply ground)
- Inverter example:

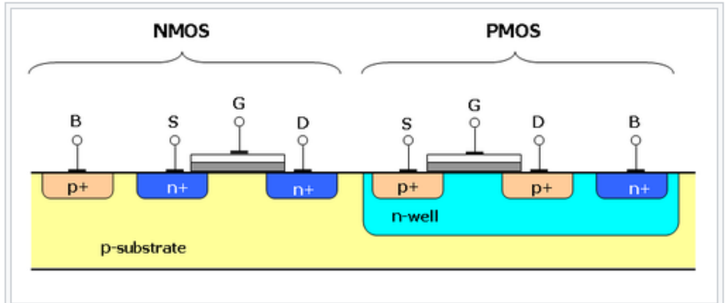
Schematic for an Inverter



Inverter Truth Table

In	Out
0	1
1	0

Device Cross Section (no wiring shown)



Cross section of two transistors in a CMOS gate, in an N-well CMOS process

https://en.wikipedia.org/wiki/MOSFET

Logic Devices

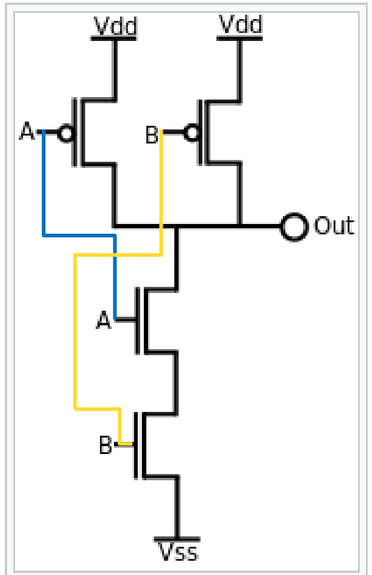
Design → Release → Mask Fab → Wafer fab → Post Fab

Simple Logic Device (NAND)

NAND Truth Table

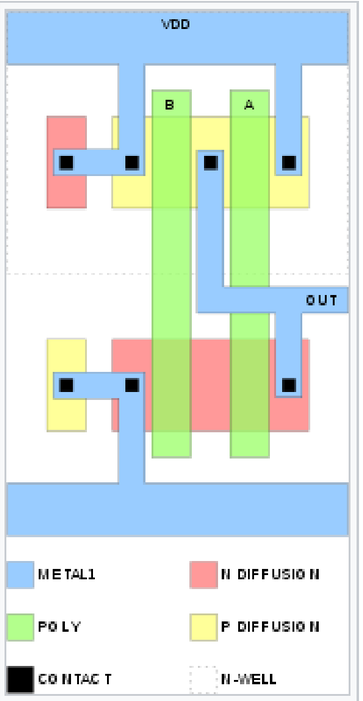
A	B	Out
0	0	0
0	1	0
1	0	0
1	1	1

Schematic



NAND gate in CMOS logic

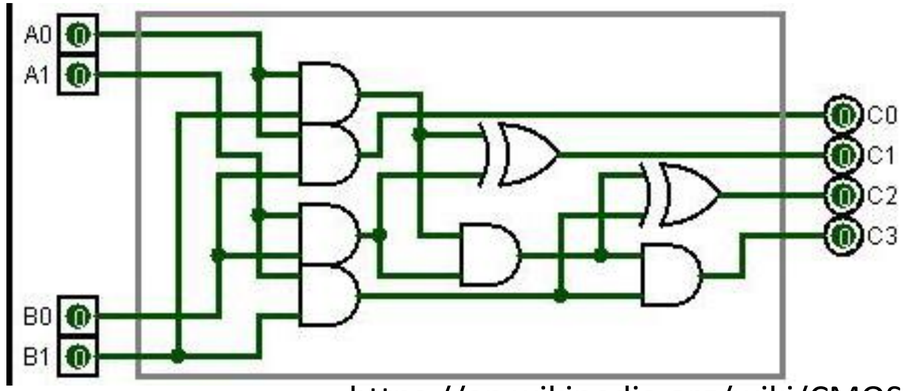
Layout



The physical layout of a NAND circuit. The larger regions of N-type diffusion and P-type diffusion are part of the transistors. The two smaller regions on the left are taps to prevent latchup.

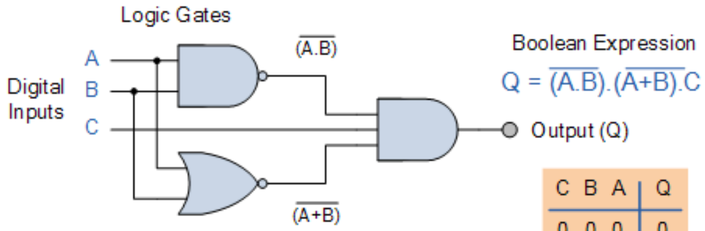
Combine Logic Elements to Arbitrary Circuit

2 Bit Multiply



https://en.wikipedia.org/wiki/CMOS

Arbitrary Logic Function



Logic Diagram

Typical Truth Table

C	B	A	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

IC Design 101

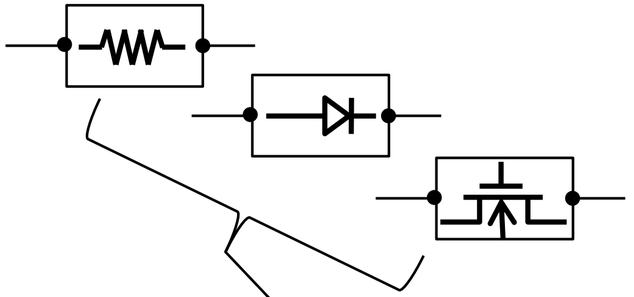
Enable Design for Fabrication

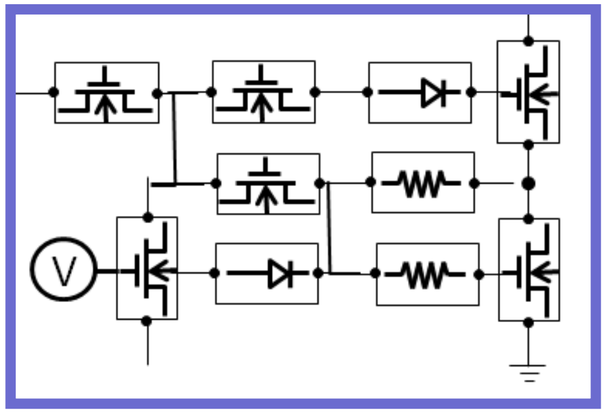
Design → Release → Mask Fab → Wafer fab → Post Fab

Thousands of electrical elements

How does Shape affect output?
How does Voltage affect output?
How does Temperature affect output?

Characterization and Modeling Engineer





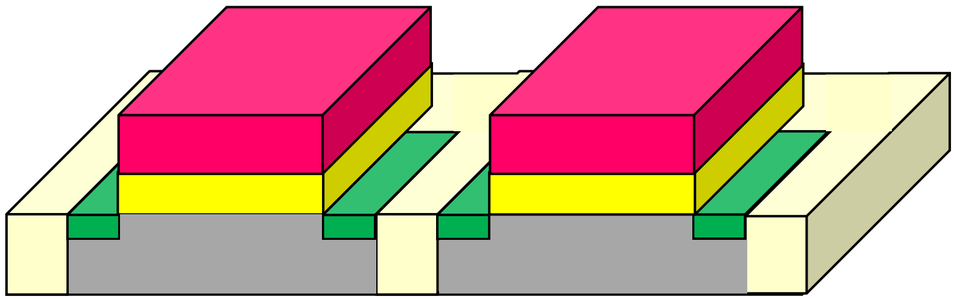
Compact Model published in PDK*

Customer uses the model for designing products

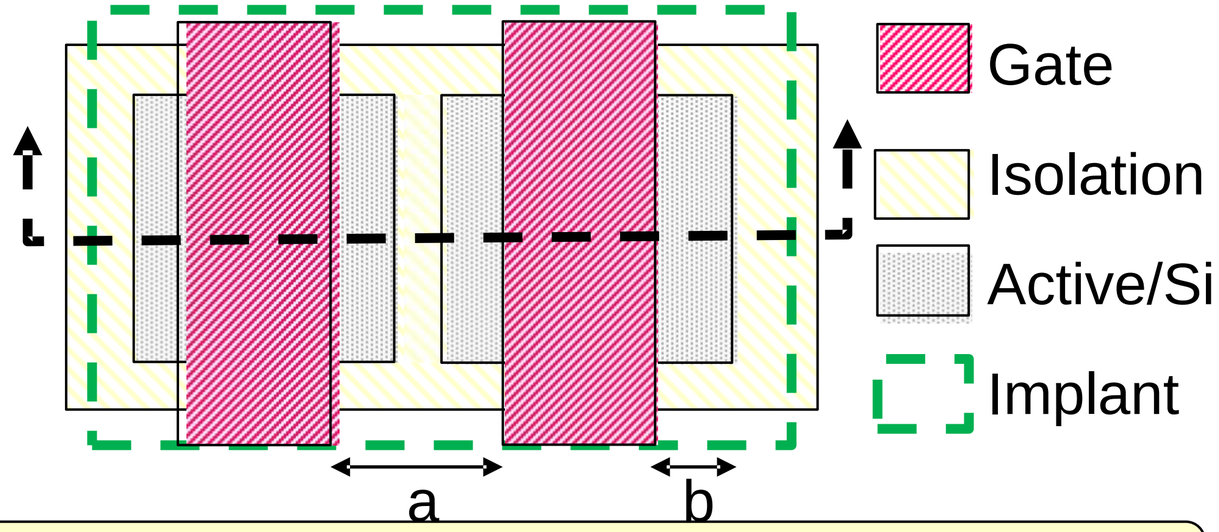
Foundry looks good when:
a) “On” currents are high
b) “Off” currents (leakages) are low
c) Switching is fast
d) Variations w/ temp are low

Enable Design (PDK example)

Cross-Section



Top-Down / Layout

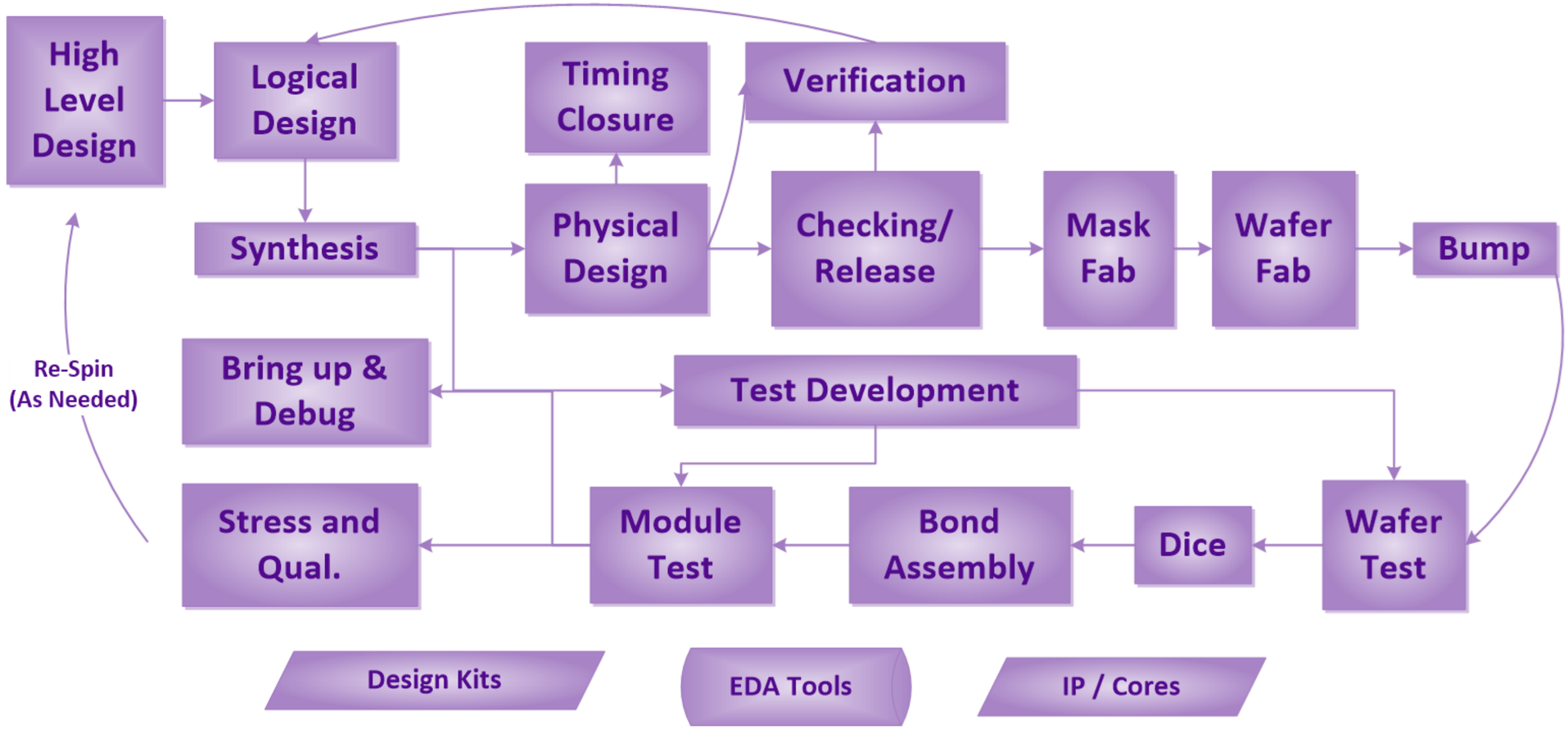


Here is what we'd see in a 'Design Manual'

a) 14nm Technology, Ground Rule #468: "2 Gates must be no closer together than xx nm."
b) 14nm Technology, Ground Rule #812: "Distance from Gate to Isolation must be no larger than yy nm."

Design → Release → Mask Fab → Wafer fab → Post Fab

Typical IC Development Activities

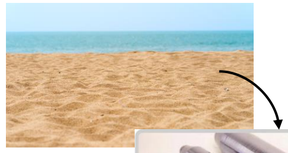


Outline

1. Background
2. Foundry Overview
3. Customer Focus
4. Foundry Focus
5. Summary & Questions

Building Chip Levels

Lifecycle – Sand to Electron Logic Overview



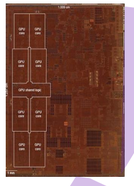
Silicon

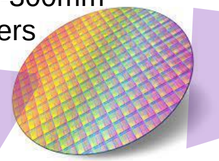
Foundry

Fabrication tools

~400 chips/wafer

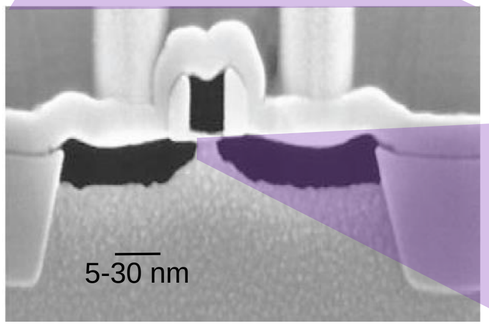
200-300mm wafers





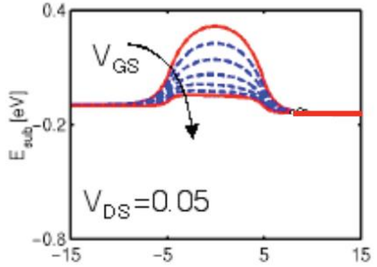
10B Transistors/chip

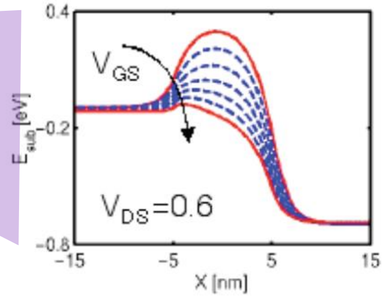
S G D



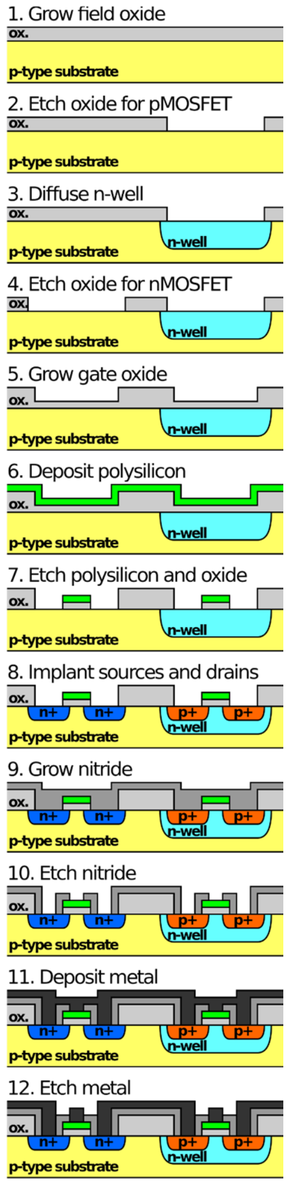
CMOS Transistor Cross section

Potential Energy of electron

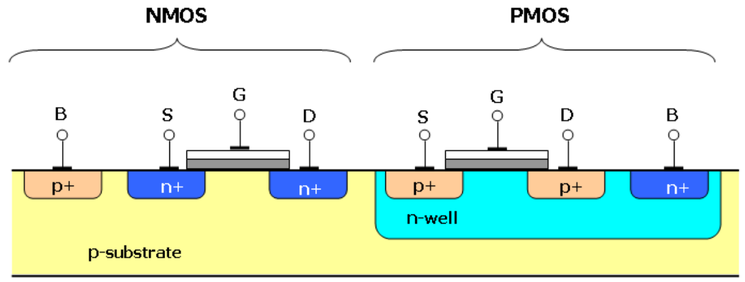


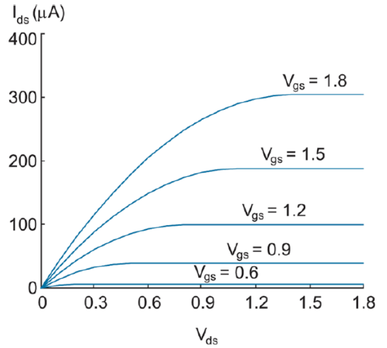


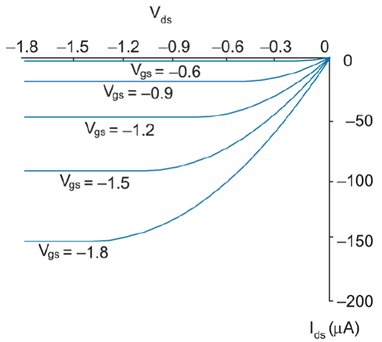
Fabrication Process



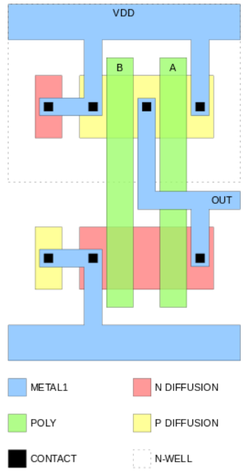
Transistor to Processor Overview

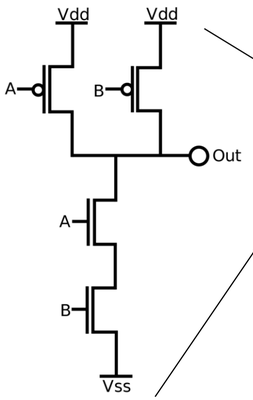




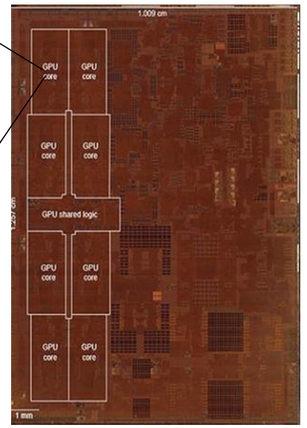


Layout and Schematic of NAND Device





Product Chips



Sourced from across the internet

Mask and Wafer Fab Described

Design → Release → Mask Fab → Wafer fab → Post Fab

Checking
- Verifies that physical shapes for each level comply with design rules

Kerf Merge
- Addition of design agnostic structures for manufacturing alignment and control
- Such standard Kerf structures are placed in the “interstitial” space between customer die.

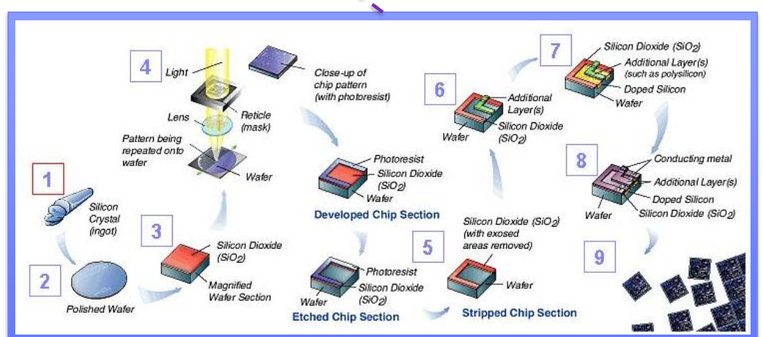
Data Prep
- Compensations applied to physical shapes, to counter exposure & wafer fab processing causal effects, to result in on wafer structures that match the design

Masks are fabricated individually
- Depending upon the design and technology, 21 to 73 mask levels are uniquely fabricated for each customer program (such mask sets are built once and re-used in manufacturing for that program)

Fracturing
- Breaks the physical design shapes into primitive shapes the mask write tools can handle

Mask Write
- Light beam exposure tools write the shapes on a photoresist layer
- Etching is performed to create the shapes in chrome on glass

Inspection
- Each mask is optically inspected to verify the written shapes match the incoming data and are defect free



http://www.semiwiki.com/forum/showwiki.php?title=Semi%20Wiki:Semiconductor%20Fab%20Wiki

Wafer Fabrication
- Industry standard semiconductor tools, with processes and recipes, are utilized to build each customer program
- Each “mask set” is specific to a customer’s program

Kerf Test
- Standard Interstitial kerf structures are tested at Metal 1, and again at Last Metal, to determine if each wafer is within manufacturing specifications

What is a Mask?

End Customer: "I want a chip which can do xxx"

Designer : "OK, I'll connect the 100,000,000 devices in this manner."

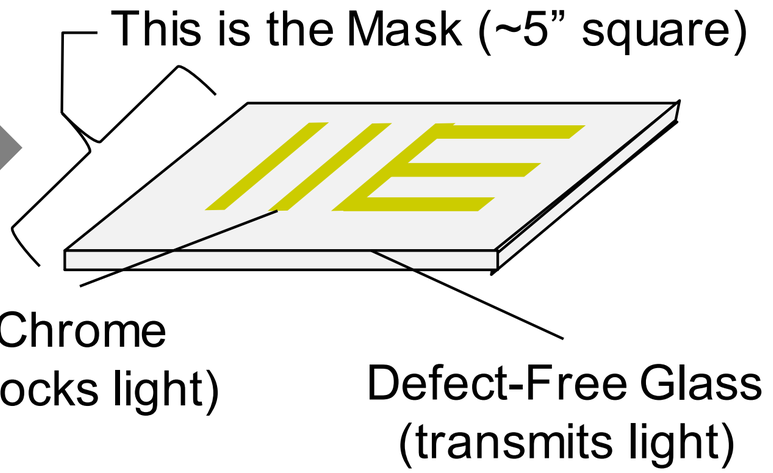
Foundry (GF): "You must not violate these rules (how close to put devices, etc.)"

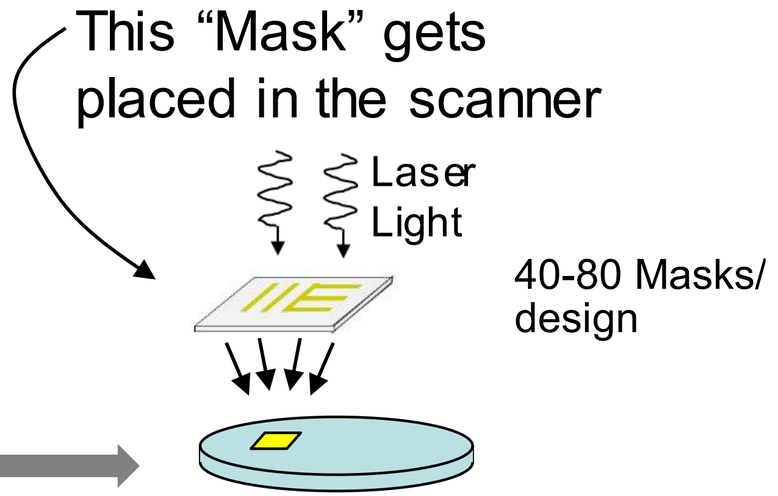
Designer: "Confirmed. Here is my layout."

Foundry: "Thank you. We will build these masks, then run the Si."

We "Tapeout" the digitized info to a Mask House

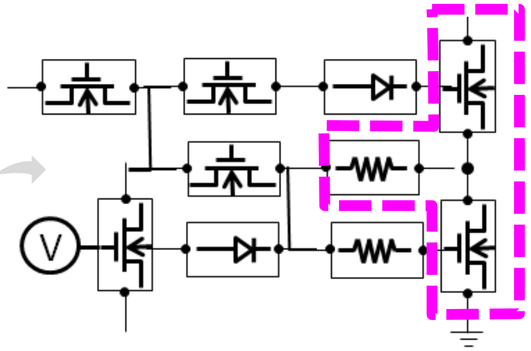
Fab Planning Starts wafers



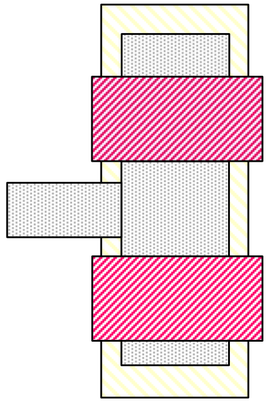


Design to Mask

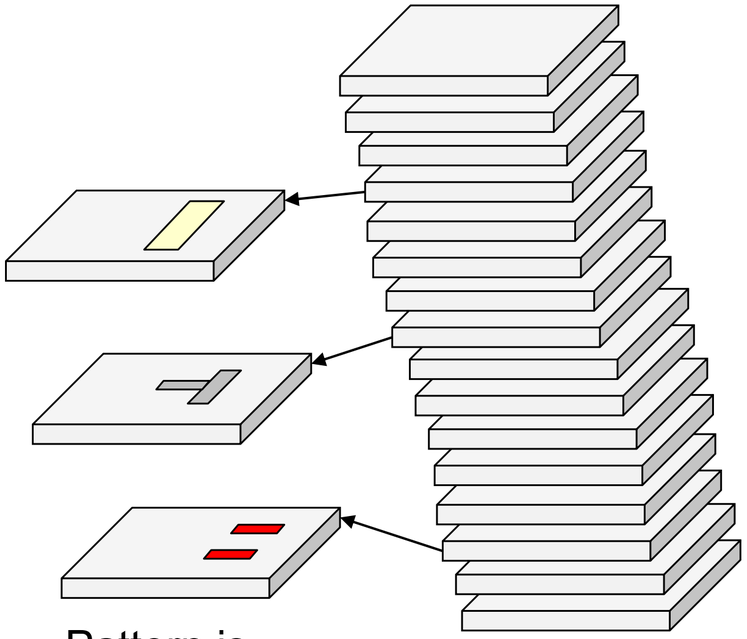
Algorithm → **Logic (10110..)**



Designer's View



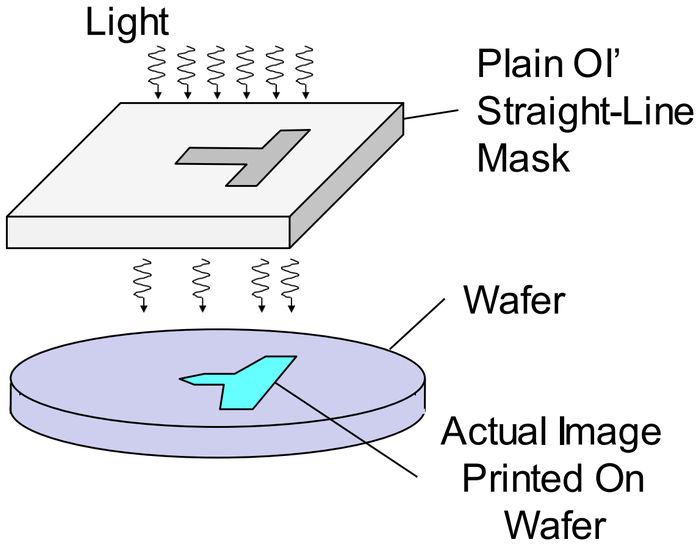
Layout View

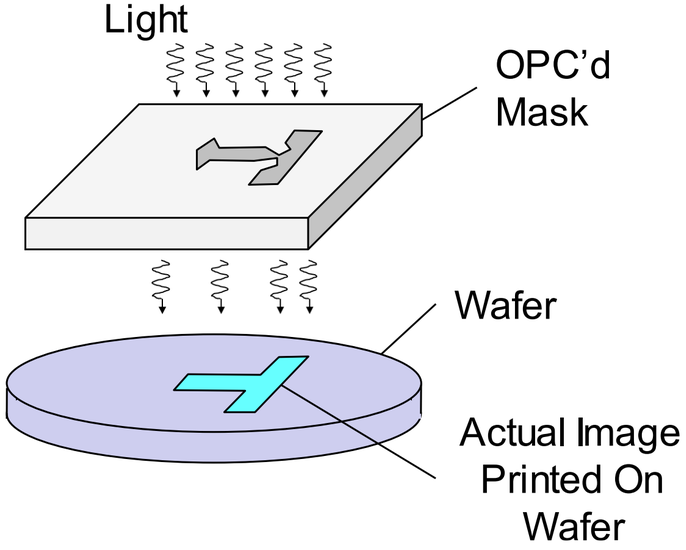


Pattern is On Masks

Complete Maskset

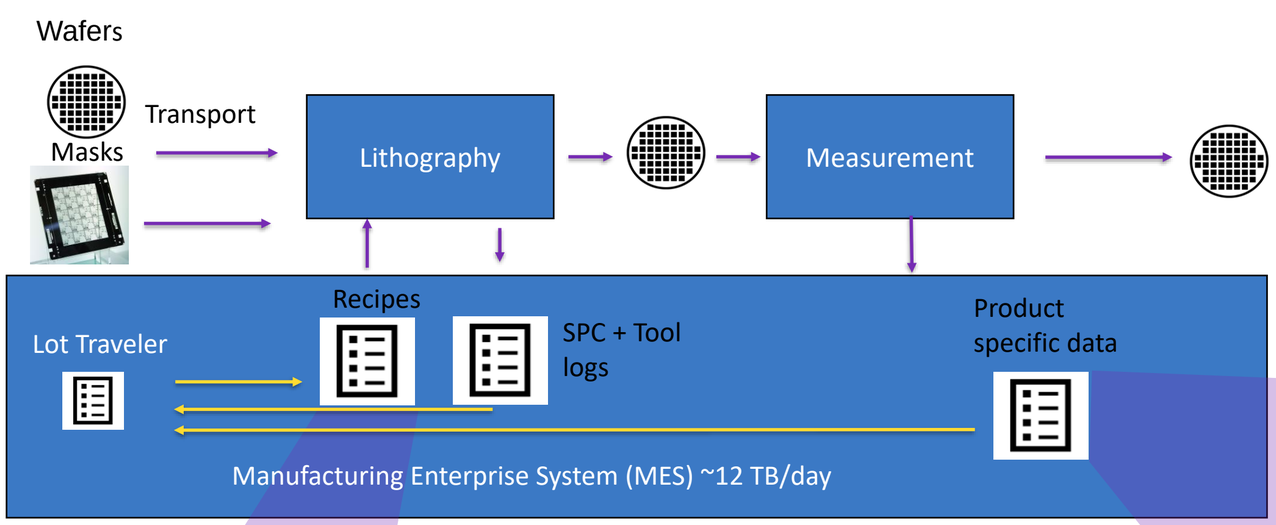
Optical Proximity Correction (OPC)



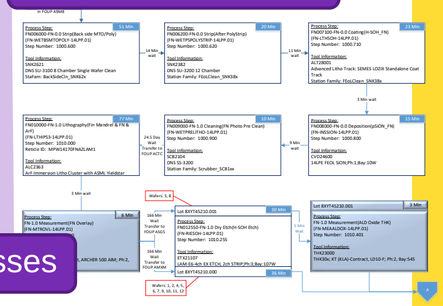


Fabrication as Transformation

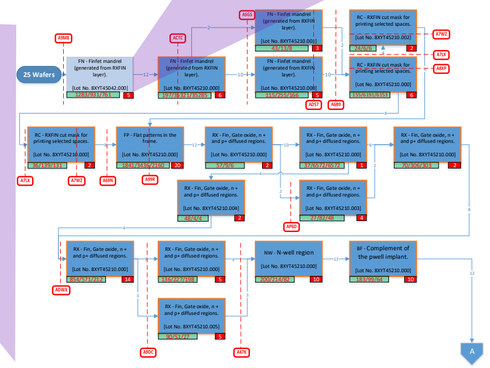
Design → Release → Mask Fab → Wafer fab → Post Fab

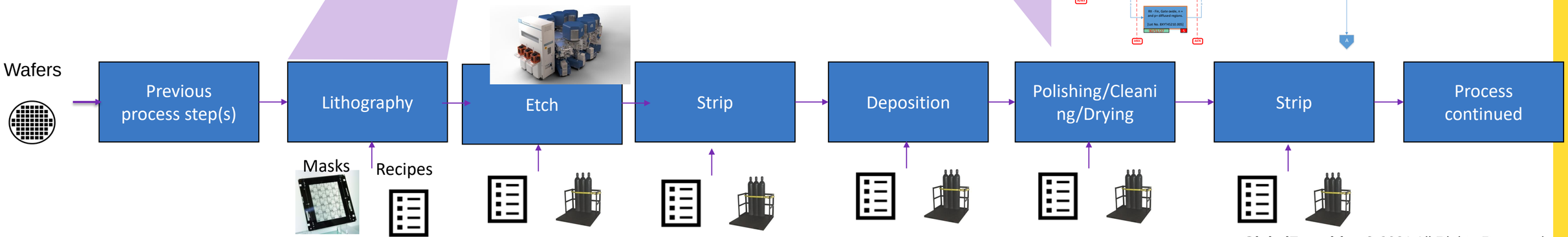


>950 Detailed Steps



>250 High-level Processes





What Tools Do we use?

Off-Line Metrology

AMAT Deposition

TEL Furnace

Kokusai Deposition

A Litho “Cell”

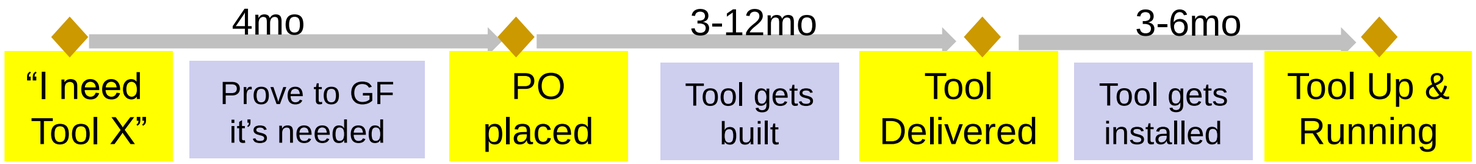
FOUP Loader

TEL Track

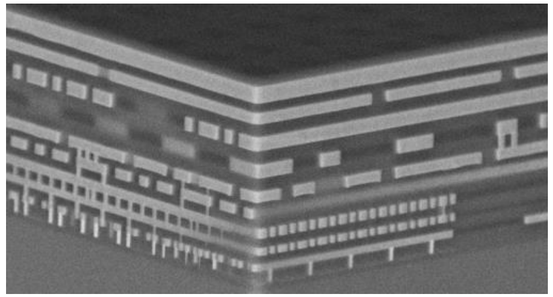
ASML Scanner

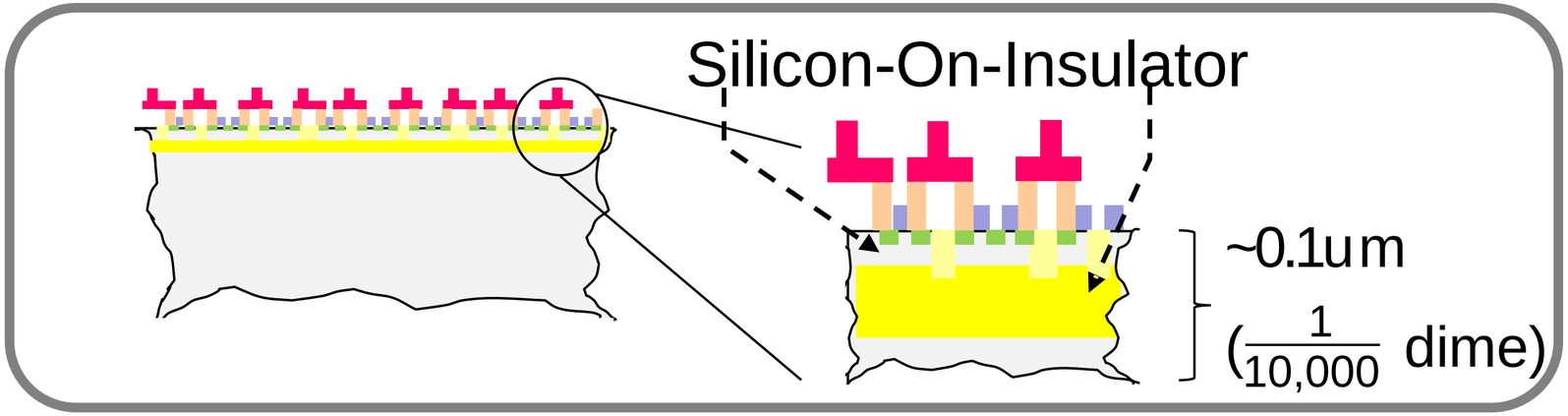
AMAT Implanter

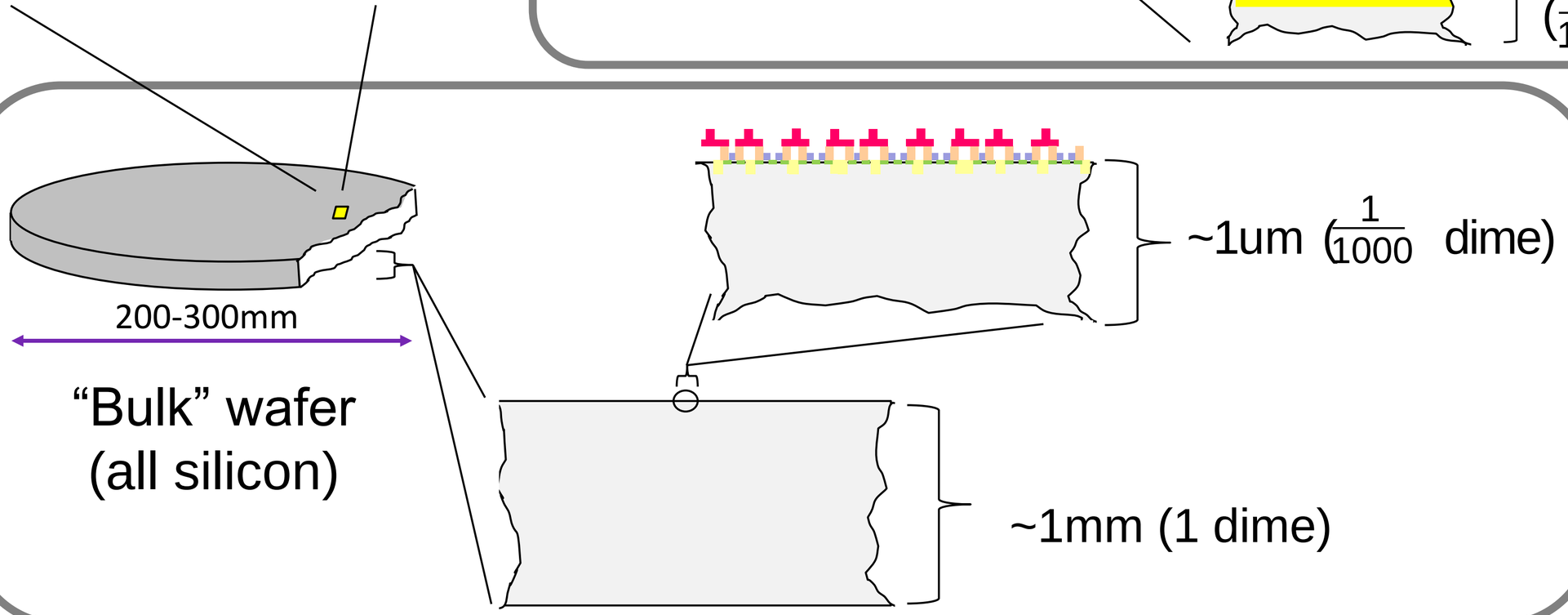
Ebara Polisher



Wafers and Technology sizes

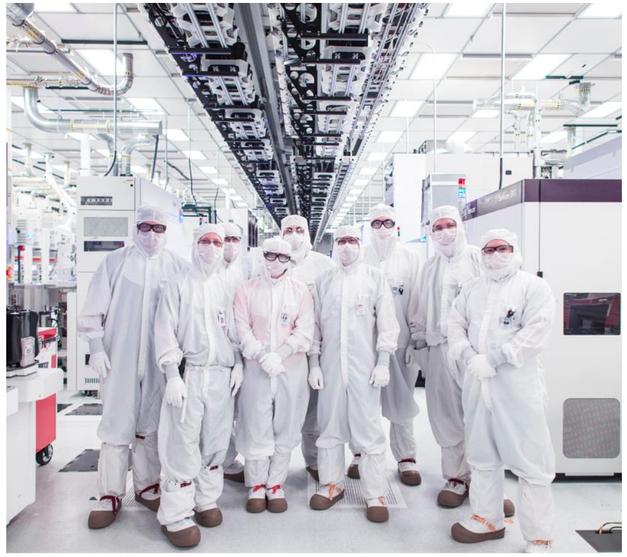






Who Does the work?

- Facilities: Keeping water / gases / chemicals / airflow clean & consistent
- Industrial Engineering: Planning materials movement through the fab (bottleneck tools, how many wafers to start, new tools for capacity, …)
- Equipment Engineering: Keeping the tools up / matched to brothers
- Process Engineering: Develop / maintain recipes (gas flows, temps, …)
- Integration: Determine the series of 1000+ steps to go from start to finish
- Test: Test plans run on probers to extract electrical data and publish for use
- Device Engineering: Analyze the electrical data: are chips operating correctly?
- Characterization: Electrical & Physical analysis (TEM, SEM, …)
- Metrology: Measure thicknesses, dimensions
- Contamination-Free Mfg (CFM): Defect detection / classification
- Yield: Combine results of Metro, CFM, Test, Char'n to increase # good die
- Packaging: Encapsulate the chip, and enable connections to circuit board
- Ground Rules / Design Manuals, PDK: Establish a "Rule Book" that our customers must follow as they design their chip, so that we can repeatably build what they ask
- Manufacturing Tech / Automation / IT: Data acquisition / manipulation / storage tools (billions of data points taken daily from tools, testers)



Who Does the work: Lots & Routes

Integration Engineer

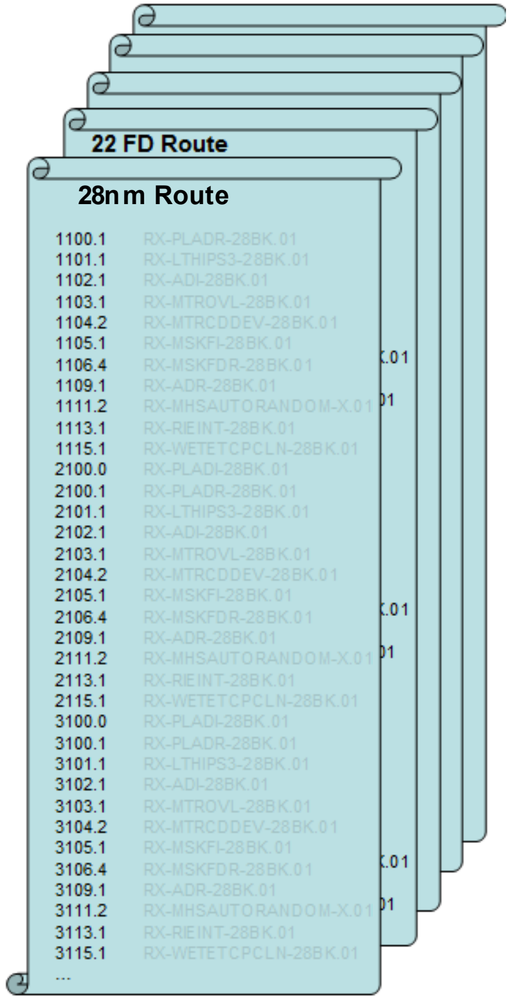
"I organize the series of 1000+ steps to enable all of the devices to be built in a single route."

Route-Build Engineer

"I check the route to assure tool-recipe agreement, and eliminate tool-to-tool contamination possibilities"

Operations Engineer

"I look across all lots in the fab, identify pinch-points, and maximize throughput."



Metrology Engineer

"I measure thicknesses and physical properties, enabling control charts."

Contamination-Free Engineer

"I detect & identify particles on the wafers to highlight tool / process issues."

Industrial Engineer

"I look at the tools & recipes listed on each route, and the predicted # wafers for next 2 years, and determine if we need to adjust / buy more tools."

Who Does the work: Facilities

Facilities Engineer
"I provide clean and consistent water, gases, and chemicals to the tool."

Automation Engineer
"Every wafer, every recipe, I assure the software monitors for errors / hiccups and reports all processing details."

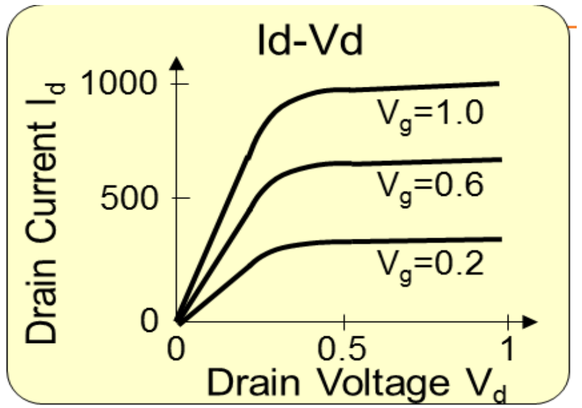
Equipment Engineer
"Given confidence in consistent raw materials, I assure the valves, flow controllers, sensors are working, so we get the exact flow we want at the temp we want."

Unit Process Engineer
"Given confidence in flow rates, I develop a recipe which calls gases, flows, and temps so that we deposit / etch exactly what we want – no more, no less."

Who Does the work: Technology

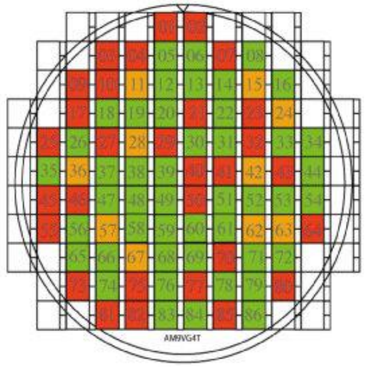
Device Engineer

“I look at outputs from individual devices, and advise on how to improve performance.”



Test Engineer

“I probe individual devices and full circuits, and provide the data in useful format for analysis by others”



Reliability Engineer

“I stress the individual devices and the full chips beyond normal conditions, to enable estimation of lifetime.”

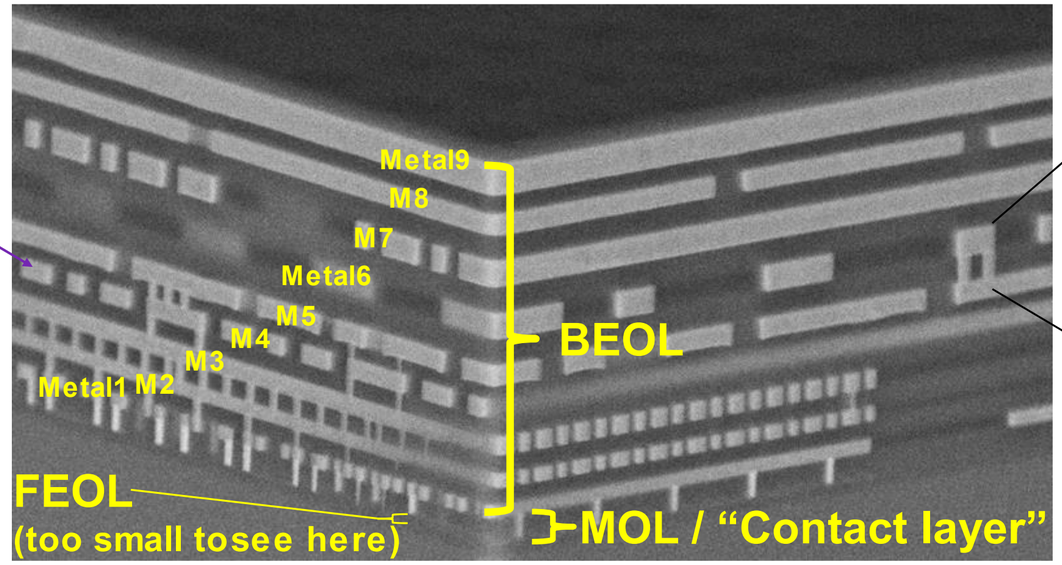
Yield Engineer

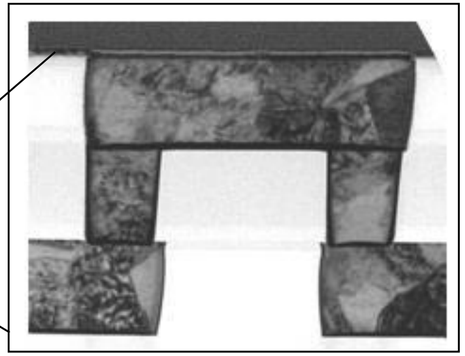
“I look at outputs from full circuits and memory arrays, and correlate to metrology / contamination results, to determine how to increase the % working chips.”

Chip Levels

Back end levels (BEOL)

- Build up of insulating layers, metal interconnect wiring, and vias defining passive structures
- Routes power and ground
- Connects front end structures to define chip functionality
- Interfaces with external connections





Metal 6

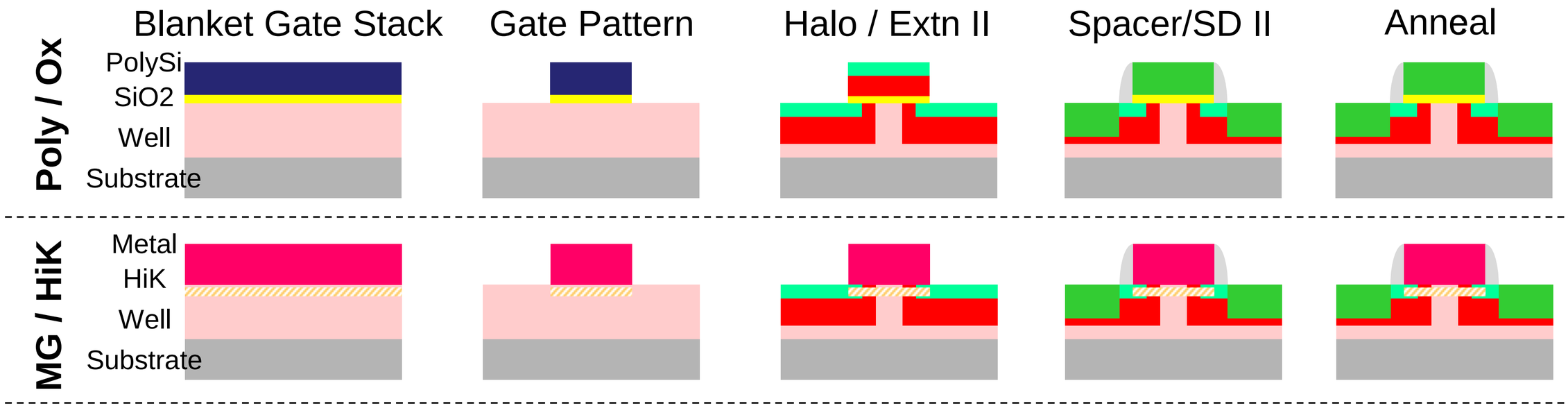
Via 5

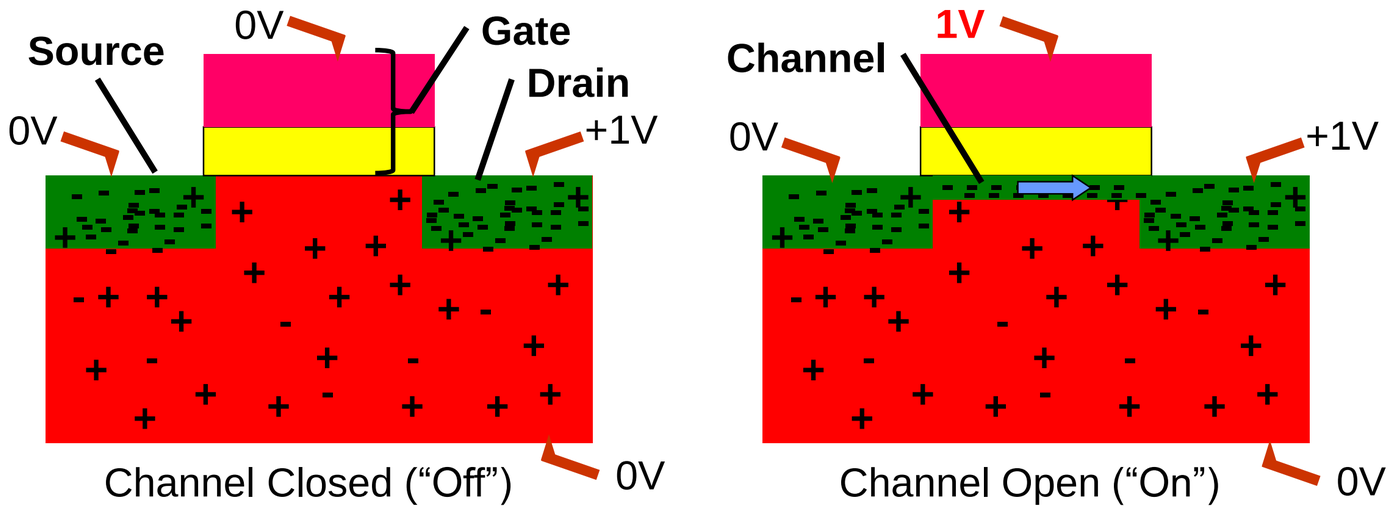
Metal 5

Front end levels (FOEL)

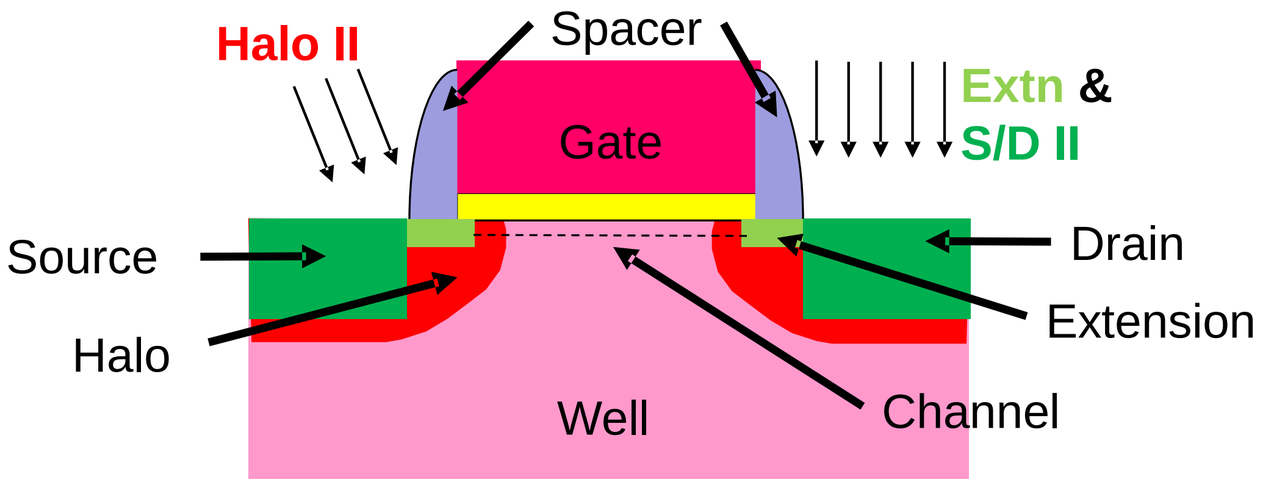
- Build up of insulating layers, and polysilicon, diffusion, & implants, defining primitive active circuit Devices:
  - Transistors
  - Diodes
  - Capacitors
  - Resistors
  - Memory storage elements
- Creates primitive building blocks for subsequent connection with back end levels to create functionality

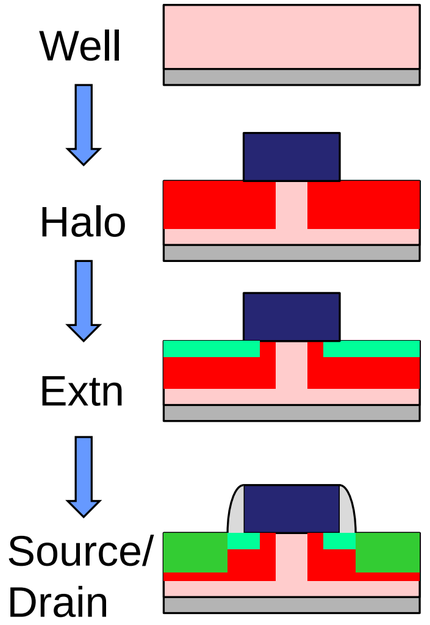
Front End: Transistor and Gates





Implants





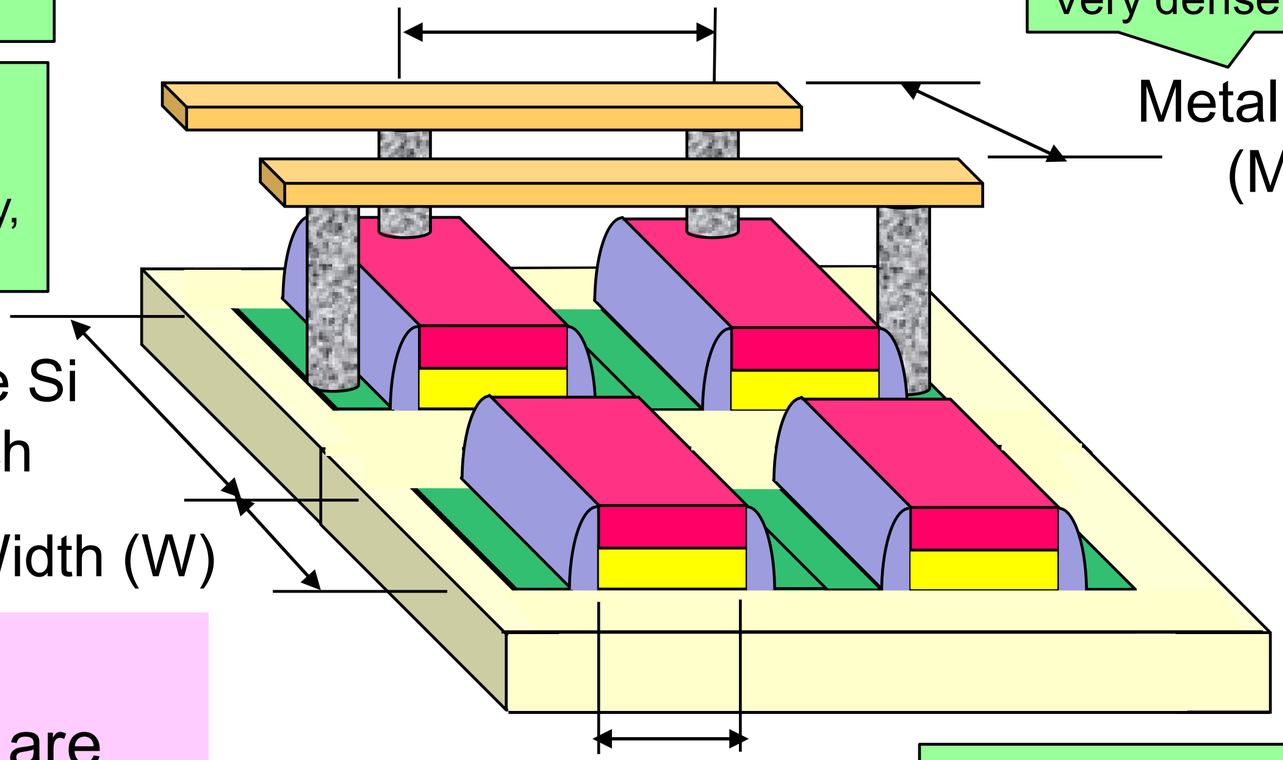
- Halo implants block current from passing beneath the channel. This implant is the opposite type to the Source and Drain.
- Extension implants are used to “extend” the source and drain under the spacer. These are doped the same as the S/D (n-type for NMOS, p-type for PMOS).
- Transistors require several different doping / resistance levels

Implant	Dose (cm^{-2})	Doping Conc’n (cm^{-3})	Resistivity
Wells	~5E12	~5E17	High
Halo	~5E13	~5E18	
Extension	~5E14	~5E19	
S/D	~5E15	~5E20	Low

Technology Node: CMOS

For so many years, we made gates from polysilicon, that we started calling gates “poly.”

Active’ Si is means the electrically active (doped) regions,where we’re building devices. Essentially, whatever is NOT isolation.

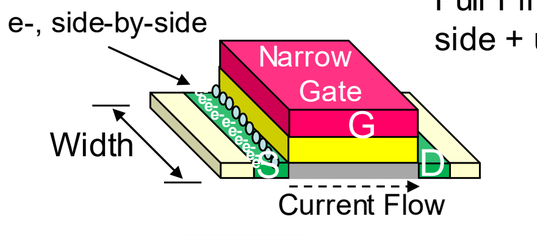


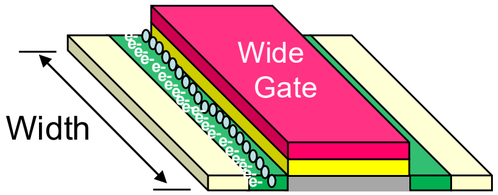
Metal 1 is the lowest metal in the BEOL stack. Very densely packed.

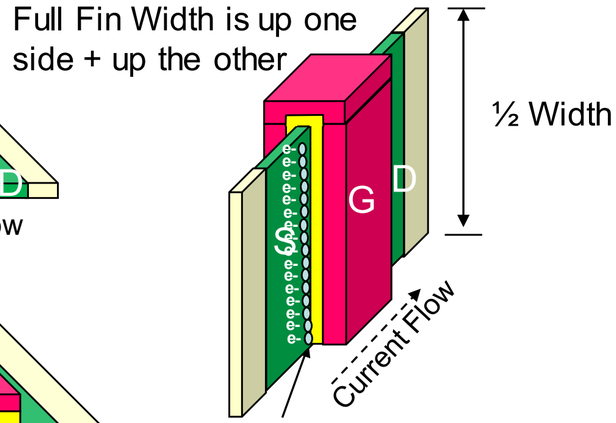
Here we show a Planar Technology – the X’tors are in the plane of the wafer.

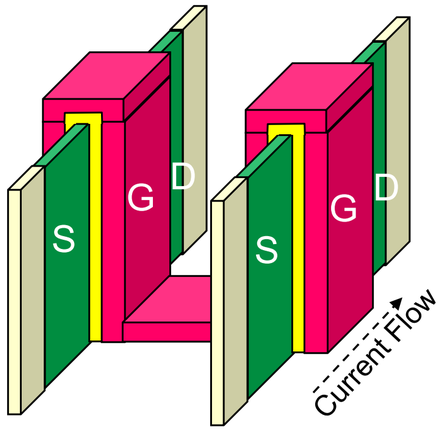
Shorter Lg = less distance for e- to travel, so faster switching

Technology Node: CMOS FinFET





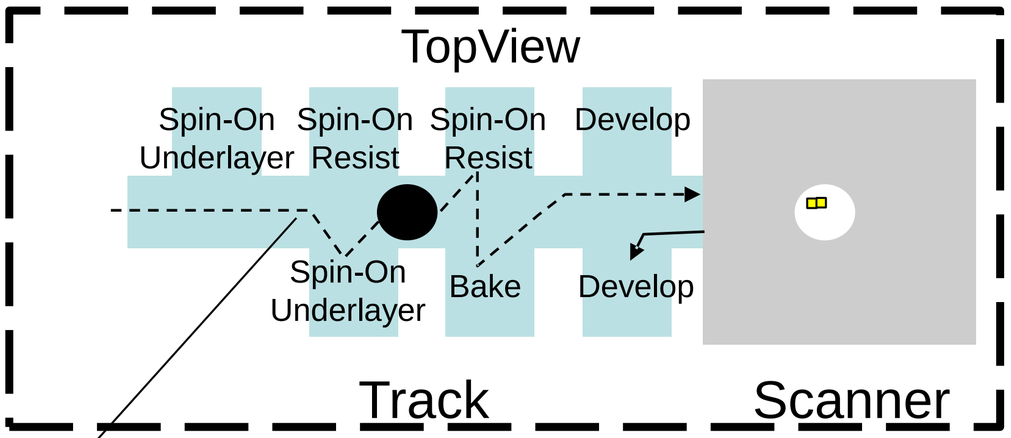




FinFET Technology (14, 10, 7nm)

- Nodes are known by their key lengths & pitches:
  - Gate Length
  - Metal 1 Pitch
  - Fin Pitch (new)

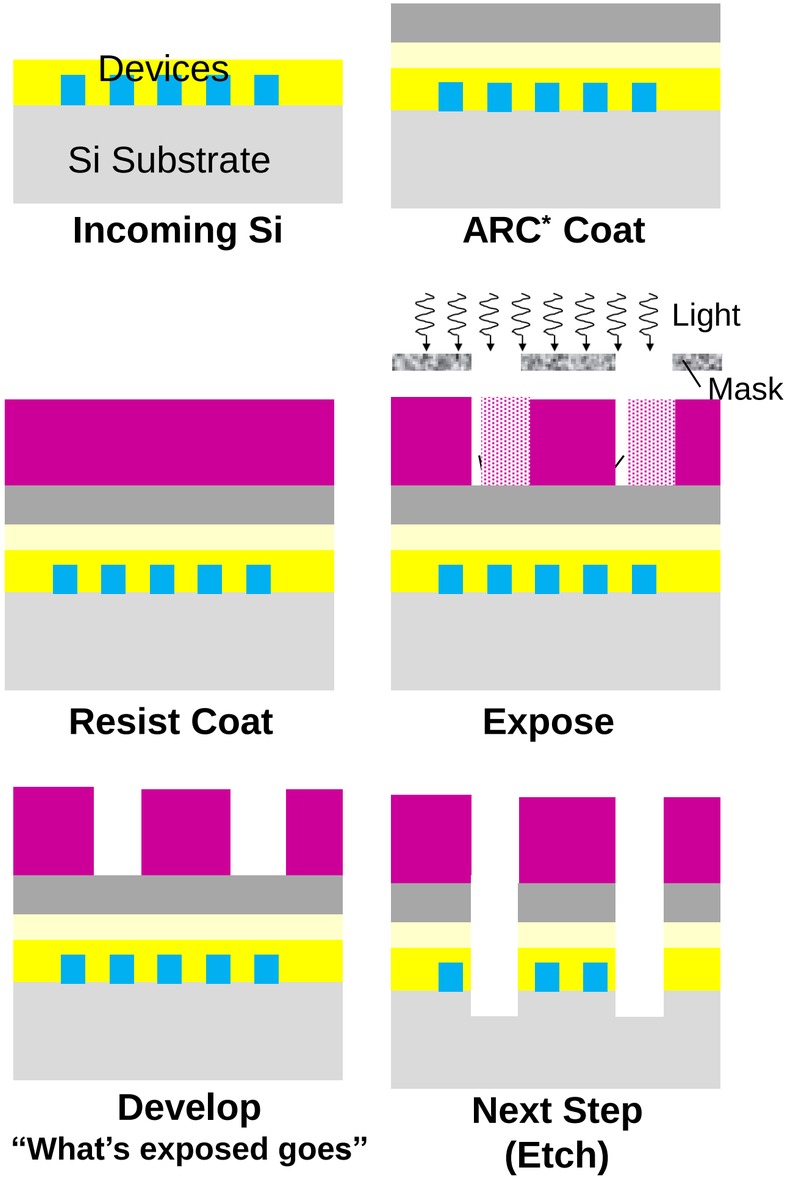
Litho: Track and Scanner



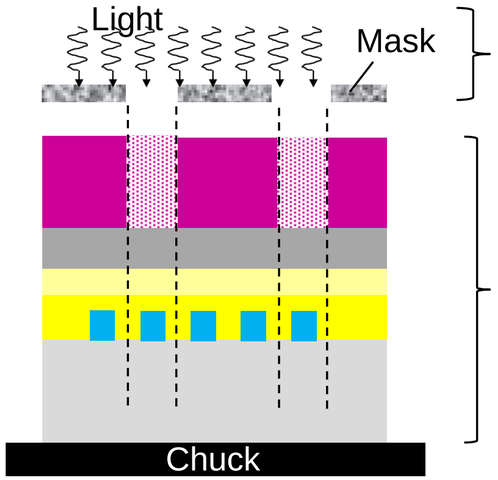
Wafer moves through various points on the track

Shines light to “expose” first die, then wafer “steps” slightly to the next spot, and expose the next one.

Side View

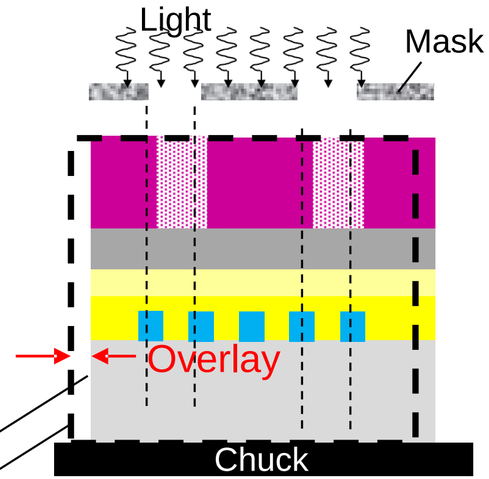


Litho: Overlay

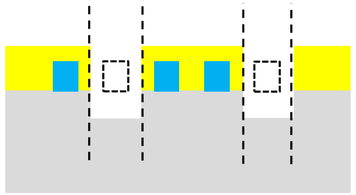


This is part of the Litho Tool.
It doesn't move…

… but the wafer is on a move-able chuck.
We try to bring it back to the exact same spot as when we printed 2 days ago.
That would be a perfect "Overlay".

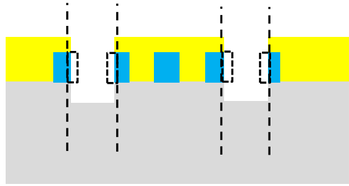


Where it is today
Where it was 2 day ago



Perfect Overlay
= Good Etch

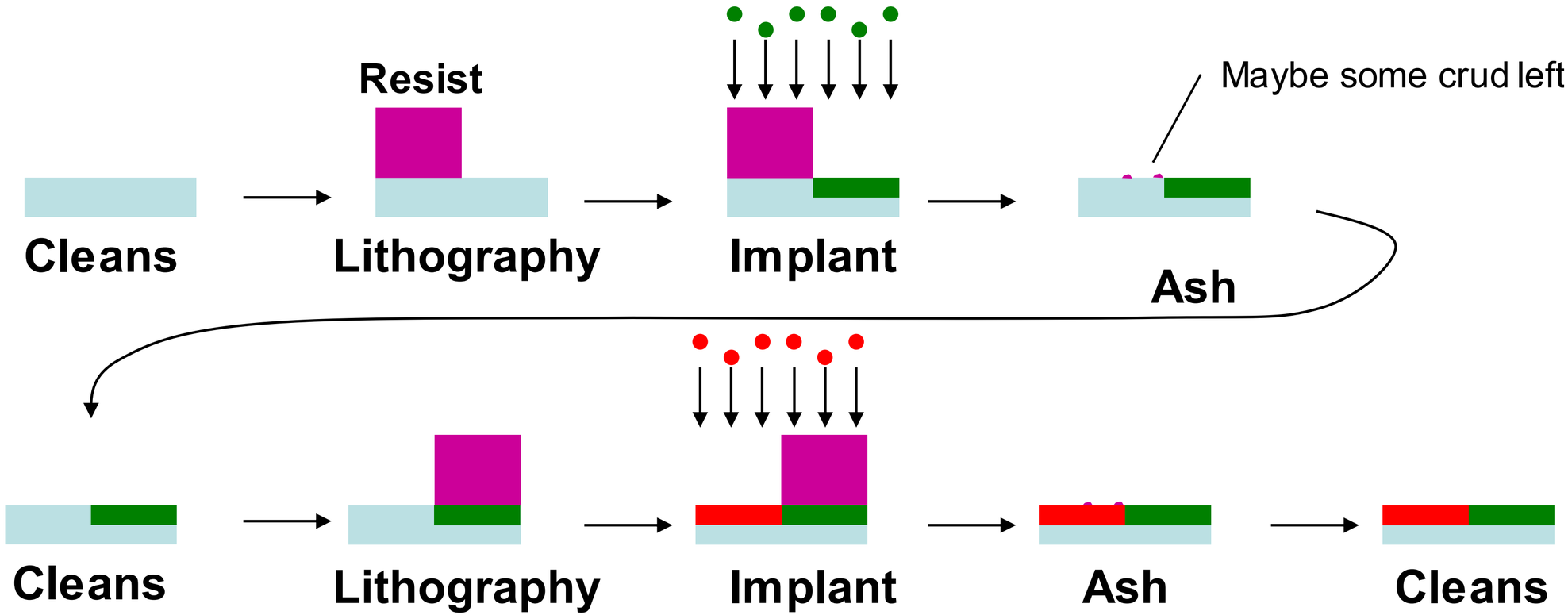
Bad Overlay
= Bad Etch



- When I shine my light, how well am I lined up with the underlying structures?
- Overlay on current tools ~5nm, meaning the tool says:
  "I can always come back to within 5nm (~20 atoms) of where I was last time"

  … Amazing

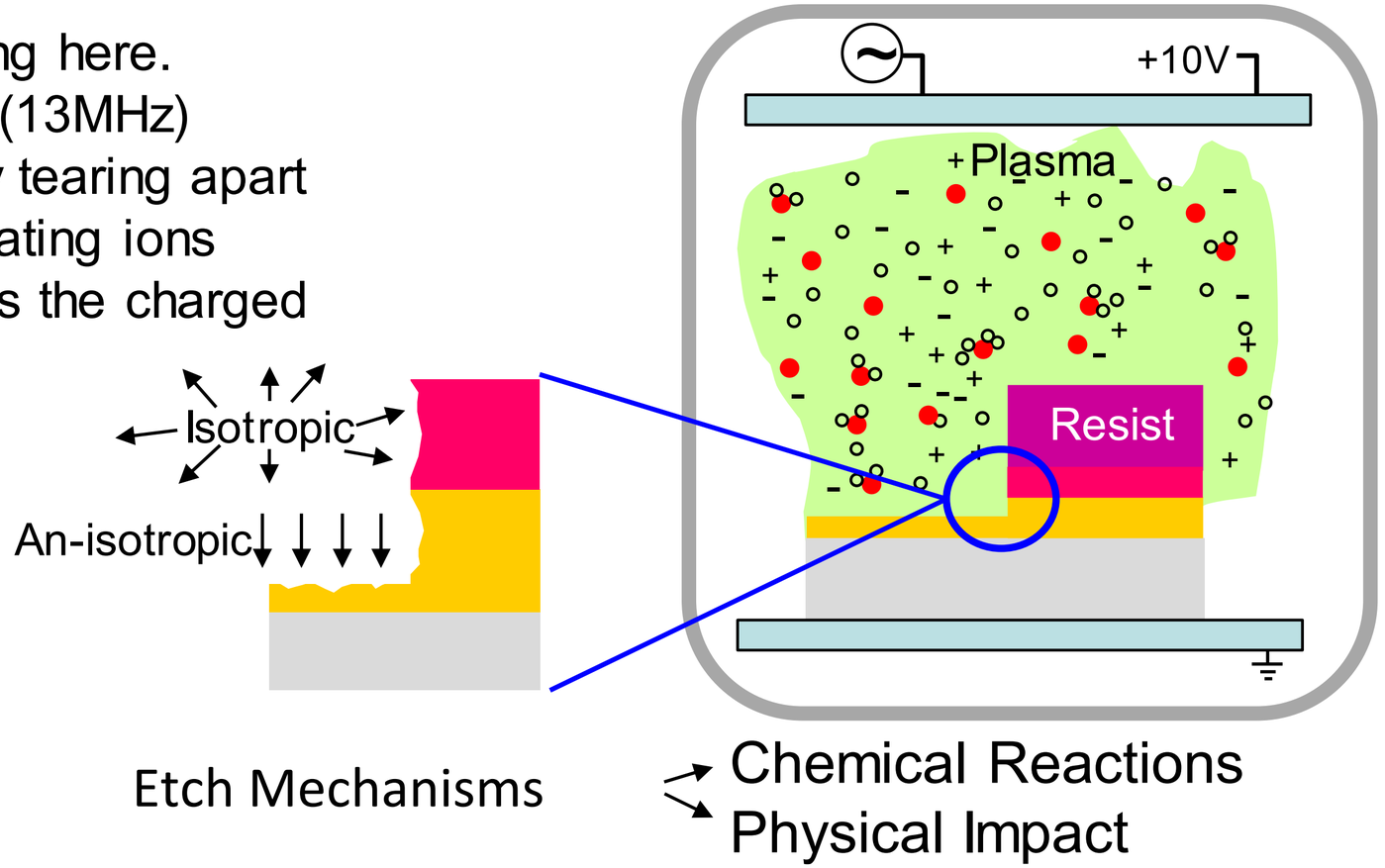
Litho, Implant, Etch…



- We have created 2 distinct regions of different doping – N and P.
- Together these form a Diode. We've made a device!

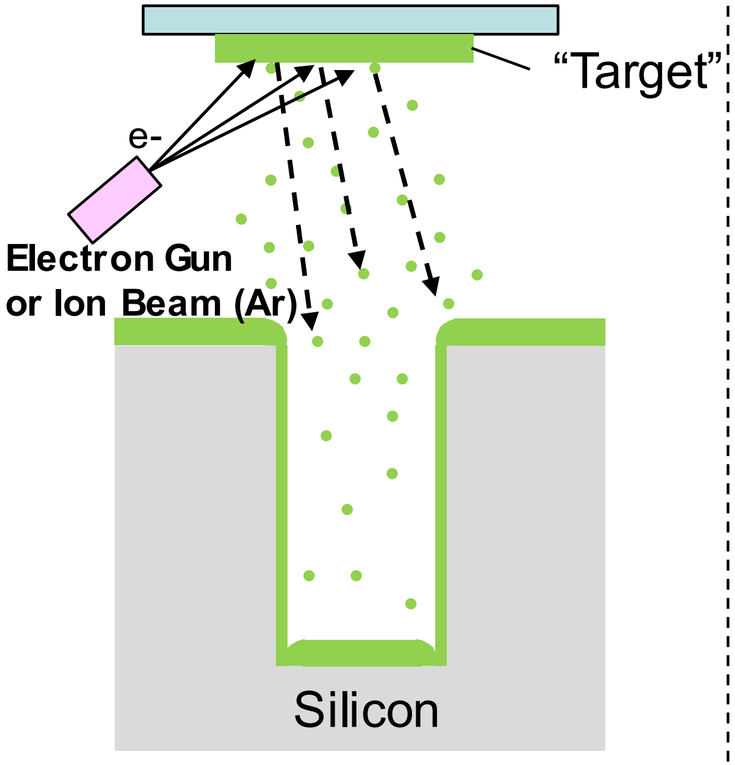
Etch: Reactive Ion Etch

There are 2 voltages happening here.
- High Frequency Alternating (13MHz)
  This creates the plasma by tearing apart the atoms in the gas, creating ions
- Constant (DC) voltage drives the charged ions down to the surface



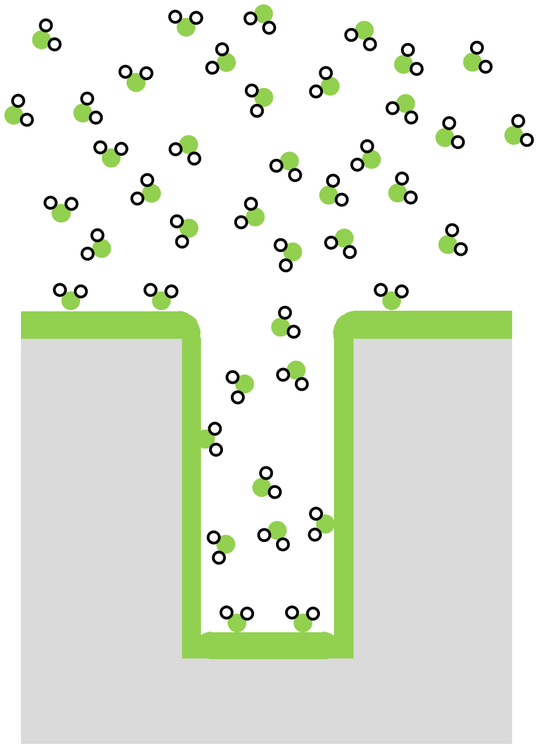
Many Etches are used in semiconductor fabrication … RIE is the most common and controlled

Deposition Methods

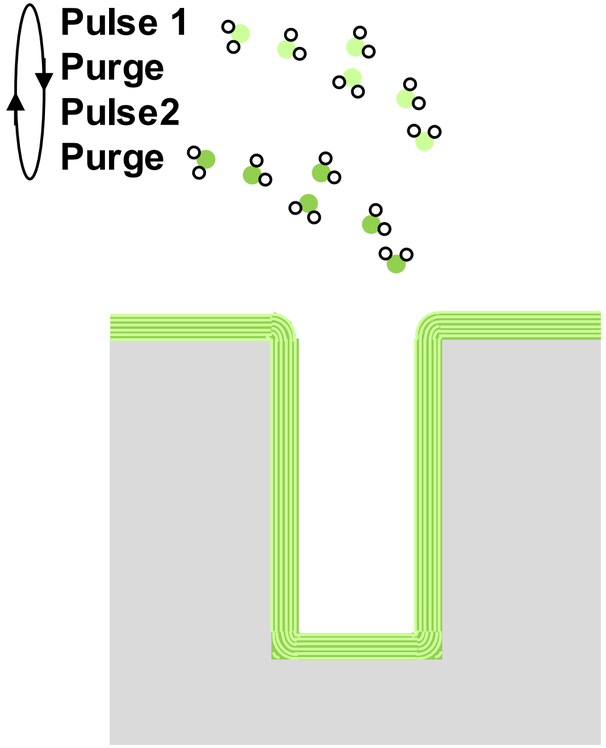


PVD = Physical Vapor Deposition

Fast / Cheap
Less Control
Ideal for thick films
Conformality 30-90%



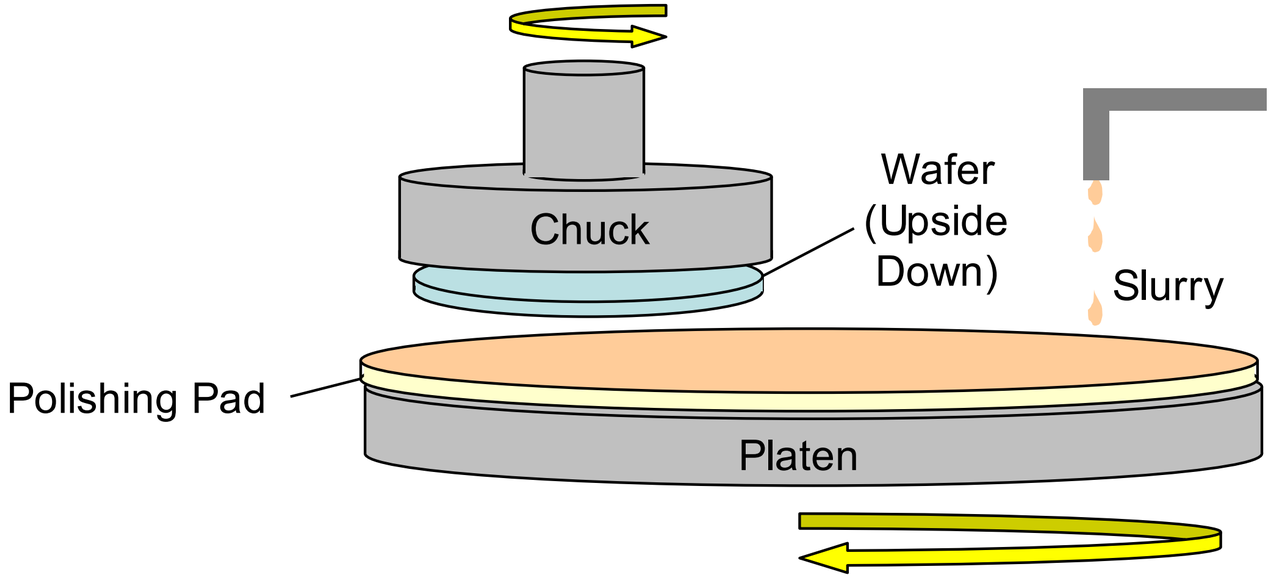
CVD = Chemical Vapor Deposition

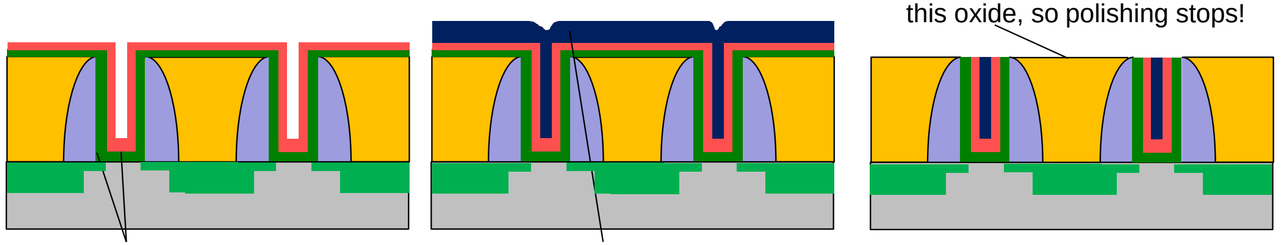


ALD = Atomic Layer Deposition

Slow /Expensive
Great Control
Ideal for thin films
Conformality ~100%

Chemical Mechanical Planarization





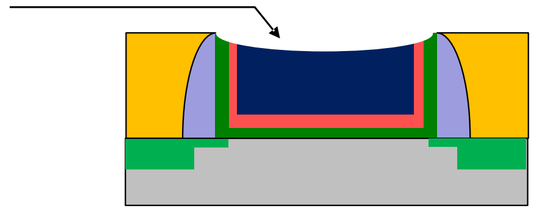
These 2 layers done by Atomic Layer Deposition (HiK & TiN, for example)

Remaining gap is filled by Chemical Vapor Deposition (Tungsten). “Over-fill” is OK.

Chemical reaction won’t occur on this oxide, so polishing stops!

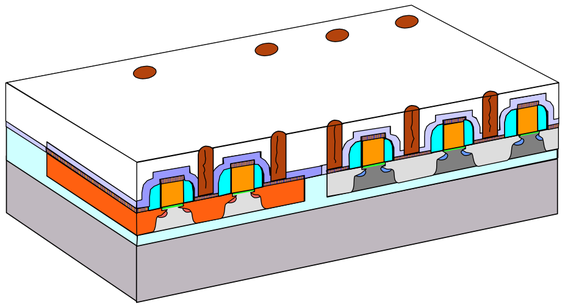
Polish (CMP) to remove undesired excess material.

Features that are too wide can dish…



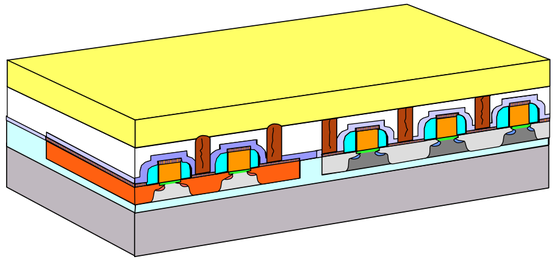
Back End : Metal 1

1



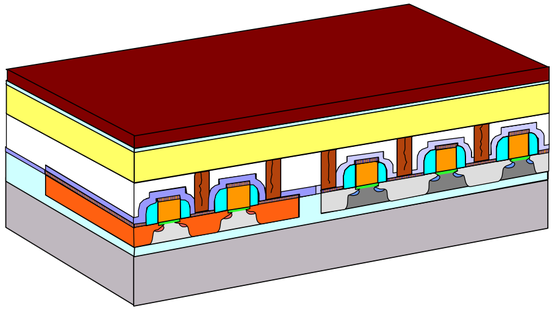
Reveal Vias to transistors

2



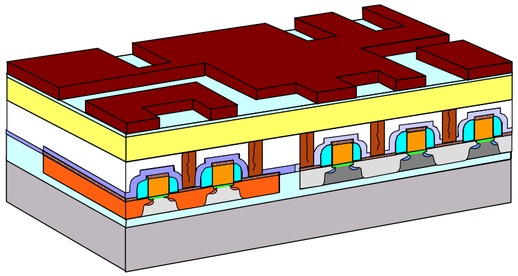
Deposit oxide dielectric

3



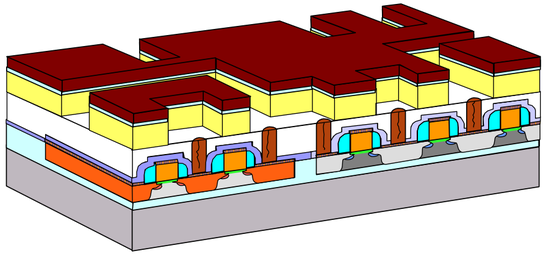
Deposit photoresist

4



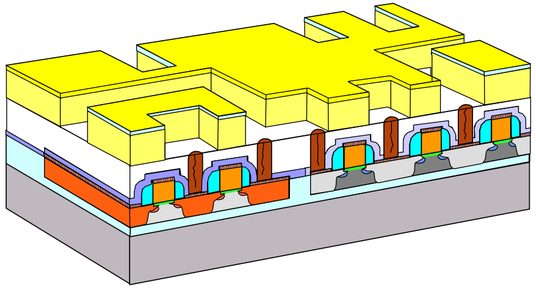
Pattern photoresist

5



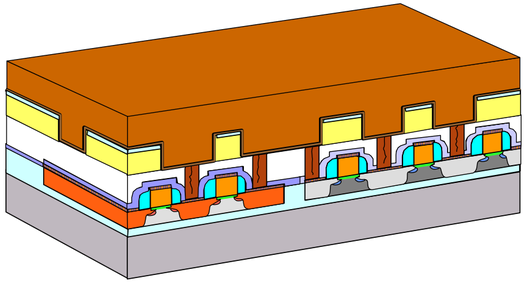
Etch oxide dielectric

6



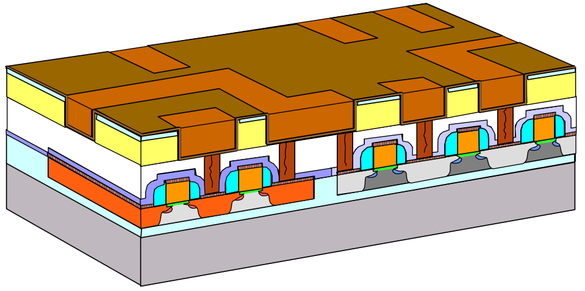
Strip photoresist

7



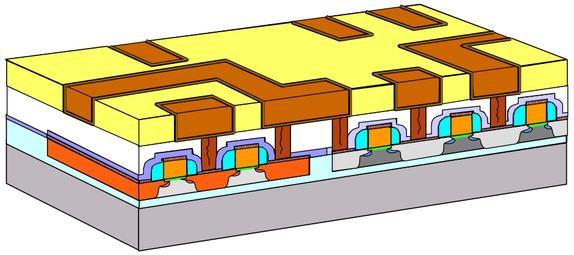
Deposit liner & plate copper

8



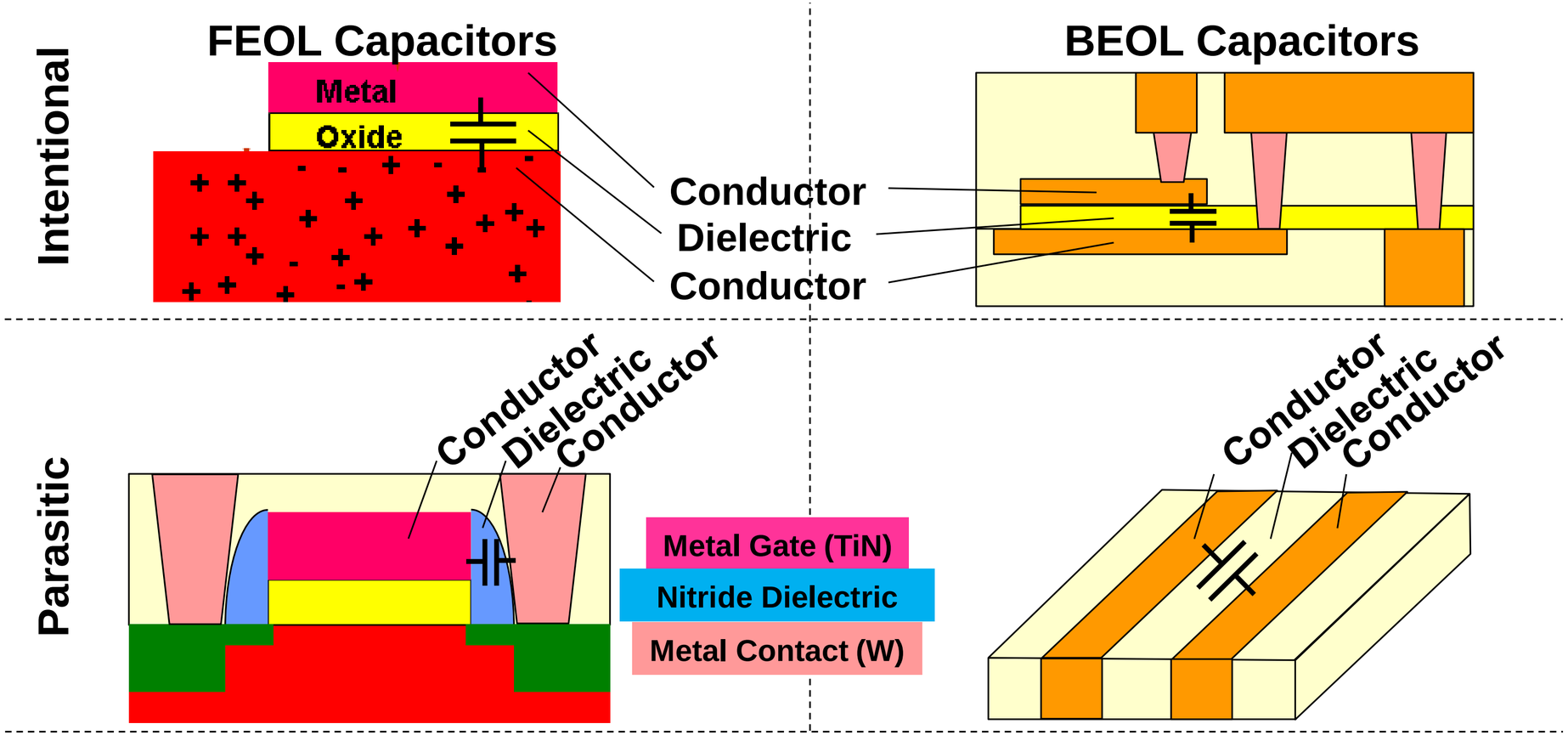
Chemical Mechanical Planarize to liner

9



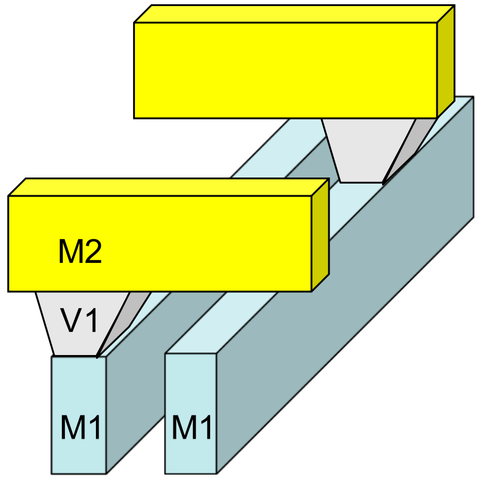
Remove liner

Capacitors

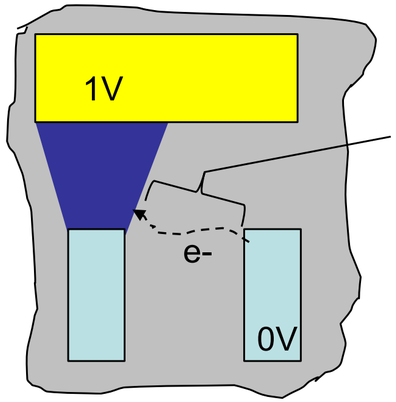


- A capacitor is simply a stack: Conductor / Dielectric / Conductor
- Some capacitors we build intentionally so we can store charge in our circuit.
- Others occur unavoidably. These are referred to as “Parasitic” capacitors.
- BEOL capacitors are often called “MIMCaps” (Metal / Insulator / Metal).

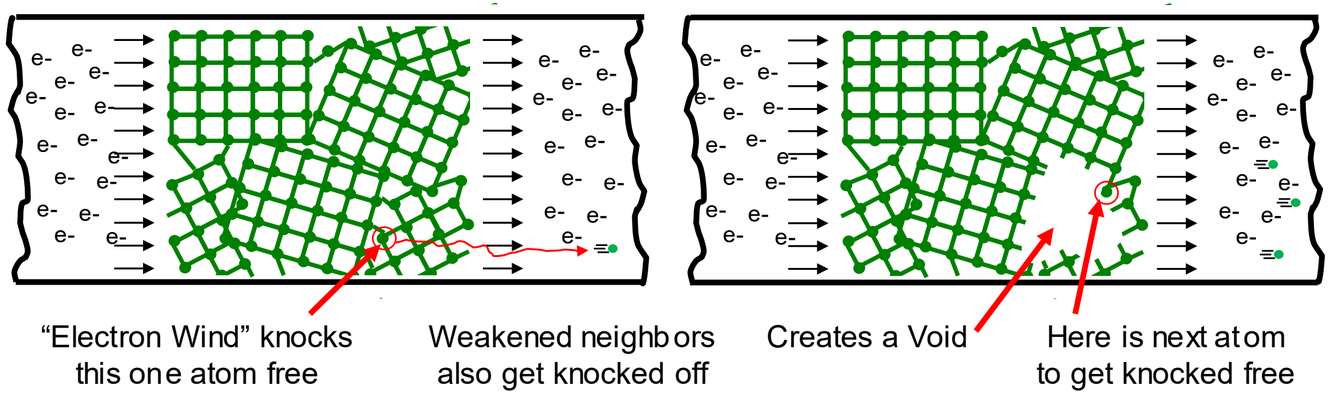
Interconnect: Leakage & Voids



TDDB leakage path



This distance is critical

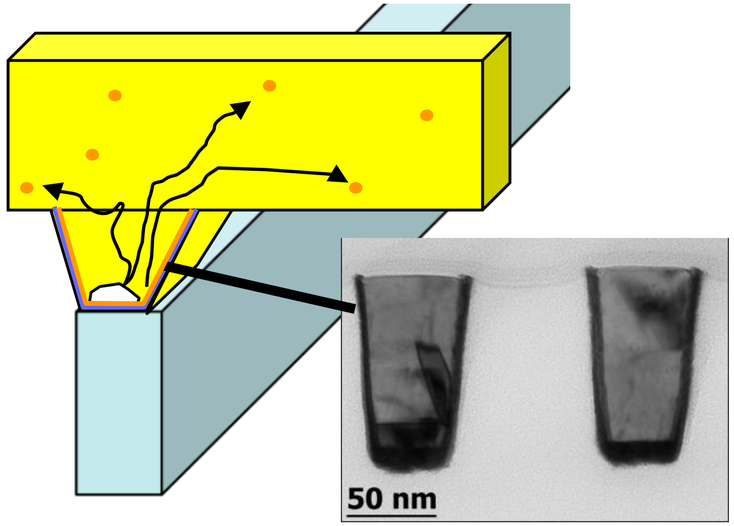


"Electron Wind" knocks this one atom free

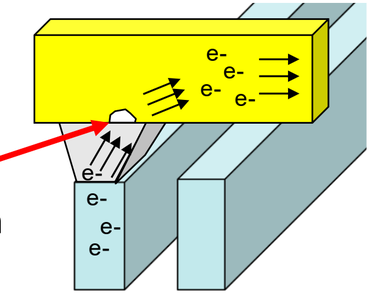
Weakened neighbors also get knocked off

Creates a Void

Here is next atom to get knocked free

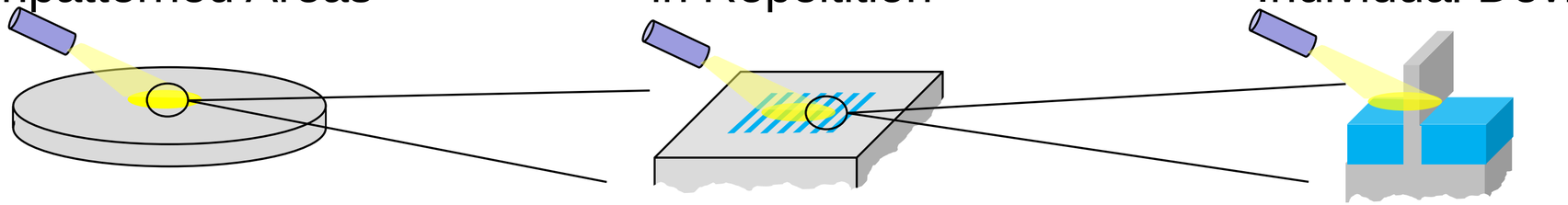


- Electrons are 1/1000th the size of an atom …
  … but if enough hit an atom, they can move it!
- The atom leaves behind an empty site.
  Its neighbors are now weakened …
  … and they are the next to get knocked off
- If enough of these atoms get moved, a void is created.
- Small voids ➔ Large voids ➔ Line Breaks ➔ Death
- Avoid EM by a) material selection (interface layers);
  b) careful processing & eliminating initial defects



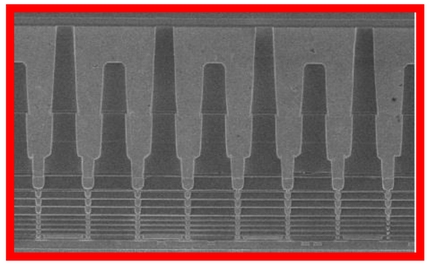
Metrology Overview

Impact to wafer	Scrap wafer & Analyze outside the fab	Analyze in the fab[1], then scrap wafer	Analyze in the fab, and keep wafer running
Spot Size across wafer	Large, Flat, Unpatterned Areas	Small Patterns in Repeitition	Specific, Individual Device
Depth into wafer	Thick Bulk Layers (100nm +)	Thin Layers (2-100nm)	Surface Only - Several atoms thick (<2nm)



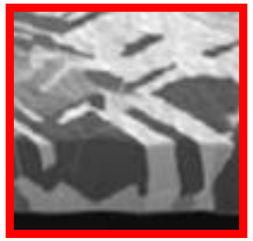
SEM and TEM

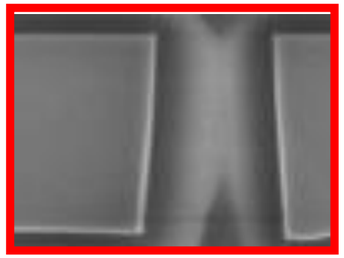
10,000nm
10 u m

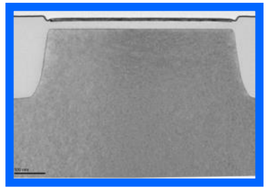


Multiple Layers

1000nm
1 u m

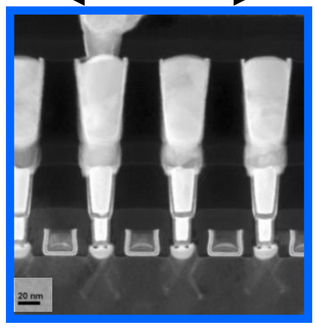


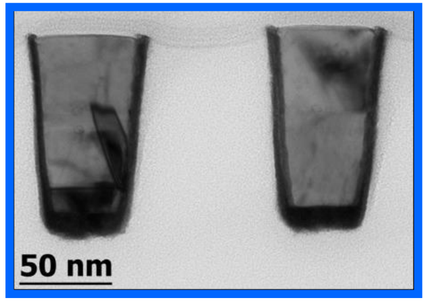


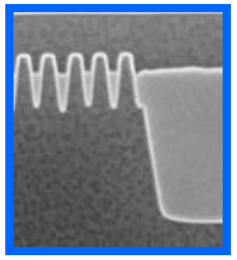


Single Layer

100nm

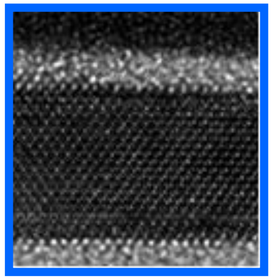






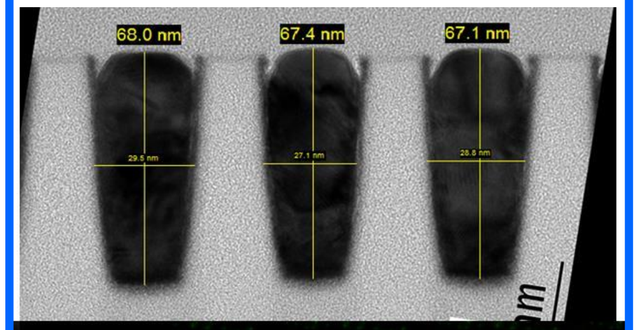
Single Structure

10nm



Atom Spacing

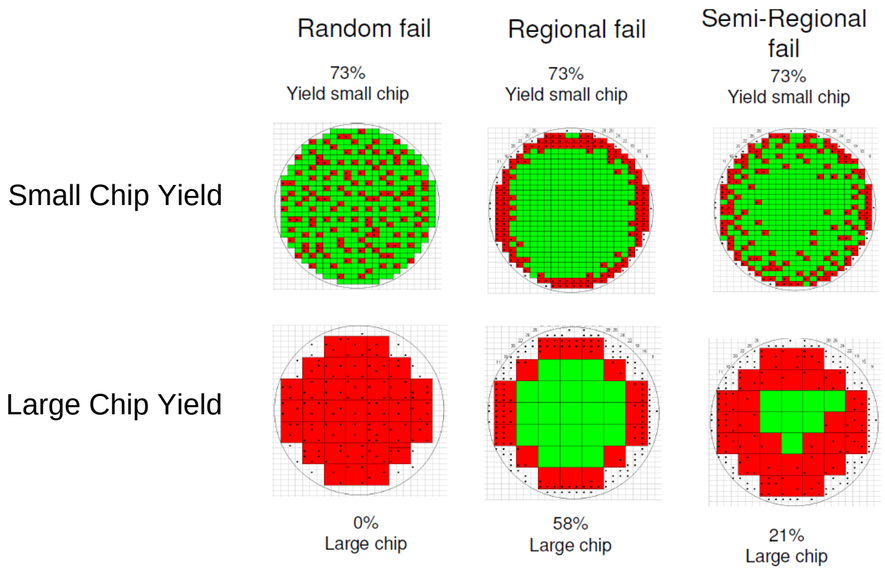
Can Detect Elements

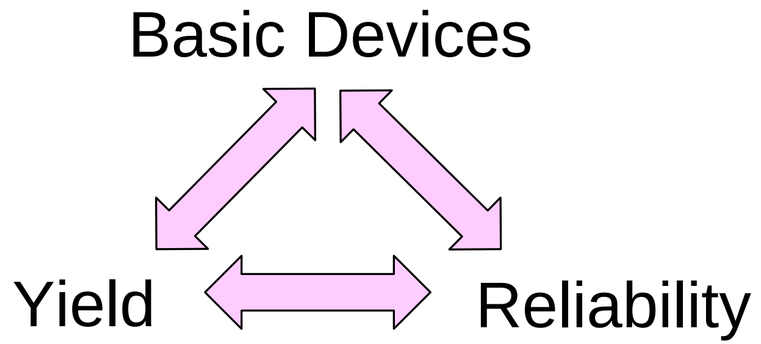


Yield is King

$$\text{Yield} = \frac{\text{\# of Functional Die on a Wafer}}{\text{\# of Total Die on a Wafer}}$$

Chance of a Die Yielding	=	Chance of No Parametrics Defects	X	Chance of No Systematic Defects	X	Chance of No Random Defects
72% Yield	=	90%	X	90%	X	90%

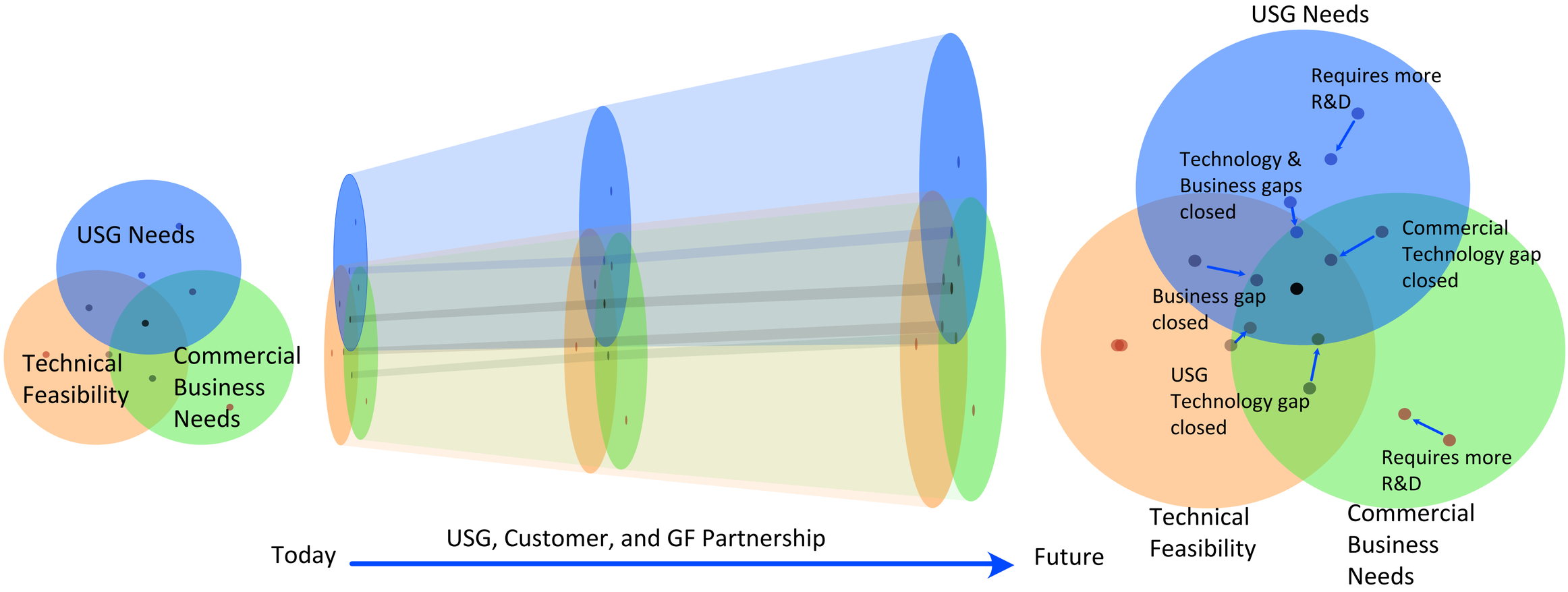




Yield requires volume and constant battle with physics… …volume requires commercial markets and investments

Aligned Futures Roadmap

Opportunity for Maximizing technology alignment through Industrial Policy



Dual-use technology initiatives with USG partnership and funding to deliver domestic production capabilities and capacity for Critical Infrastructure and Specialized Defense needs

Summary

Foundry Ecosystem and Technology is complex and at the edge of physics

- Foundry Ecosystem is the way that ideas are transformed to technology through differentiated microelectronics platforms driven by commercial market forces
- Systems require a diverse set of advanced technologies (majority >12nm): digital, analog, rf, mixed-signal, power, photonic, etc., to enable specialized capabilities
- Foundry Ecosystem requires design infrastructure, IP, and fabrication for masks and wafers, and advanced packaging for a diverse set of technologies and applications
- Yield and quality are the focus of foundry manufacturing and requires very high volume and a talented workforce looking at the finest of details
- Technologies optimized for dual use will require an alignment of roadmaps and funding from the USG and Customers

*Thank you to Bill Taylor for a number of slides throughout the presentation.

BACKUP