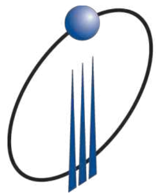
System in Package Tutorial (MCM/Hybrid)

Presenters/Hosts (in order): Matt Bergeron/Sultan Lilani Hosts
Tony Lowry, SEAKR, Matt Bergeron, Integra, Ken Halsey, Integra, Sultan Lilani, Integra

Celebrating Over 35 Years of Providing High Quality Semiconductor Services

June 29, 2021



System-in-Package Benefits

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- Simplifies the product system board
  - Layers and density
  - I/O count and pitch
- Increases functionality per unit area/volume
  - Reduced size
  - More performance in less space
- Improves Electrical Performance
  - Reduces parasitic
- Reduces Manufacturing Costs
  - Reduced component count
  - Inventory and carrying costs
  - Lower supplier support
  - Improve yield

- Improved Reliability
  - Solder joint reduction
- Lessens specialized expertise and testing requirements
  - Simplifies complex RF functions
  - Eliminates tuning at the system board level
  - Tested subsystem functions
- Improves time to market
  - Make changes to subsystem without (costly) changes to system board
  - Standardize subsystem “Macros” across a product family
- Can be a platform for derivative products

Note: Benefits can move to detriments if bad decisions are made on key considerations and trade-offs

K.I.S.S. Rule

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- **The more complex you make a system/package = the more challenges to overcome**
- **Some of the Challenges:**

Challenge #1 – Can I actually make the substrate work? (thickness, performance, widths and space/cost)

Challenge #2 – Can I procure the parts needed in the formfactor that will work (can you get die?)

Challenge #3 – Mathematically the more components you have in a system the more likely a failure. Simple example: 1 die in a flip chip & 90% typical yield = 90% Yield
5 die in a SiP and 90% yield on each = 59% yield
(.9x.9x.9x.9x.9)

Challenge #4 **-** Reliability. The mix and match of components, shields, die, etc. can create stresses at the package or board level.

Challenge #5 - Testability -Testability has to be designed in from the beginning.

Agenda/Topics Covered

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1 Key Engineering Considerations

a) Design considerations and trade-offs
b) What to include
c) Key Engineering considerations

2 Layout and Fabrication of Substrates

a) Substrate
b) What to know before you start
c) Design rules and cost drivers

3 Assembly Considerations

a) Floor Plans
b) Assembly Design Rules
c) Stacking/encapsulation

4 Testing, Qualification & DPA

a) Test considerations
b) Complex Testing
c) Qualification Testing

Engineering and Segmentation

Tony Lowry, SEAKR Engineering LLC

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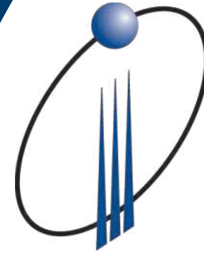

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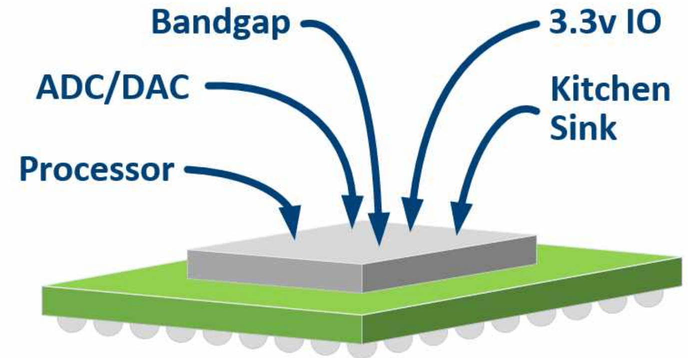
The ASIC Challenge (System on a Chip)

- Traditionally, ASICs integrate as much technology into a single die as possible
  – Integration saves power and size

<u>However</u>

  – More integration into advanced nodes
    - Greater cost
    - IP limited availability or IP porting fees
    - Yields go down
  – Industry has reacted by creating more flexible ASICs to cover multiple applications



Smart De-aggregation of ASIC Design

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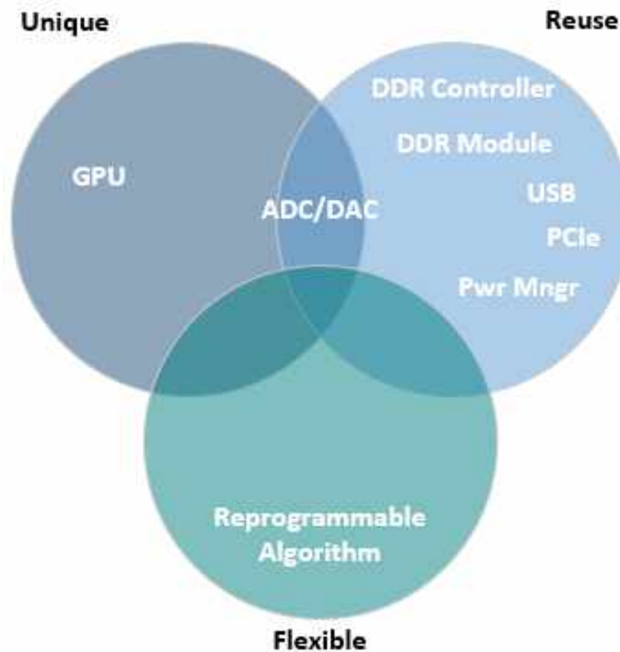
- De-aggregation represents new opportunities to reduce cost by reusing functional building blocks across multiple assemblies
- We call these die-level building blocks “Chiplets”
- Designs are no longer confined by the single choice of technology node or process as they are in monolithic design
  - 7nm FinFET processors with high speed connectivity to 90nm SiGe GPS or 16nm DDR controller or 40nm ADC/DACs
  - Older IP would no longer need to be ported to new technology nodes saving cost of porting fees, prototypes, test, and yield loss

Where To Start

- Separate the Reusable from the Unique from the Flexible

Example Design

- GPU
- Reprogrammable Algorithm
- DDR
- USB
- PCIe
- ADC/DAC
- Power Manager



Where To Start

- Identify the best technology and any groupings
- Conceptualize the Floorplan

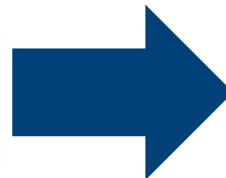
GPU
- 7nm
- Customer Specific
- Custom Dev

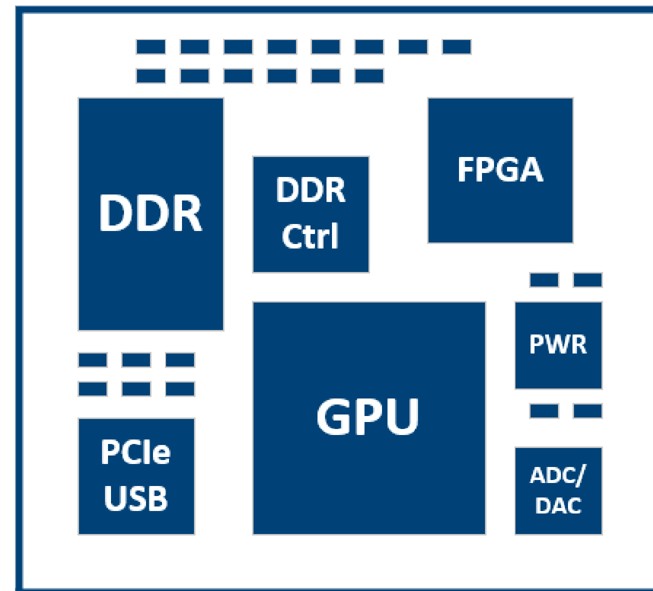
DDR
- 28nm
- Existing Die

ADC/DAC
- 45nm
- Existing Die

Interface
- 90nm
- PCIe MAC + PHY
- USB Ctrl + PHY
- Custom Dev

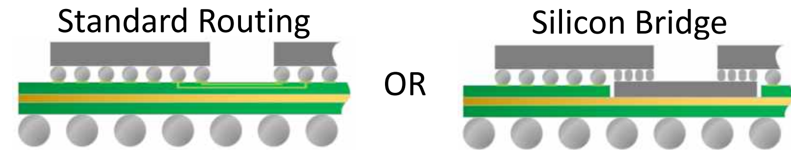
Prog Algorithm
- 28nm
- Existing FPGA

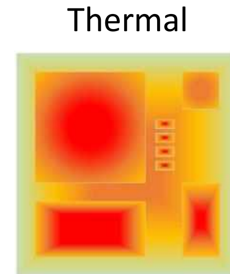


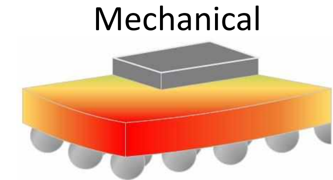


SiP Package Considerations

- Interconnectivity (Protocol, Bandwidth, Power)
- Standard substrate or silicon interposer or silicon bridge
- Signal and Power Integrity
- Thermal Integrity
- Mechanical Integrity
- Escape Routing







High Bandwidth Die to Die Interconnect

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Feature	XSR Extreme Short Reach	USR Ultra Short Reach	AIB Advanced Interface Bus
Proprietary	Yes	Yes	Open Source
Bandwidth	800Gbps / mm die edge	500Gbps / mm die edge	1Tbps / mm die edge
Distance	Up to 50mm	Up to 40mm	As close as possible
Drive off chip	Yes	No	No
Substrate	Organic, C4 @150um pitch	Organic, C4 @150um pitch	Silicon Bridge, microbump @55um pitch
Relative Power	Low Power	Very Low Power	Very Low Power
Vendor Information	Rambus, Synopsys	Kandou Bus	Intel Whitepaper

Future for SiP

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- Cost savings and competitive advantage has and will continue to be the driving force behind integration
- SiP has proven that the added complexity of package design is worth the reduction in power and reduction in board complexity
- SiP technology combined with newer low power die to die connectivity, has enabled smart de-aggregation of monolithic ASIC design into Chiplets
- Eco-System of Chiplets will drive more innovation in SiP design along with package materials and thermal solutions

Layout and Substrates

Matt Bergeron, Integra

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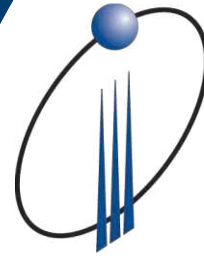

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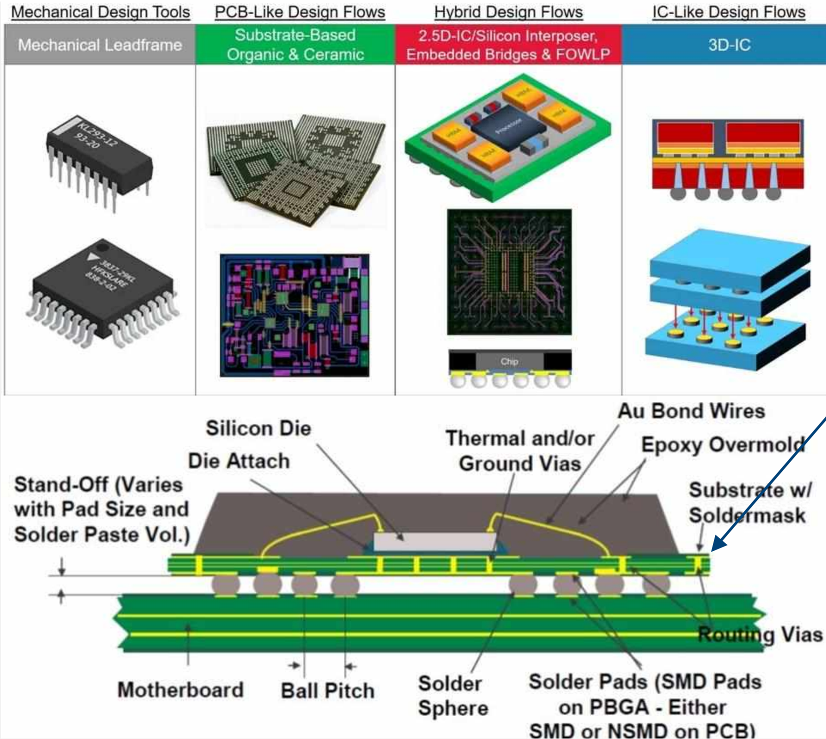
Substrates



Substrates

- Semiconductor Laminates
  - ✓ Laminate Type BT, ABF, RFBTs
  - ✓ Dk & Df
  - ✓ Subtractive, Semi-Additive, Buildup
  - ✓ L/S, Via size, capture pad, filled vias, bump on via.
  - ✓ Top Side Metallization Copper OSP, wirebondable gold, CuOSP over SOP, Gold over Copper
- Ceramics- HTCC or LTCC
- Glass

Complexity of Design is increasing

Design is Only Getting Harder…

Transistor-level	Gate-level	ASIC	SoC	Heterogenous Integration
1980	1990	2000	2010	Now
Functional	Functional	Functional	Functional	System-Level
	Timing	Timing	Timing	Functional
		Power	Power	Timing
			Reliability	Power
				Reliability
				Thermal
				Mechanical

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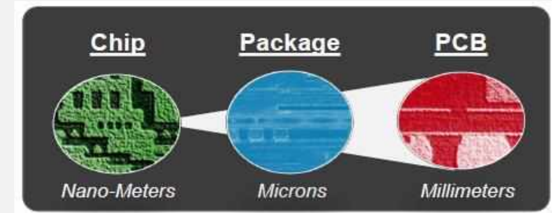
- **We see customers today using more design elements including:**
  - Signal Integrity
  - Power Integrity
  - Thermal
  - Mechanical



Key things to identify prior to starting the design

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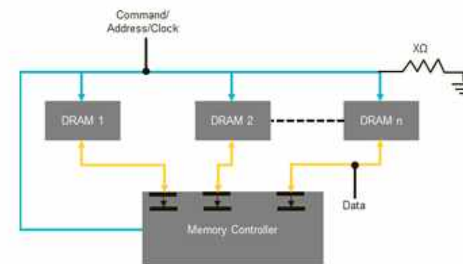
- **Target Fabricator & Assembler**
  - Know their design rules
- **Know the manufacturers of substrate materials**
  - Have the published mechanical & electrical characteristics of the materials.
- **Know the passive component (i.e. capacitors)**
  - Manufacturers, the procurement lead times and End Of Life status of various parts.
- **Know the IP vendors and clarify requirements as soon as possible in the design process and ensure direct communication with the designer to answer questions quickly.**

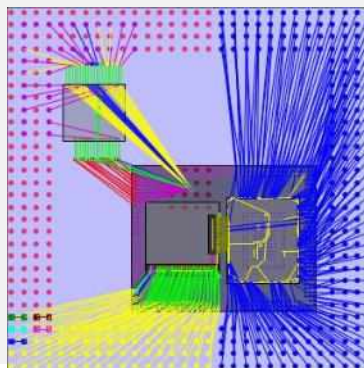
Typical Resin Properties

Resin System	ε[1MHz]	T_g [℃]	Relative cost
FR-4-epoxy	3.5-3.60	125-135	1
Polyfunctional FR-4	3.5-3.60	140-150	1-2
High Temperature one component epoxy system	3.90-4.00	170-180	3-6
Bismaleimide Triazine epoxy(BT)	3.2-3.30	180-190	3-6
Polyimide epoxy	3.5-3.6	250-260	10-20
Cyanate ester(CE)	2.80-3.50	240-250	20-30
Polyimide	3.30-3.40	>260	10-20
PTFE(melting point)	2.03-2.09	327	10-15



Key Design Issues

- **Ask for accountability of substrate design modules or pieces.**
  - Ensure that individual routes and interfaces are into **SI/PI simulation as early as possible** and present results for each of these one by one.
  - The final **SI/PI analysis should be a confirmation** run only, not part of the design process.



- **Arrange to have the design into an initial DFM/DFA review very early in the process (within the first month in the project).**
  - The first review should be done when the representative structures are all in place, meaning some routes or interfaces routed from top to bottom of stack, and the following are implemented, even if it is just a few samples:
    - Solder resist openings
    - Fiducials and markings
    - Assembly features including passive component footprints
    - Stackup fully defined.

Substrates & Design Rules

SUBSTRATE DESIGN RULES

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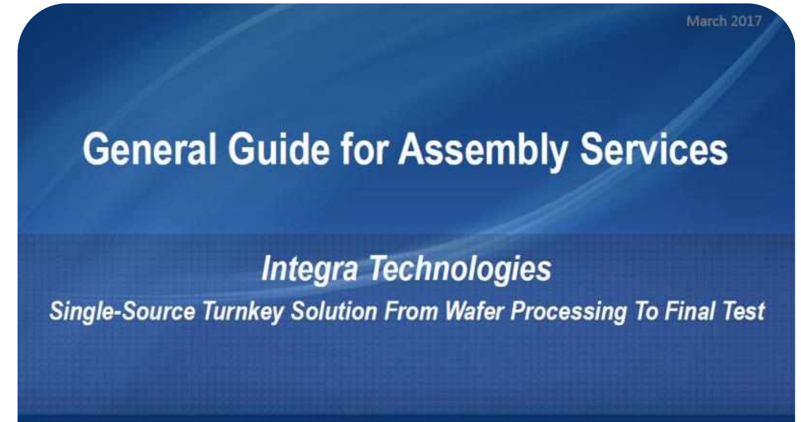


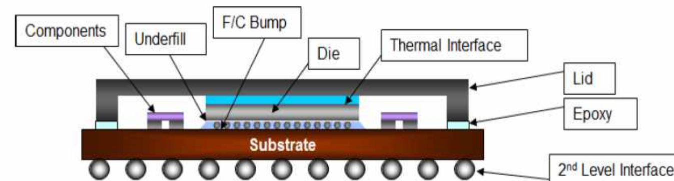
Design Rules

- Interaction between Assembly rules and Substrate rules
- Just because it works for one – doesn't mean it works for both
- Example – surface finish

FLIP CHIP FEATURES *Confidential*

SURFACE FINISH	Electroless Nickel Gold, Au : min 0.3 µm
	ENIG (Electroless Nickel Immersion Gold), Au : min 0.03 µm
	OSP (Organic Surface Preparation) : Glicoat - SMD F2(LX)
	SOP (Solder On Pad)
BUMP PAD TOP CO-PLANARITY	maximum 30 µm / Unit

Table 18. Flip Chip Surface Finish



Description	Options	Details / Experience
Substrate	Ceramic, Organic laminate, Flex Circuit, PCB	
Die	Si / SiGe / GaAs / Low K	I/O = 3 min to ~ X (bumps)
Lid / Heat Spreader	Ceramic /Aluminum / Cu	
	Lid Stiffner / No lid	
Thermal Interface	Grease / Gel / Adhesive	
Underfill	Namics 8439-1 / Other(s)	
SMT Components	Resistors, Capacitors, etc. *(high quantities are subject to review)*	Conductive epoxy / Solder
F/C Bump	Eutectic PbSn: 37/63	Pitch = 125um min
	SAC or other Pb-free	Pitch = 125um min
	High Pb: 90/10, 95/5, 97/3	Pitch = 125um min
2nd Level Interface	LGA	Pitch = 0.4 mm min
	BGA [Eutectic / Pb-free]	Pitch = 0.4 mm min
Substrate Metalization	Ceramic	Ni/Au
	Organic	Solder on Pad (SOP) / ENiG

Cost Drivers of Substrates

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Cost Drivers & Elimination of Vendors

- Lead time
- More layers
- Larger area
- Exotic connections between layers
- Higher aspect ratios
  - ✓ Small holes through thick substrate
- Special tolerances
- Smaller features
  - Lines and spaces

(Unit : µm unless noted)

ITEM			SPECIFICATIONS & TOLERANCE	
			Standard	*Special*
Core Material		Type	HL832, HL832HS, E679BR, E679F, E679FB	HL832NX *, E679FGB *
		Thickness	100, 150, 200	60, 80, 400
Cu Foil Thickness		Outer	9, 12, 18 (1/4 oz, 3/8 oz, 1/2 oz)	36 **, 70 *** (1 oz, 2 oz)
		Inner	12, 18, 36 ** (3/8 oz, 1/2 oz, 1 oz)	70 *** (2 oz)
Prepreg *(with woven glass)*		Type	GHPL830, GHPL830HS, GEA679W, GEA679F	GHPL830NX *,GEA679FG *
		Thickness	60, 100	40, 45, 50
RCF (RCC)		Thickness	50, 60, 65, 80	70, 85
Drill/Pad Size	Through Hole (Mechanical)	Outer	120/270, 150/300, 200/375, 250/450	120/250 (Core ≤ 150), 100/230 (2 L)
		Inner	150/450, 200/500	120/370, 150/400, 200/450
		Aspect Ratio	3.0	- - -
	CO_2 Laser	Outer	100/250, 130/300 (Bottom Cu ≥ 18)	80/200
		Inner	100/250	80/200
		Aspect Ratio	0.7	- - -
Layer to Layer Metal Alignment			+/- 75	+/- 50
Line/Space		Outer	50/50	35/35
		Inner	75/75	50/50
Copper Plating (Through Hole Wall) Thickness *(Electroless Cu)*			10 +/- 5, 15 +/- 5, 20 +/-5	25 +/- 5, 30 +/- 5, 35 +/- 5
Plugging Ink		Type	HBI200, AE1125 *, THP100DX1 *	AE3030
Solder Resist		Type	AUS5, AUS7, AUS308 *,AUS310 *	AUS402 *, SR7200G *, S-500
		Thickness	15 +/- 10, 20 +/- 10, 25 +/- 10	30 +/- 10, 35 +/- 10 (Double Coating)
		Opening Size	150 (minimum)	90 **** (minimum)
		Min. Width	100 (minimum)	80 (minimum)
		Registration	+/- 50	+/- 37.5
Surface Finish		Type	Soft Bondable Au, Hard Au *****	OSP, SOP, Direct Au (without Ni) ******
		Plating	Electrolytic, Electroless	- - -
Plating Thickness		Nickel	3, 5 (minimum)	- - -
		Gold	0.3, 0.5 (minimum), 0.03 (ENIG)	- - -
Capped Via Finished		Line Width	60 +/- 25	50 +/- 25
		Cu Thickness	25 +/- 8	21 +/- 8
Board Twist / Bow			1.0 % per strip (maximum)	0.5 % per strip (maximum)
Board Parallelity			+/- 100	- - -
Tooling Hole to Tooling Hole (min: 1mm)			+/- 50 (0 ~ 200 mm)	- - -
Tooling Hole to Strip Edge			+/- 50 (0 ~ 50 mm)	- - -

* Halogen Free Type
** Line / Space ≥ 100 / 100 mm
*** Line / Space ≥ 150 / 150 µm
**** Solder Resist Thickness : 10 µm
***** Electrolytic Plating only
****** Electroless Immersion Plating only

SiP – Assembly Considerations

Ken Halsey, Integra

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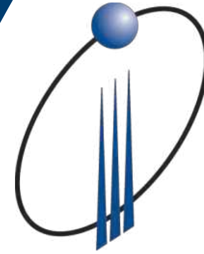
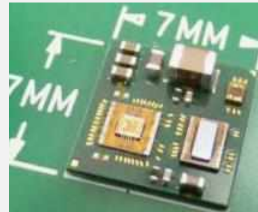


Assembly Consideration for SiP

- Die I/O Count, Component Placement, PCB Overall Size, along with other mechanical considerations
- Some trade-offs and considerations:
  - Separation of thermally sensitive die
    - Memory limits maximum junction temperature to 85˚C
    - Processor and logic can run up to ~100˚C
    - Power supply parts may run up to 125˚C
  - Size and shape of the board
  - Components & Passives in SiP – solder attach hierarchy
    - Need inside vs. on board
    - Size & Location

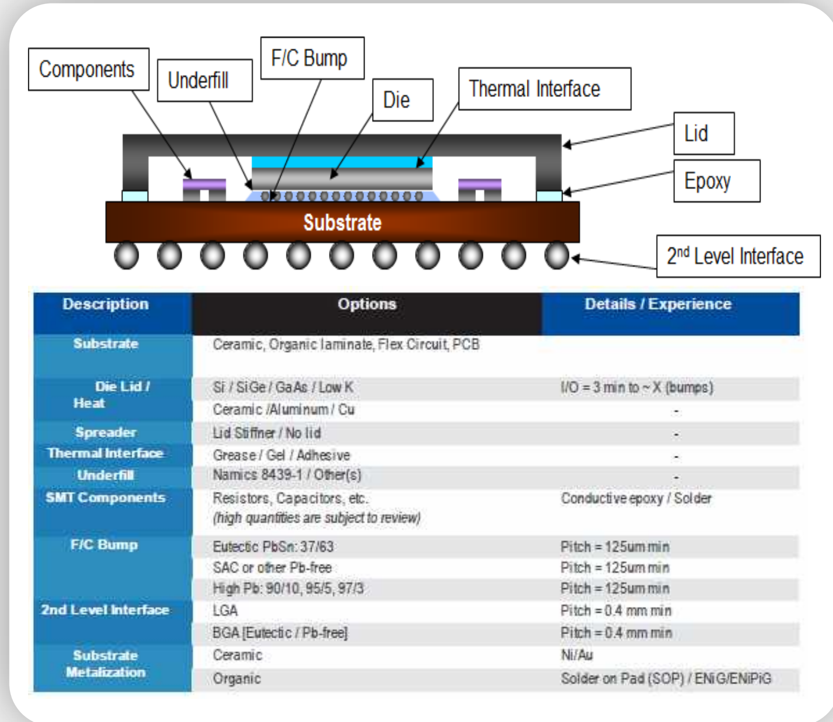


- Other discussions and solutions:
  - Package-on-Package (PoP) for DDR
  - Package-in-Package (PiP)
  - Increases overall package thickness
  - Mount passives on backside of substrate
    - Requires ball depopulation and special fixturing
  - Wire bonding capillary requires spacing for manufacturability
  - Use an external DDR/FLASH combo package, mounted on the backside of the motherboard
    - Drives I/O count and routing out of the package
  - Stack capacitors of same form-factor
  - Stacking of Die – Flip Chip and Wire Bond mix
  - Flip Chip die may require underfill
    - Room to underfill and “Keep Out Zones”

General Design Rules

Assembly

- Format: Array or single unit assembly (larger SiPs)
- Underfill keep-out zone
- Wire bond keep-out zone
- Component spacing
- Front side, backside components attachment
- Solder hierarchy: Eutectic vs. Pb Free
- Shielding methods: metal lids
- Encapsulation: Transfer mold, Dam & Fill, metal or ceramic lids



Description	Options	Details / Experience
Substrate	Ceramic, Organic laminate, Flex Circuit, PCB	
Die Lid / Heat	Si / SiGe / GaAs / Low K	I/O = 3 min to ~ X (bumps)
	Ceramic /Aluminum / Cu	-
Spreader	Lid Stiffner / No lid	-
Thermal Interface	Grease / Gel / Adhesive	-
Underfill	Namics 8439-1 / Other(s)	-
SMT Components	Resistors, Capacitors, etc. *(high quantities are subject to review)*	Conductive epoxy / Solder
F/C Bump	Eutectic PbSn: 37/63	Pitch = 125um min
	SAC or other Pb-free	Pitch = 125um min
	High Pb: 90/10, 95/5, 97/3	Pitch = 125um min
2nd Level Interface	LGA	Pitch = 0.4 mm min
	BGA [Eutectic / Pb-free]	Pitch = 0.4 mm min
Substrate Metalization	Ceramic	Ni/Au
	Organic	Solder on Pad (SOP) / ENIG/ENiPiG

Stacking Die – Space Saving

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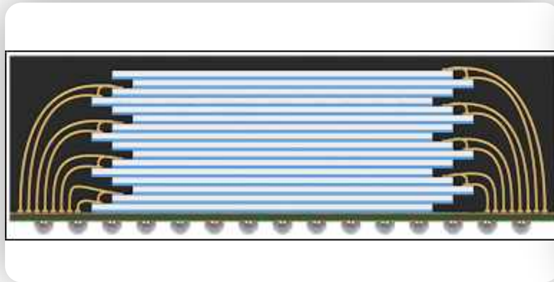
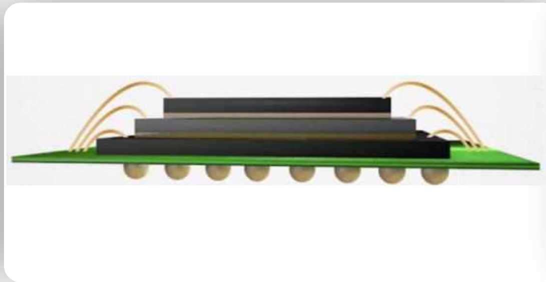
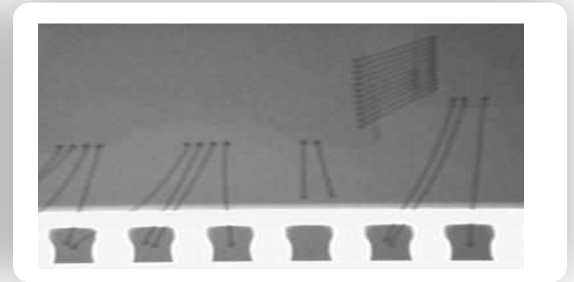
- Die Stacking is the process of mounting multiple chips on top of each other within a single semiconductor package
  - Die stacking, which is also known as 'chip stacking', significantly increases the amount of silicon chip area that can be housed within a single package of a given footprint
  - Aside from space savings, die stacking also results in better electrical performance of the device, since the shorter routing of interconnections between circuits results in faster signal propagation and reduction in noise and cross-talk
- There are a number of approaches – some blended with flip chip
  - Same size die, stair case stack, pyramid, die to die bonding







Note: There are other considerations such a true 3D stacking that are not discussed here

Die Considerations – Making the Right Engineering Tradeoffs

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Die Considerations - Die Count and Area will drive overall SiP/MCM size

- Die Attach Methods
  - Epoxy, DAF, silver glass, eutectic
- Interconnect Technologies
  - Wire bond type & diameter
    - ✓ Gold, Copper, Aluminum (power products)
    - ✓ Wire bond assembly rules
    - ✓ Surface metallization
  - Flip Chip
    - ✓ Ball Pitch, Count, Diameter
    - ✓ Bump composition
- Other Considerations
  - Thickness of die, Flip Chip or Wire bond rules, substrate line and spacing
  - I/O Configuration and location – is it routable?
  - Power Dissipation

Package Constraints

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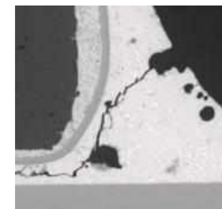
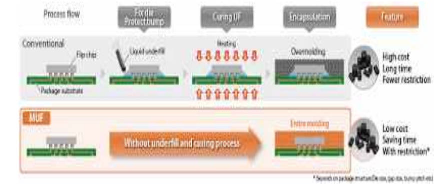
Package Requirements / Constraints

- Overall maximum height, X-Y dimension, PCB thickness
- Die count and sizes
- SiP components and locations
- Packaged parts mounted on the SiP
- Warpage
- Thermal constraints
- Solder Hierarchy & solder joint integrate
- Environmental
  - MSL, fine / gross leak, HTOL, etc.



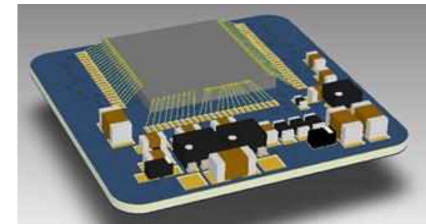
Encapsulation Considerations

- **Open Cavity**
  - Great RF insulation (especially when coupled with ground plane)
  - Less process steps
  - Access to various components for rework
- **Transfer Mold / Glob Top / Dam & Fill**
  - In some cases can be lower cost
  - Can interact poorly with SiP components such as plastic parts
  - Difficult to trouble shoot
- **Flip Chip**
  - Underfill/No Underfill?
  - Bump considerations in Mil/Aero applications (tin whiskers)
  - Reworkability
  - Vision concerns



Glob Top Encapsulation Process and Result:

Dam & Fill (Frame & Fill) Encapsulation Process and Result:



Testing and Qualification

Sultan Lilani, Integra

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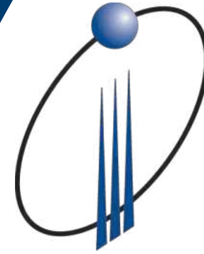

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General Testing Considerations

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SiP Test Considerations

- Evaluate the SiP Design and consider if it should be classified as
  - ✓Application Specific IC
  - ✓Hybrid IC
- SiP by definition will have complex functional test requirements
- Plan on spending a considerable amount of time on the testing plan
  - ✓Testing the appropriate parts of each portion of the SiP
- Characterization and Production plans may vary radically (as with normal products)

SiP Electrical Testing

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Keys to cost-effective electrical test solutions:

- Early engagement with SIP designers to ensure design incorporates features for appropriate test coverage. These include access points, test modes etc.
- Leverage SCAN Chain and JTAG solutions using digital vectors from simulations.
- Focus on verifying connectivity of SIP components and interactions between SIP components, not necessarily performance of each parameter of individual SIP components
- Consider temperature performance of entire SiP due to the limitation of temperature performance of each component of the SiP
  - ✓ One component of the SiP may limit the operating temperature of entire SiP
- Test to usage conditions like speed and temperature extremes.

Overall Recommended Electrical Test Methodology

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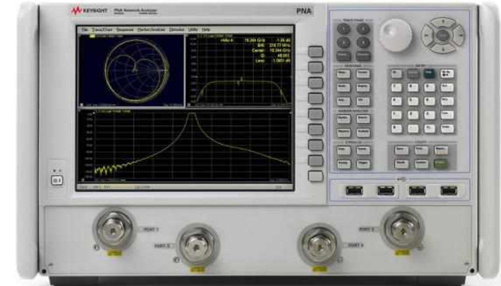
Test the Device the Specified Performance Characteristics

- Functional at-speed
  - ✓ Application speed at a minimum may not need spec speed
  - ✓ Test frequency is a major tester cost driver
- Comprehensive functional testing
  - ✓ Test all device functionality
  - ✓ Fault grading is not possible
    - ➢ Only the manufacturer has device modeling capability
- Test key AC parameters
  - ✓ Key parameters are usually referenced to device clocks
    - ➢ Propagation delay
    - ➢ Setup and hold times
  - ✓ Use go-no-go testing to cover most AC parameters
    - ➢ Tested over the entire functional pattern
  - ✓ Selected AC characterization measurements can be made
- DC measurements to the full specified limits
  - ✓ Attempt to test 25C parameters at extended temperatures
  - ✓ Limit adjustments may be required after testing
- Select the appropriate tester
  - ✓ No one tester can effectively test all technologies

Electrical Testing equipment

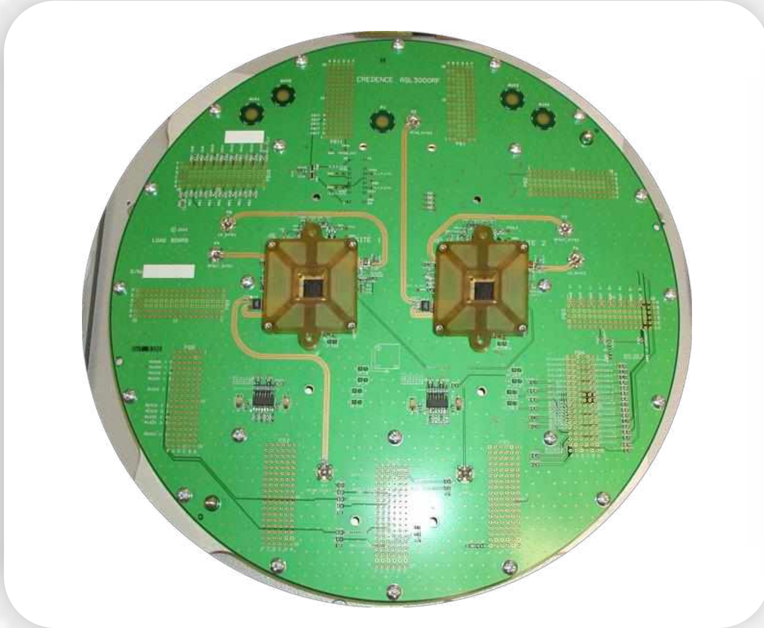
Integrate industry standard Automated Test Equipment (ATE) with auxiliary equipment to augment capabilities.

Examples: Credence ASL3000 + 50GHz RF Network Analyzer



Electrical Testing equipment

- Implement parallel test solutions and automated handling of product during testing when possible to keep cost of test low.



SiP Qualification Considerations

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- Evaluate the SiP Design and decide if it should be considered:
  - Application Specific IC
  - Hybrid IC
  - Look for Mil-PRF-38534 (multiple die)and Mil-PRF-38535 for screening and qualification guidance
- Most SiPs use non-packaged die
- Consider material characteristic of the SiP product (example: organic substrate vs. ceramic substrate) – CT and Environment consideration
- Consider performing construction analysis and pre-screen DPA to understand the manufacturing technology

Mil PRF 38534 Key Sections

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1. SCOPE

1.1 Scope. This specification establishes the general performance requirements for hybrid microcircuits, multi-chip modules (MCM) and similar devices, and the verification requirements for ensuring that these devices meet the applicable performance requirements. Verification is accomplished through the use of one of two quality programs (Appendix A). The main body of this specification describes the performance requirements and the requirements for obtaining a Qualified Manufacturers List (QML) listing. The appendices of this specification are intended for guidance to aid a manufacturer in developing their verification program. Detail requirements, specific characteristics, and other provisions that are sensitive to the particular intended use should be specified in the applicable device acquisition specification.

Appendix A defines the quality management program that may be implemented by the manufacturer. Appendix A includes an option to use a quality review board concept, hereafter referred to as the Technology Review Board (TRB) in this document, which may be used to modify the generic verification, design, and construction criteria provided in this specification. Appendix B is not currently being used. Appendix C defines generic performance verifications. These verifications consist of a series of tests and inspections which may be used to verify the performance of devices. They may be used as is or modified as allowed by this specification. Appendix D defines generic performance verifications for non-hermetic device technologies. Appendix E defines generic design and construction criteria relative to this technology, including rework limitations and major change testing guidance. Appendix F provides statistical sampling procedures. Appendix G provides the requirements for Radiation Hardness Assurance (RHA).

Mil PRF 38534 Key Sections

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1.3 Classification. Seven quality assurance levels are provided for in this specification. Four of these classes, in highest to lowest order, are K, H, G and D, as defined below. The fifth class is Class E, the quality level associated with a Class E device is defined by the acquisition document. The sixth and seventh classes are L and F for non-hermetic devices, with Class L being the higher quality assurance level.

1.3.1 Class K. Class K is the highest reliability level provided for in this specification. It is intended for space applications.

1.3.2 Class H. Class H is the standard military quality level.

1.3.3 Class G. Class G is a lowered confidence version of the standard military quality level (H) with QML listing in accordance with 4.5.2.2, a possibly lower temperature range (-40ºC to +85ºC), a manufacturer guaranteed capability to meet the Class H conformance inspection and periodic inspection testing, and a vendor specified incoming test flow. The device will meet the Class H requirements for in-process inspections and screening.

1.3.4 Class D. Class D is a vendor specified quality level available to this specification. This is a possibly lower temperature range (0ºC to +70ºC) part with a vendor specified test flow available from a QML listed manufacturer.

1.3.5 Class E. Class E designates devices which are based upon one of the other classes (L, K, H, G, or F) with exceptions taken to the requirements of that class. These exceptions are specified in the device specification, therefore the device specification should be carefully reviewed by the user to ensure that the exceptions taken will not adversely affect the performance of the system.

1.3.6 Class L. Class L is the highest quality class for non-hermetic devices.

1.3.7 Class F. Class F is the standard quality class for non-hermetic devices.

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MIL-PRF-38534L

APPENDIX C

* TABLE C-VI. Package evaluation requirements.

Subgroup	Class		Test	Specification or Standard			Quantity (accept number)	Reference paragraph
	K	H			Method	Condition		
1	X	X	Physical dimensions	MIL-STD-883	2016	Acquisition document	3 (0)	C.3.8.3
2	X	X	Visual Inspection 1/	MIL-STD-883	2009		100 percent	C.3.8.4
	X	X	Device Finish 2/	MIL-PRF-38534	N/A	Acquisition document	3 (0)	C.3.8.4
3	X	X	Thermal shock	MIL-STD-883	1011	C	3 (0)	C.3.8.2 and C.3.8.5
	X	X	High temperature bake	MIL-STD-883	1008	1 hour at +150°C		
	X	X	Lead integrity	MIL-STD-883	2004 2028	A1 (braze attached leads, 3 lead minimum). B1 (rigid leads and terminals only) B2 (lead fatigue) D (pad adhesion of leadless chip carriers) E (plating integrity of flexible and semi-flexible lead, 3 leads minimum).		
					2028 3/	Pin grid array leads		
	X	X	Seal		1014	A4 Unlidded cases		
4	X	X	Metal package isolation		1003	600 V dc 100 nA maximum	3 (0)	C.3.8.6
5	X	X	Solderability	MIL-STD-883	2003	Soldering temperature +245°C ± 5°C	3 (0)	C.3.8.7
6	X	X	Salt atmosphere		1009	A	3 (0)	C.3.8.8

1/ JESD 9 may be used as a guideline to enhance MIL-STD-883, method 2009.
2/ Using a recognized methodology (e.g. EDS, XRF) verify that finishes containing tin (Sn) have a minimum of 3 percent lead (Pb) by weight per MIL-PRF-38534 (JESD213 is also acceptable). Not required on packages with gold plated bodies and pins.
3/ B1 of method 2004 can be used as an option.

THANK YOU

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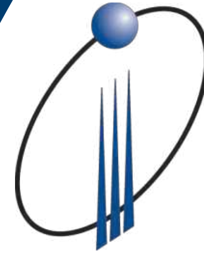

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