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School *of* Engineering

NEPP ETW 2023

Single-Event Effects in Silicon Carbide High Voltage Power Devices for Lunar Exploration

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NASA 2020 LuSTR SiC Program Call for Proposals

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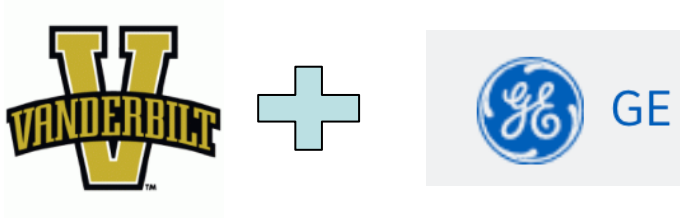
Electrical Performance:

- **SEE-tolerant SiC power diodes: Minimum 1200 V, 40 A, with maximum recovery time of 40 ns**
- **SEE-tolerant SiC power transistors: Normally off (enhancement mode), minimum 600 V, 40 A, Rds_on < 24 mOhms while preserving low switching losses.**

Radiation Goal:

- **No heavy-ion induced permanent destructive effects upon irradiation while in blocking configuration (in powered reverse-bias/off state) with ions having a silicon-equivalent surface incident linear energy transfer (LET) of 40 MeV-cm^2/mg of sufficient energy to maintain a rising LET level throughout the epitaxial layer(s).**

- **Application Goal: Micro-Grid on the moon at 1 kV DC**



Power Device Technologies – Why SiC?

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ADVANCED POWER TECHNOLOGY®

APT1001RSVR

1000V 11A 1.000Ω

POWER MOS V®

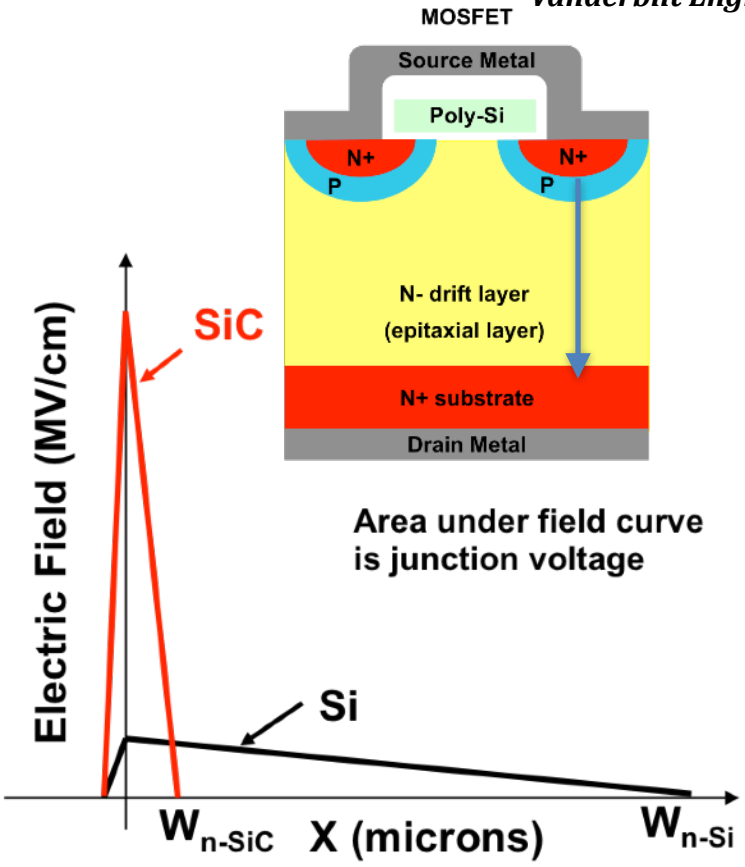
Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V®

CREE

C3M0065100J

Silicon Carbide Power MOS
C3M™ MOSFET Technology
N-Channel Enhancement Mode

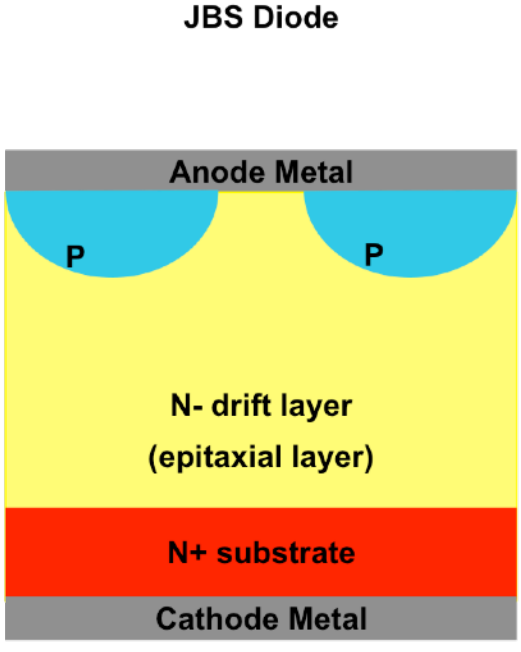
V_{DS}	1000 V
$I_{D\ @\ 25°C}$	32 A
$R_{DS(on)}$	65 mΩ

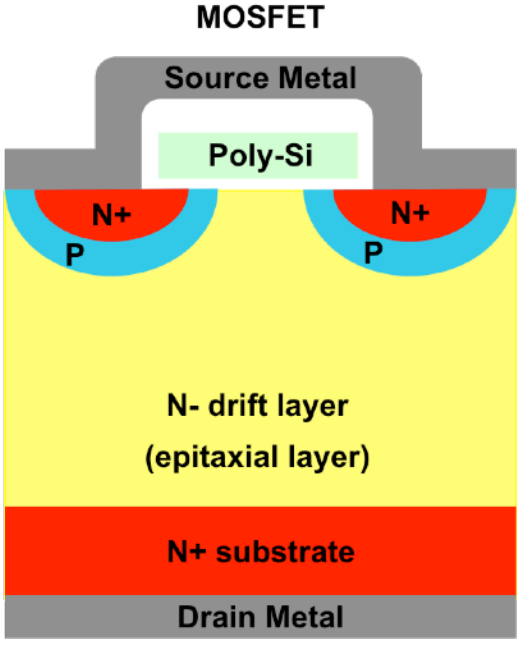


On-resistance of SiC ~ 6% of Silicon Device
Much better choice than Si for high voltage

Silicon Carbide Vertical Power Devices

- Vertical power device
  - Suitable for diodes and MOSFETs
  - Vertical current flow
  - Performance influenced by epitaxial region resistance

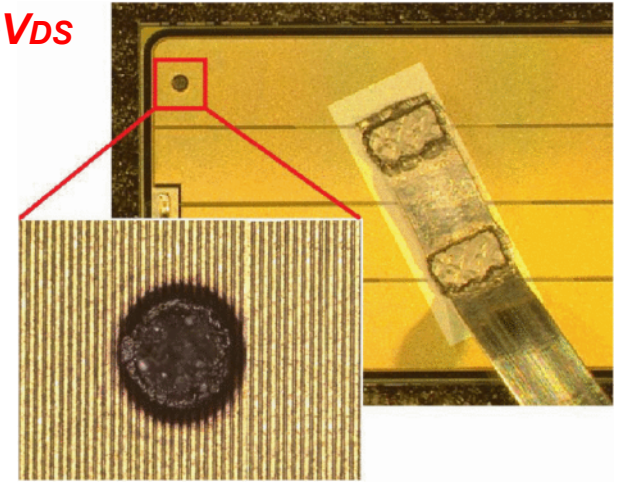




Radiation Effects in Power Devices

- Total Ionizing Dose (TID) – charge trapped in insulating layers
  - Parametric shifts in device electrical characteristics (i.e. threshold voltage)
- Single Event Effects – ions deposit charge in active device regions
  - Transient current/voltage pulses
  - ***Permanent increases in leakage currents with each ion***
  - ***Single event burnout (SEB) around half of rated-V_{DS}***

From: G. Consentino et. al, 2014 IEEE Applied Power Electronics Conference and Exposition



Space applications: Catastrophic failure is not an option!

Single-Event Leakage Current (SELC)

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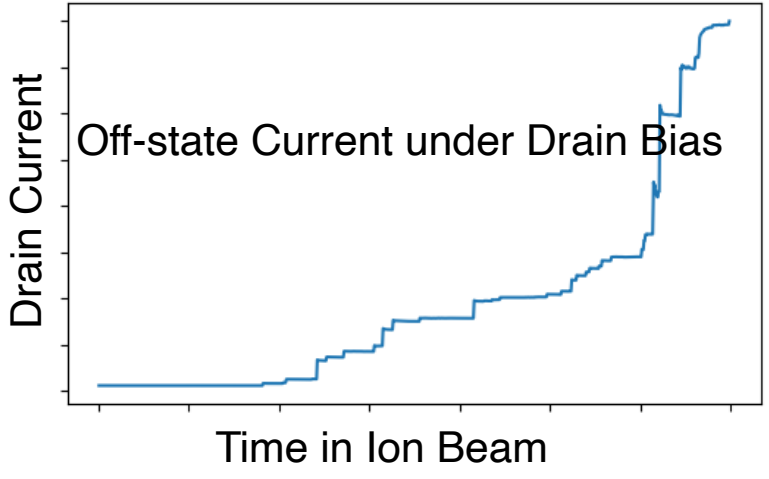
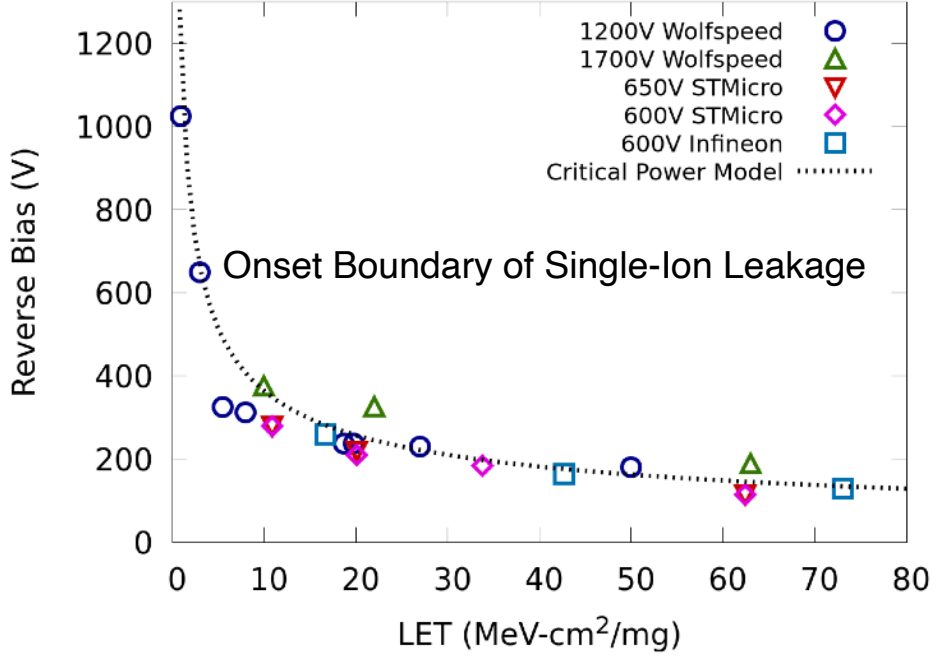
- SiC devices show step changes in off-state current for single ion strikes
- SiC devices show onset of the effect at reverse biases ~20% of rated breakdown voltage.
- Leakage independent of manufacturer or breakdown voltage (epi depth)
- Large enough for parametric failure



R.A. Johnson, et al, IEEE TNS, Jan. 2020



SEB in 1200 V SiC Vertical DMOS and JBS Schottky

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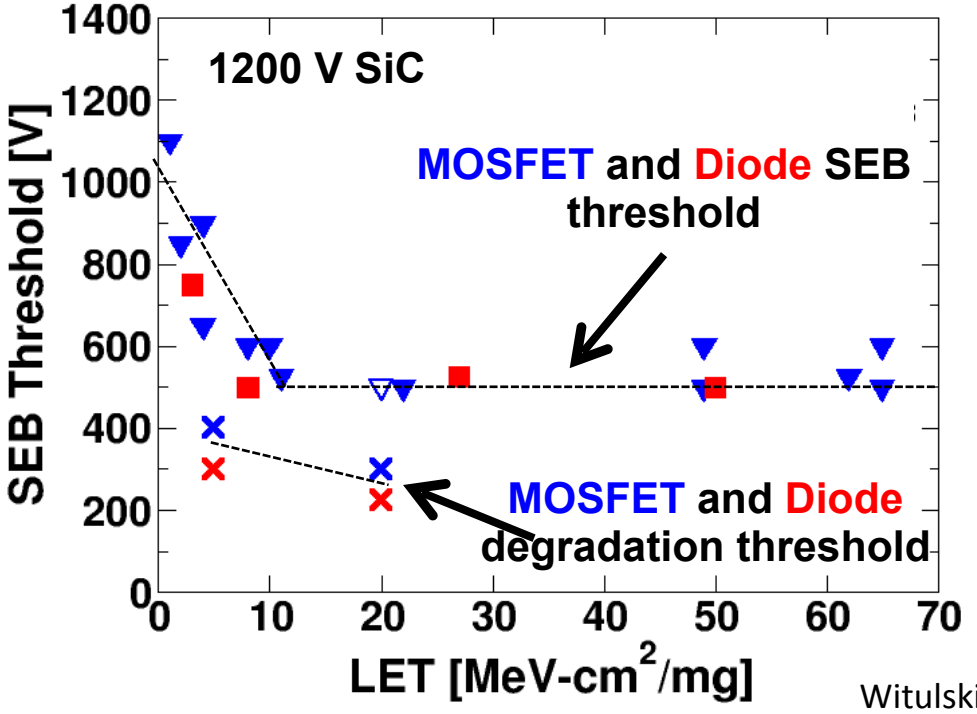

Heavy ion-induced SEB and degradation data for SiC MOSFETs and diodes from:
Mizuta 2014
Lauenstein 2015 (LBNL)
Witulski 2018 (RADEF and TAMU)
"Hockey Stick" curve

- Note that SiC and diodes have the same SEB Bias-LET boundary
- Indicates a similar SEB mechanism

Witulski, et al, IEEE TNS, 2018

Heavy ion data suggests common mechanism(s) responsible for SEB and degradation in SiC

Ion-Induced Current Densities and Re-Distribution of Electric Field

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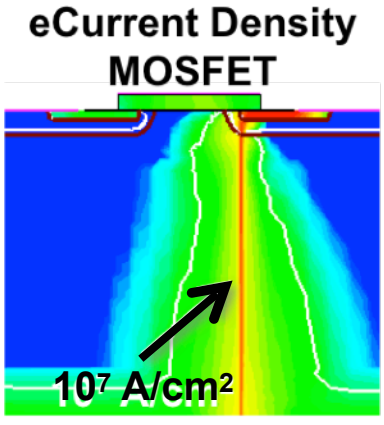
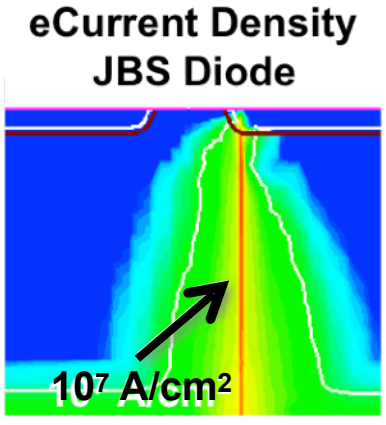
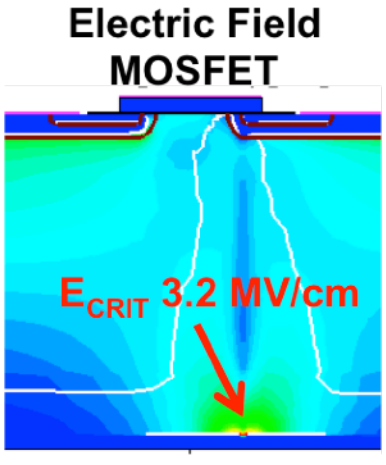
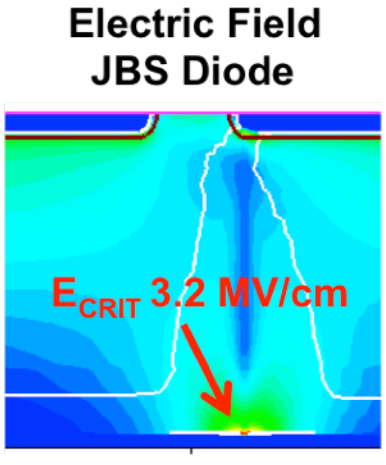
3D TCAD heavy ion simulation of 1200 V SiC

- **LET = 10 MeV-cm²/mg @ 500 V**
- **Short circuit from high carrier density**
- **Re-distribution of electric field**
- **Maximum field goes from 2 to 3.2 MV/cm**









Power density is extremely high along strike path, high current density and high electric field

$$Pd = J \cdot E$$

D.R. Ball et al, IEEE TNS, Vol. 67, 2020

J. McPherson et al, IEEE TNS Vol. 68, 2021

Goal: Design Radiation-Tolerant Diode/MOSFET

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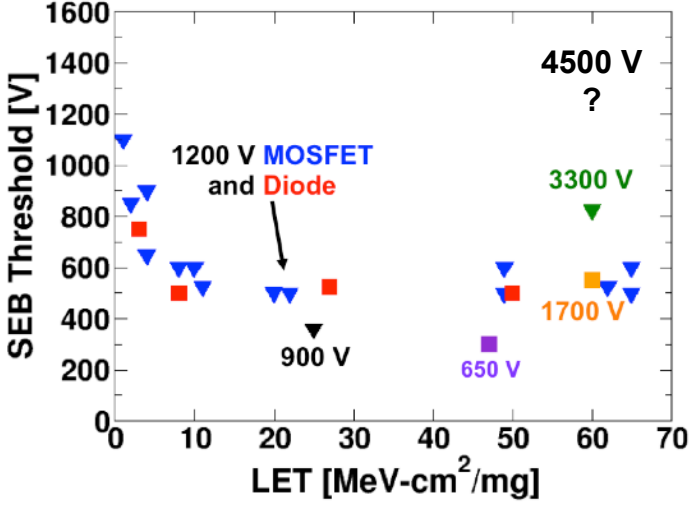
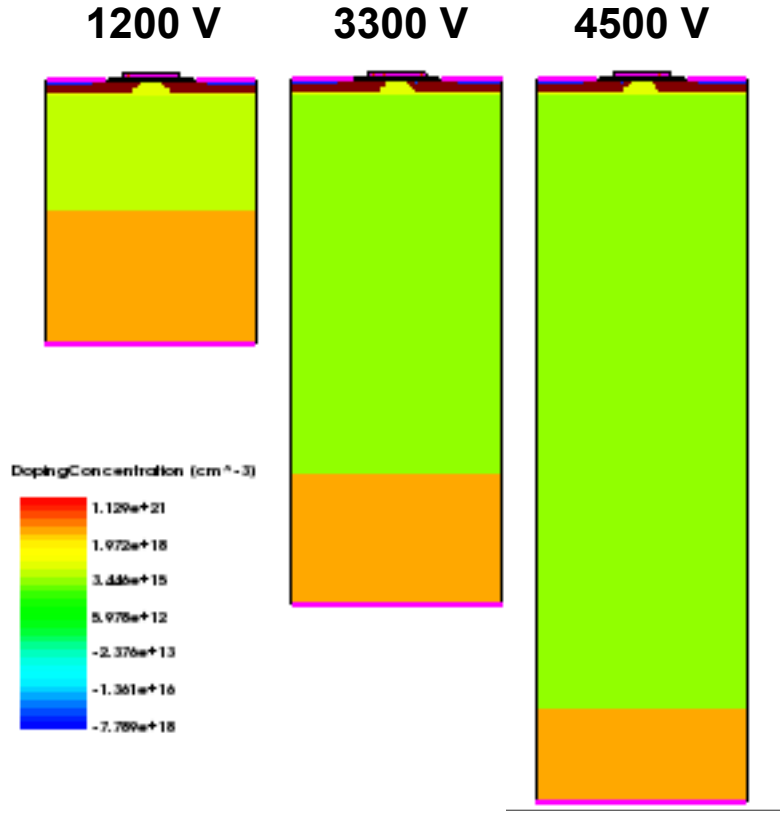
- VU and GE design device intended to survive catastrophic SEB
- 3D TCAD heavy ion sensitivity study – VU
  - Increase epi thickness
  - Decrease epi doping
  - Effective increase in voltage rating
  - Note: 3300 V device shows SEB @ 850V





Ion-Induced Electric Field Redistibution

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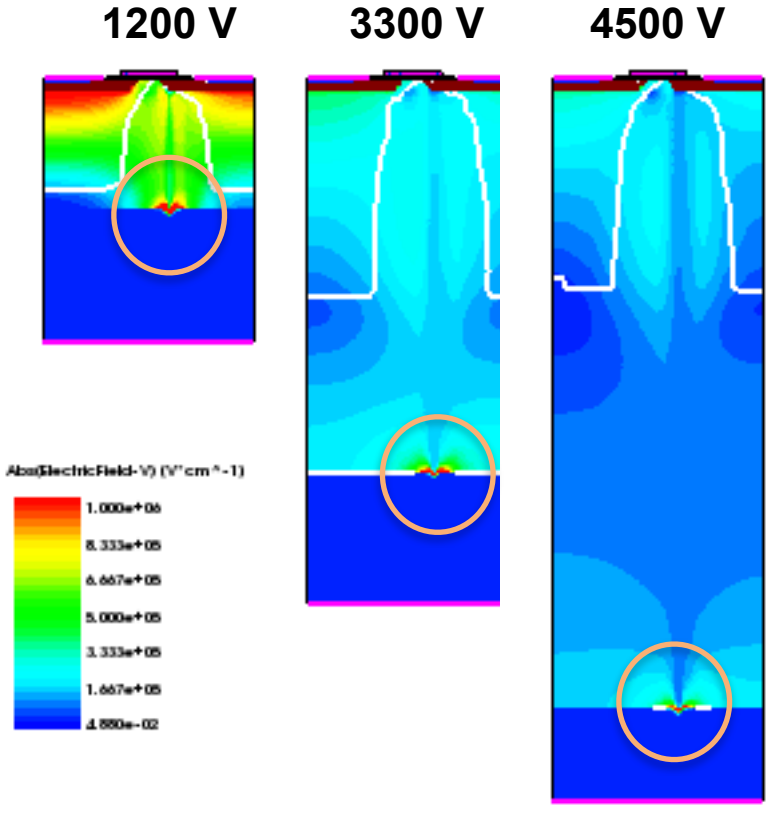
3D TCAD heavy ion simulation of SiC MOSFET variants

- **LET = 60 MeV-cm²/mg @ 500 V**
- **3300 V and 4500 V device show significantly lower electric fields compared to the 1200 V device**



Fabrication and Test Approach Plan for Baseline 3.3 kV Devices

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Deliver Standard Devices

#	Device Type		Project Scope
1	Standard planar MOSFET (1.7kV OR 1.2kV)	Test & establish baseline	Radhard design and fabrication
2	Standard Schottky diode 3.3kV	Test & establish baseline	Radhard design and fabrication
3	Charge-balanced diode 3kV	Test & establish baseline	
4	Charge-balanced MOSFET 3kV	Test & establish baseline	

Design & Fabricate RadHard Devices

TECHNICAL INSIGHTS
- Epi region affects SEB and SELC
- Metal-SiC interface may affect leakage
- Try to keep good electrical performance

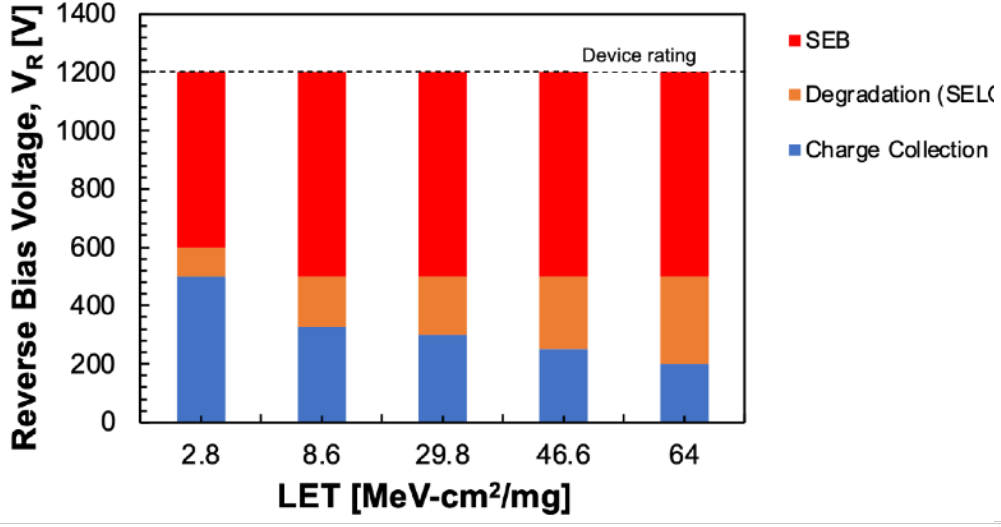
DESIGN, FAB, TEST, PACKAGE
- Vary epi thickness and doping to lower peak electric fields
- Some devices have metal windows
- ~ 10 variant devices
- Parallel lots: diodes (~4 months) and MOSFETs (~6months)
- Post-fab tests: Vth, $R_{DS(on)}$, Vdss
- Parylene coating of open-can packages
- Six wafers each of diodes and MOSFETs

TECHNICAL CHALLENGES
- Material quality issues including defects, impurities → test bare wafers
- Device design that ensure both electrical performance and rad-tolerance

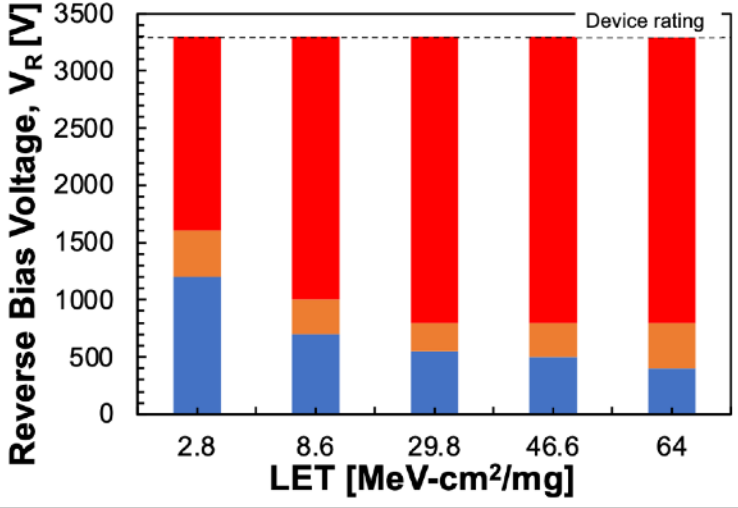
Apply insights on radiation impact on SiC to implement SEE tolerant power devices

Comparison 1200 V and 3300 V SiC Vertical Diode Single Event Burnout and Degradation Boundaries

1200 V SIC Diodes



3300 V Diodes



Absolute increase of SEB Boundary by about 300 V, but not proportional increase

More test results to be reported in NSREC and RADECS 2023

A. Sengupta, et al, “Single-Event Effects in 3.3 kV SiC Power Devices during Heavy-Ion Irradiation,” SEE/MAPLD, 2023

GE SiC MOSFET Fab Schedule

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			FAB																												
			Substrate receipt and evaluation	Start Lot	Substrate doping adjustment (Implant)	Align Mark	Pwell (Implant)	Spacer	N+ (Implant)	P+ (Implant)	JTE (Implant)	Implant Activation	Field Oxide	Gate Dep	Gate Pattern	ILD	Ohmic	Back Side Ohmic & RTA	Gate Pad Via	Pad Metal	Passivation	Back Metal	Polyimide	Complete	Gate Di-electric tests	Device Parametric Tests	Resistivity measurements	Data Analysis and Yield	Dicing	Pick-n-Place	Die Packaging	Parylene Coating
			5%	6%	11%	14%	20%	24%	29%	34%	39%	44%	49%	54%	59%	64%	69%	74%	79%	84%	89%	91%	95%	100%								
Lot	Status	Spec																														
DX353	Fab	4.5 KV MOSFET	Completed June-9-2022	10-Jun-22	Completed June-22-2022	Completed 27-June-2022	Completed July-12-2022	Completed July-9-2022	Completed Aug-8-2022	Completed Aug-29-2022	Completed Dec-02-2022	Completed Dec-07-2022	Completed Dec-16-2022	Completed Dec-22-2022	Completed Jan-06-2022	Completed Jan-11-2023	Completed - March 29-2023	Completed	Completed	Completed	Completed	Completed	Completed	Completed June-1-2023	In Progress							

GE MOSFET Variants recently completed the fab run and is in wafer test

GE SiC Junction-Barrier-Schottky (JBS) Diodes

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			FAB																			
			Substrate receipt and evaluation	Start Lot	Align Mark	JBS (Implant)	JTE (Implant)	Implant Activation	Field Oxide	Backside ohmic metal	Frontside Via contact Pattern	Frontside Via Etch Completion	Schottky Metal Deposition	Frontside Schottky Metal Patter	Passivation	Back Metal	Polyimide	Complete	Device Parametric Tests	Resistivity measurements	Data Analysis and Yield	Dicing	Pick-n-Place	Die Packaging	Parylene Coating
			5%	6%	10%	15%	35%	40%	45%	60%	65%	70%	75%	80%	85%	90%	95%	100%							
Lot	Status	Spec																							
WX039	Fab	4.5 KV JBS	Completed June-9-2022	16-Jun-22	Completed 21-June-202	Completed Jul-22-2022	Completed Aug-2-2022	Completed Aug-5-2022	Completed Sept 13-22	Completed Sept 27-22	Completed Sept 30-22	Completed Oct4 -22	Completed Oct 6-22	Completed Oct 12-22	Completed Oct 17-22	Completed Oct 20-22	Completed Oct 24, 2022	Completed Oct 25, 2022	Completed Jan 6, 2023	Completed Jan 6, 2023	Completed Jan 11, 2023	Completed Jan-26-2023	Completed Feb-16-2023	Completed May 12, 202	Completed May-23, 202

- Fabrication, packaging, testing of new SiC JBS diodes complete
- Ion-beam-ready devices delivered to Vanderbilt late May
- Planning for heavy ion test week of July 10th

Diode Variants

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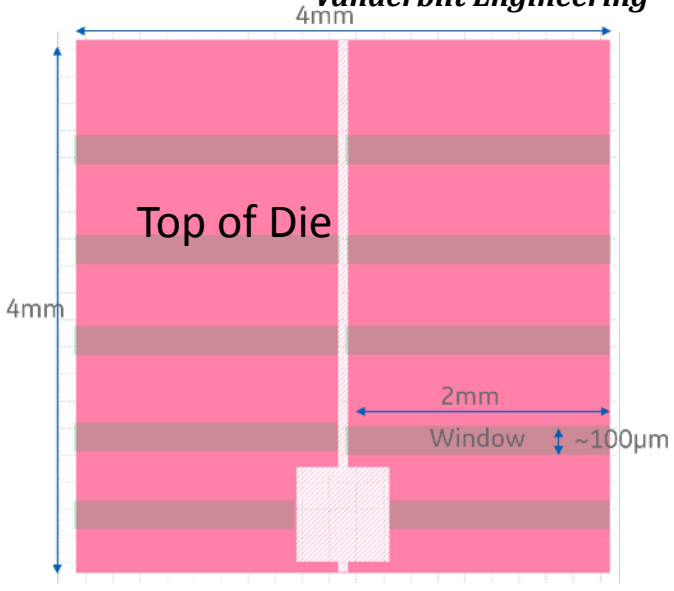
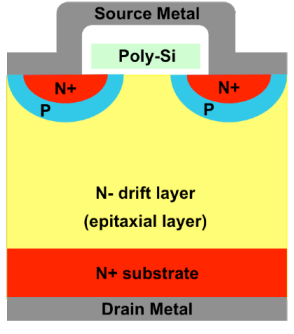
Windowed devices
- Metallization leaves fraction of die uncovered
- Covered with conductive layer like silicide
- Allows for optical testing
- Test metal-semiconductor hypothesis for SELC



Ten JBS diode variants
- Variations in window coverage
- Variations in doping
- Variations in packaging for testing

Cross-section
Of device



Vanderbilt Nano-Photonics Laboratory

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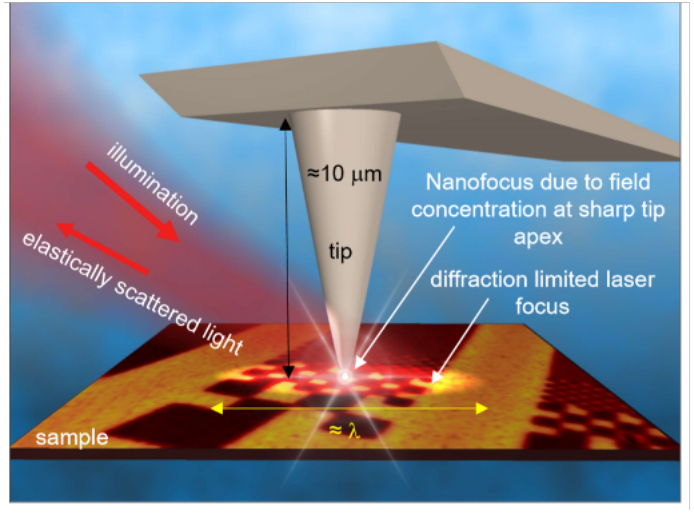
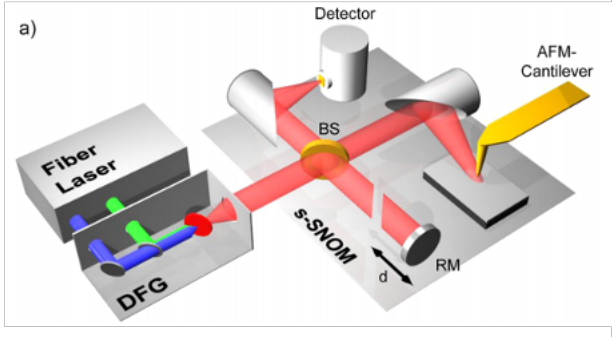
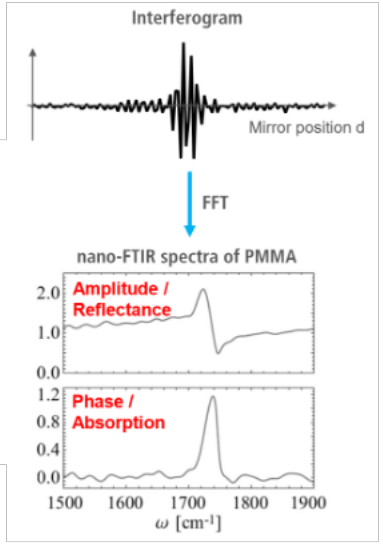
- Dr. Joshua Caldwell in Mechanical Engineering and Materials Science
- s-SNOM (scattering-type scanning near-field optical microscopy): detects light scattered by nanometer scale regions directly under the AFM tip.
- A compelling technique for studying nanoscale light-matter interactions with spatial resolution set by AFM tip.
- Useful for studying changes in crystal structure induced by ion beam radiation







nano-FTIR

Summary: Program Timeline

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June 2022 Test GE Baseline 3.3 kV devices at TAMU Ion Accelerator June 2022
July 2022 New JBS diodes and MOSFETs launched on GE Fab lines
Dec 2022 JBS Diodes exit Fab
Jan. 2023 Electrical testing of diodes
Mar. 2023 Open-cavity TO 257 packaging/Parylene coating
Apr. 2023 Delivery of JBS diodes to Vanderbilt
June 2023 Heavy Ion test of diodes at TAMU
June 2023 SiC MOSFETs exit Fab
July 2023 Electrical Testing
Aug. 2023 Packaging/Parylene
Sep. 2023 Heavy ion test of MOSFETs at TAMU
Dec. 2023 Final Results presented at LSIC Fall Workshop