



Qualcomm Snapdragon and the NESC Guidelines

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Overview

- Goal – Infuse 7nm Snapdragon automotive generation devices into JPL Class B missions
- Approach:
 1. Use the NESC Recommendations on the Use of Commercial-Off-The-Shelf (COTS) Electrical, Electronic, and Electromechanical (EEE) Parts for NASA Missions (NESC-RP-19-01490)
 2. Leverage automotive quality and reliability approach to retire risks regarding quality and reliability
 3. Promote board level qualification and reliability methodology as means to address system level reliability and process vs lot based qualification schemes



Snapdragon SA8155P SoC (7nm)

- The SA8155P is the automotive version of the 7nm 855 mobile phone device
- SA8155P is designed for use in a vehicle display and instrument cluster and ADAS Level L1/L2 automotive cockpit platform applications.
 - 8 custom 64-bit Kryo CPUs (A76 and A55 generations)
 - Qualcomm® Adreno™ 640 GPU capable of 64-bit virtual addressing as well as hardware tessellation
 - Qualcomm® Hexagon™ 6 DSP and a Neural Processing Engine (NPU) for machine learning acceleration
- Automotive devices are gaining interest again in space community due to high standards of quality and reliability (ppb defectivity)
- Automotive device makers share a radiation effects concern of transient single event effects due to terrestrial neutron environment and process materials that produce alpha particles like ultra-low-k dielectrics.

Qualcomm Adreno, Qualcomm Hexagon, and Qualcomm FlexRender are products of Qualcomm Technologies, Inc. and/or its subsidiaries.



“Radiation Effects Characterization and System Architecture Options for the 7nm Snapdragon® SA8155P Automotive Grade System on Chip (SoC)”, D. Sheldon, et. al RADECS 2022



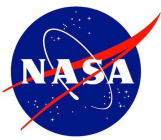
NESC Guidelines Defined Two New Terms: Industry Leading Parts Manufacturers (ILPM) and Established COTS Part (ECP)

- *Industry Leading Parts Manufacturer (ILPM)*
 - A parts manufacturer with high volume automatic production facilities and which can provide documented proof of the technology, process and product qualification, and its implementation of the best practices for “zero defects” for parts quality, reliability and workmanship.
 - Detailed criteria of ILPM and part-level verification criteria to be addressed in Phase II.
 - Recommended selecting COTS parts from *Industry Leading Parts Manufacturers*.
 - Take advantage of what commercial industry does the best - high volume automatic production manufacturer and best practices for “zero defects”



Established COTS Part is a part that:

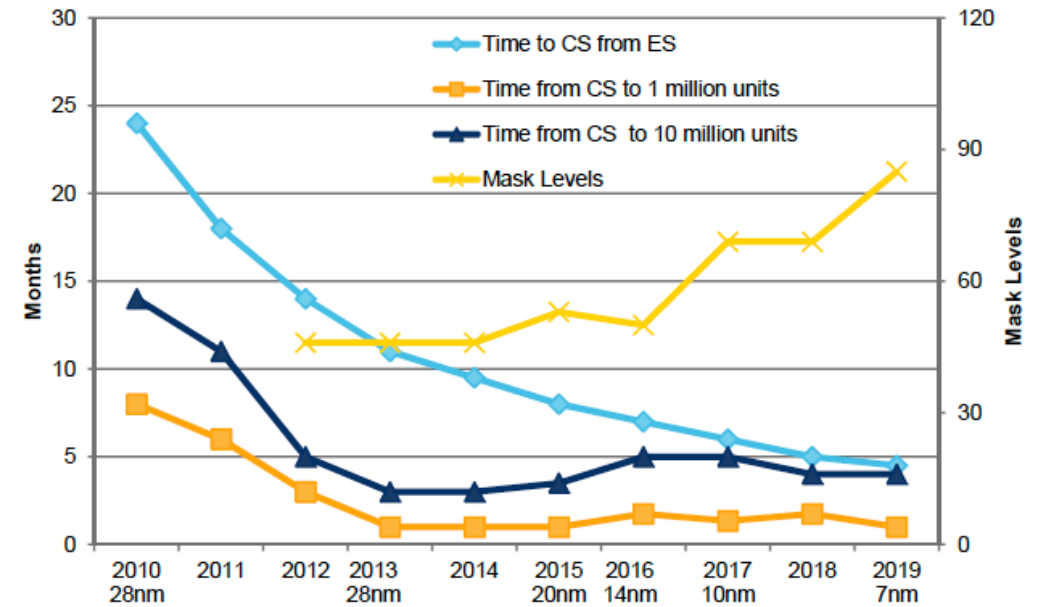
- Is produced using processes that have been stable for at least one year so there are enough data to verify the part's reliability;
- Is produced in high volume. High volume is defined as a series of parts sharing the same datasheet having a combined sales volume over one million parts during the part's lifetime;
- Is 100% electrically tested per datasheet specifications at typical operating conditions in production prior to shipping to customers. Additionally, the manufacturer must have completed multi-lot characterization over the entire set of operating conditions cited in the part's datasheet, prior to mass production release. Thus, production test limits are set for typical test conditions sufficient to guarantee that the parts will meet all parameters' performance specifications on the datasheet;
- Is produced on fully automated production lines utilizing statistical process control (SPC), and undergoes in-process testing, including wafer probing for microcircuits and semiconductors, and other means appropriate for other products (e.g., passive parts). These controls and tests are intended to maintain process tolerances and eliminate defective parts at various stages of production
- Has demonstrated consistent yield trend appropriate for high volume commercial technologies at that technology node.



Semiconductor Volume & Complexity – Opportunity and Challenges

- It's not the 1990's anymore...
- The complexity and time to introduce new semiconductors to market is profound and hard to comprehend – like no other industry
- The resulting devices are capable of providing truly revolutionary capabilities that heretofore were simply unavailable
- This enables new mission concepts – Ingenuity & SRH
- Manufacturers are investing billions of dollars to continually reduce defects and improve product quality – Space should leverage this
- Adaptation and mitigation are the key concepts to enabling successful use of game changing semiconductor technologies
- Boutique, low volume parts manufacturing cannot produce devices of this complexity.
- Criteria for meeting ILPM and ECP

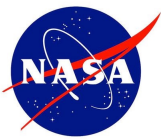
QTI Design to Volume Ships



Source: Qualcomm Technologies data



“Test, challenges with billions of transistors, terabytes of data, 5G mobile and quality”, Mike Campbell, TestConX 2019



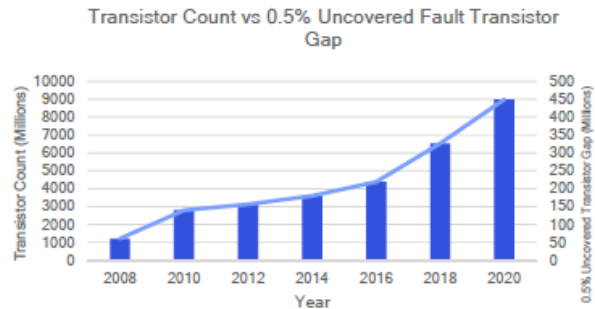
Semiconductors must constantly improve quality and reduce defects

Continuous challenges...

Mobile industry is now driving toward “almost-automotive” quality levels ($\ll 100$ DPPM)
With nearly vertical ramps in new technologies.

New technology nodes require higher number of tests:

- The 0.5% baseline fault coverage gap became TOO BIG to skip.
- EDA tools can't cover ALL faults in production.
- New fault models are needed
- ATE Vector Memory is limited
- Higher test times constrain volume



More functional tests @ NPI :

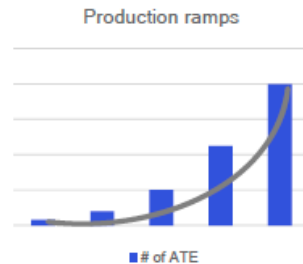
- Covering inter-block defects
- Provides gap feedback to DFT
- Helps close gap with DPPM
- Required with performance tests

Balancing Quality and Cost of Test:

- Adapt fast to higher production demands w/o quality risk increases.
- Continuous optimization of throughput capacity across family tiers.
- Live KPI monitor to guarantee all levels are met.
- Continue DFT and Test innovation solutions to address new challenges proactively.



Smarter and more adaptive test programs are needed!!



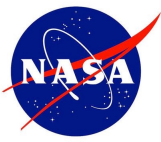
Production Ramps are going “Vertical”

- From 9 months to 3 months in latest projects.
- No room for errors
- TTR and monitor techniques in place from day 1.
- Identify effective tests ASAP

Source: Qualcomm Technologies data

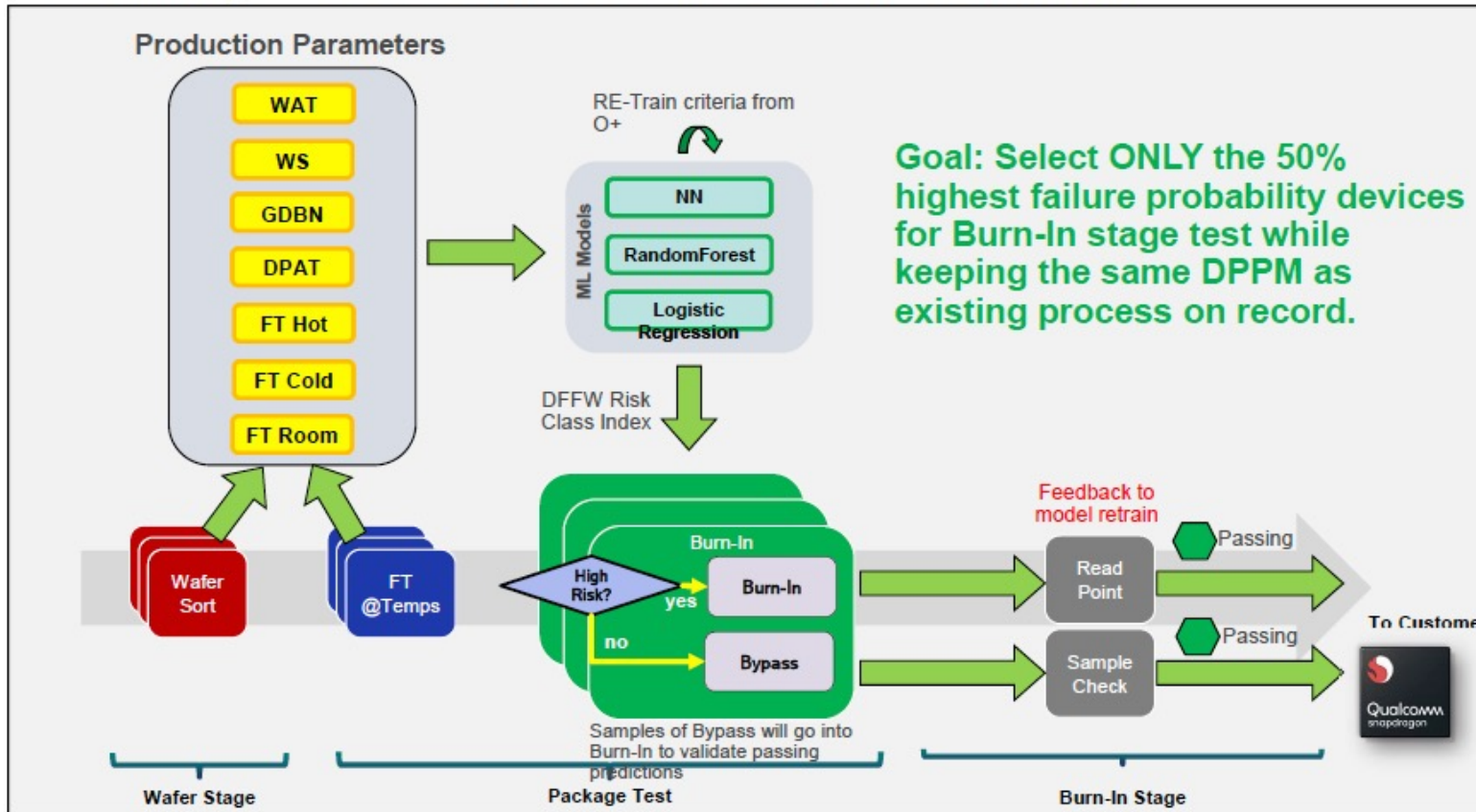
- Yield and fault coverage are fundamental concepts to success at for ILPM and ECP
- Not always true for heritage space devices
- Acknowledgement of baseline fault coverage gap
- Not addressed in existing space qualification requirements

“Test, challenges with billions of transistors, terabytes of data, 5G mobile and quality”, Mike Campbell, TestConX 2019



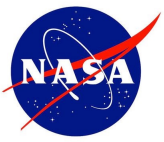
Use of AI/ML with Large Datasets to precisely meet Defect Requirements and Quality Goals

Quality - Selective devices for Burn-In



- Highlights use of NN with training data based on all production test points from wafer level to final high temperature testing
- Decision tree approach to ensure quality goals reached
- Process of record integrity is maintained and enhanced
- Criteria for meeting ILPM and ECP

"Test, challenges with billions of transistors, terabytes of data, 5G mobile and quality", Mike Campbell, TestConX 2019



Complete integration of design tools with electrical test algorithms

DFT & EDA challenges to meet < 100 DPPM requirements

Gaps in Test Mode Vs Mission Mode

EDA tools create tests only on the test modes as enabled by the Design & DFT architecture.

These test modes are expected to cover all functional paths, including cross clock domain & power domain paths - however, there may exist some gaps.

Limited EDA capabilities today to comprehensively analyze faults across all functional paths and highlight test mode gaps.

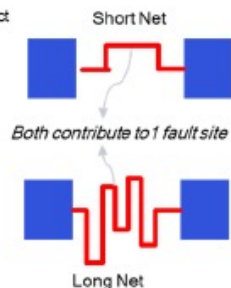


Equal Weight for all fault sites

EDA Tools assume equal defect probability and thus tend to weigh all fault sites equally.

Example: a short net and long net could have significantly different probability of defect, however, for fault accounting, they both are considered a single fault site.

Such equal weighing of faults could skew coverage metrics and impact outgoing DPPM.



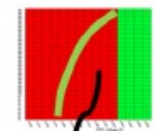
Modelling Design & Process Interactions

EDA/DFT methodologies assume ideal design margins and operate on fault models that are manufacturing defect oriented.

In advanced process nodes, Design and Process interactions are starting to cause functional path failures.

Many such functional path failures do get screened with standard DFT fault models, however, those detections are largely accidental, thus driving the need for Advanced Fault Models.

Low Voltage Failure



- Hold Marginalities
- Weak Cells (clock)
- Clock Slew
- Process Defects
- VT Shifts
- Resistive Contacts

Higher Voltage Needs for DFT Vectors

EDA tools assume perfect correlation and alignment of DFT VDDmins Vs System VDDmins.

This is not always the case, especially for high performance cores at higher power corners where a voltage boost of 20mv-50mv may be required to enable tests in production.

Such Test-Only voltage boosts could escape small delay defects from the classical Fault Model oriented defect screening.

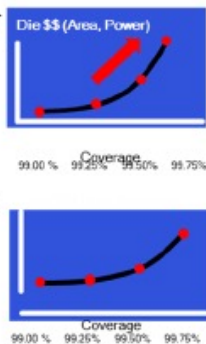


Prohibitive Cost for last 1% coverage

Significant advancements in DFT Test Compression h/w, Test Point Algorithms and best in class DFT practices have occurred in the past decade.

However, DFT (Design) cost continues to be high and increases exponentially to pick the last 1% of the fault coverage.

In addition, Test Cost (both test time and vector memory), increases significantly as coverage numbers are pushed beyond the 99% mark.

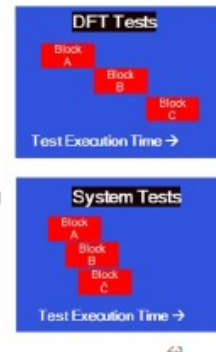


Differences in concurrency: DFT Vs SLT

EDA tools have adopted hierarchical DFT techniques to test one core at a time, unlike system tests where concurrent cores are enabled and tested simultaneously.

Such differences in concurrency between DFT and System tests put different levels of stresses and could allow for escaping subtle Power, PDN related defectivity from DFT tests.

Forward looking DFT flows are exploring testing multiple cores simultaneously, however, test power continues to be a challenge.



- DFT (Design For Test) and EDA (Electronic Design Automation)
- Continual improvement and innovation in new test methodologies to maintain quality with ever increasing complexity and commitment to yield enhancement
- Not addressed in existing space qualification requirements or captured in heritage 'upscreening' approach

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Automotive PPAP – Production Part Approval Process

- Device Specification and revision guide
- Design FMEA
- Process Flow Diagrams
- Process FMEA
- Measurement systems analysis studies
- Dimensional results
- Certificate of design, construction and qualification
- Product Materials Declaration
- AEC-Q100-009 test histograms
- Initial process studies
- ISO Certifications
- Supplier Certifications
- Part Submission Warrants

1. Ensures that a supplier can meet the manufacturability and quality requirements of the parts supplied to the customer
2. Provides evidence that the customer engineering design record and specification requirements are clearly understood and fulfilled by the supplier
3. Demonstrate that the established manufacturing process has the potential to produce the part that consistently meets all requirements during the actual production run at the quoted production rate of the manufacturing process
4. Many of these are not included in heritage space requirements

- All Qualcomm Automotive Devices (SoC, PMIC, SOM) have individual PPAPs



AEC-Q100 Qualification and Periodic Reliability Monitoring

Automotive AEC-Q100 Qual Flow

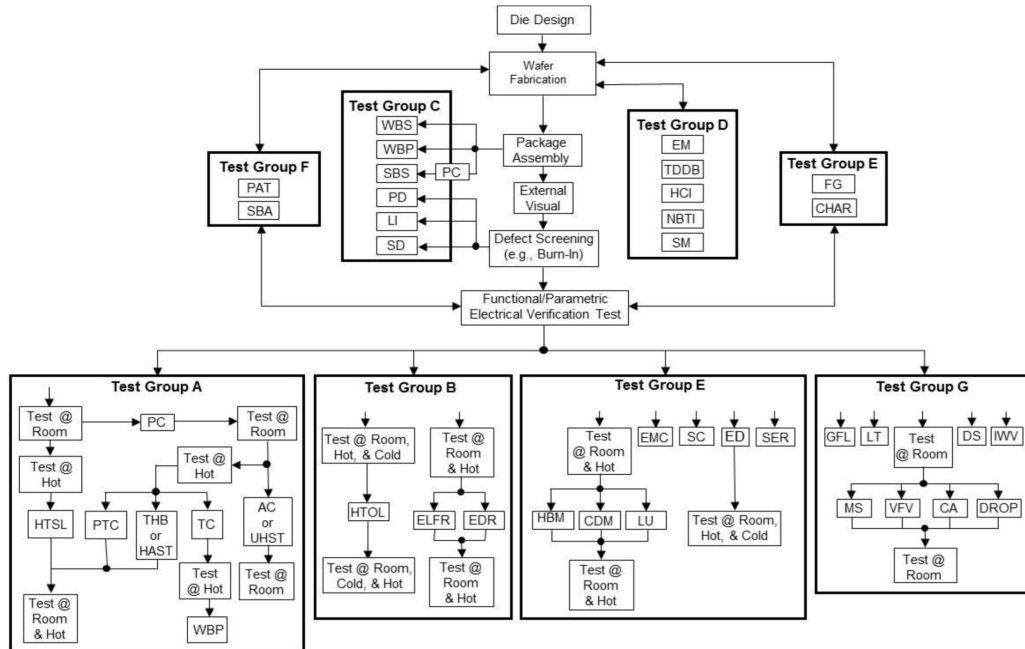


Figure 2: Qualification Test Flow

QCOM Auto Rel Monitor

Test	Sample Size	Frequency	Test Method
HTOL	1 x 77	- Quarterly for new technology 6 months for mature technology	JESD22-A106A
HAST (Unbiased & biased)	1 x 77		JESD22 – A118D & A110D
PTC	1 x 77		JESD22-A105C
Temperature Cycling	1 x 77		JESD22-A104B
HTSL	1 x 45		JESD22-A103



Risk Matrix of Available EEE Part Information for SCP BOM

Manufacturer	Part #	Quality Processes, defect reduction, traceability					Device Technology		Burn in		Radiation Testing			Risk
		Long Term Reliability Program	Documented Design Process	Production Part Approval Process	AEC-Q100 Certification of Design, Construction & Qualification	AEC-Q100 Test Histograms	Cross Section analysis	Technology specific acceleration factors and Safe Operating Area methodology	Custom Automotive BI	Board Level BI	TID	SEL	SEFI	
Qualcomm	SA8155P	1	1	1	1	1	1	1	1	1	1	1	1	12
Acme	XYZ-1000	0	0	1	1	1	0	1	0	1	0	1	0	6
Acme	XYZ-1001	0	1	1	1	1	0	0	0	1	1	1	0	7
Acme	XYZ-1002	0	1	1	1	1	1	0	0	0	1	0	0	6
Acme	XYZ-1003	1	1	0	0	1	0	0	0	0	0	0	0	3
Acme	XYZ-1004	1	0	0	0	0	1	0	1	0	1	0	0	4
Acme	XYZ-1005	0	1	1	1	1	1	1	1	0	1	1	1	10
Acme	XYZ-1006	1	0	1	1	0	0	0	1	0	1	1	1	7
Why this information is important?		Demonstrates repeatability of manufacturing process. Supports removal of lot specific requirements	Documents formal review process to ensure designs meet data sheet.	Quality control of entire process chain from wafer fab to assembly and test and shipment	Measurable standards of reliability and quality (<100 FITS @ 70C/10 yrs)	Precise part specific data that demonstrates < 1ppm population control	identify technology specific structures and confirm bias of physics models	Intrinsic physics of failure information to precisely calculate mission specific lifetime	Additional screening step to drive probability of infant mortal escaping into main population to <1e-4	Ensure flight lot has received some stress to eliminate manufacturing defects	Specific performance for space application			



NESC Recommendations

- NESC recommendations were identified and directed towards the spaceflight program or project managers, project avionics systems leads, circuit design engineers, EEE parts engineers, and the NESC.
 - COTS risk identification and mitigation: R1, 2, 3
 - Verification when using COTS parts: R4, 5
 - COTS parts selection, procurement and verification at part-level: R6, 7, 8, 9
 - COTS application and environment: R10
 - COTS for critical ground support systems: R 11
 - Class D and Sub-Class D missions: R12, 13



Different approaches are recommended according to program/project Risk Classes A, B, C, and D and human-rated missions:

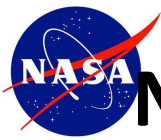
1. Recommend Classes A and B and human-rated missions consider a “MIL-SPEC parts-based design” approach. “MIL-SPEC parts-based design” approach is one in which most parts are MIL-SPEC parts and Established COTS parts from ILPMs are used only when an equivalent MIL-SPEC part does not meet functional or size, weight, and power (SWaP) or performance requirements, or is not available.
2. Recommend Classes D and Sub-D missions consider a “System of COTS” approach. “System of COTS” approach is one which most parts are Established COTS parts from ILPMs.
3. Recommend Class C missions determine which approach is the best for their projects; that is, use either a “MIL-SPEC parts-based design” approach, “System of COTS” approach, or a combined approach utilizing elements of both



NESC Recommendations - COTS risk identification and mitigation



- R-1. Programs/Projects should understand and effectively manage the risk of COTS, using a holistic approach incorporating inputs from across the project/program to make informed decisions and mitigate risk. **(F-1, F-2, F-3, F-4, O-7)**
 - Risk should be considered in the appropriate context, based on knowledge of the parts being used, the manufacturers, and how the parts are being used.
- R-2. When COTS parts are used in safety or mission critical applications without any further part-level MIL-SPEC/NASA screening and space qualification, a mission specific COTS approach tailored to project's Mission, Environment, Applications and Lifetime (MEAL) should be developed and approved by Program/Project Managers with pertinent risks clearly identified, mitigated and accepted. **(F-1, F-2, F-3, F-4, O-7)**
- R-3. For critical or single point failure applications, strategically use MIL-SPEC or NPSL parts or part/system redundancy or both where it is resource-effective (e.g., cost, schedule, or space on the board/box). **(F-1, F-7)**



NESC Recommendations - Verification when using COTS parts

- R-4. COTS parts verification should be performed at part-, board- and/or system-level. If part-level verification is largely based on the COTS manufacturer's data, then the system should be tested 500-1,000 hours of accumulated test time, with the last 200 hours being failure free. (***F-4, F-5, F-6, F-7, F-8, O-3, O-4, O-5, O-6, O-7***)
- R-5. When using COTS parts, program/project should build multiple revisions of engineering units to start functional testing, environmental testing, qualification, and verification early in the design cycle so that any issue can be addressed to minimize the impact on system risk, cost, and schedule. (***F-1b, F-3***)



NESC Recommendations - COTS parts selection, procurement and verification at part-level (I)

- R-6 When selecting COTS parts for spaceflight units, Circuit Designers should work with EEE Parts Engineers to follow the best practices including, but not limited to, the following (Section 7.10.3): **(F-5, F-6, O-1, O-2,)**
 - Select COTS parts that meet project's MEAL requirements.
 - Select COTS parts from ILPMs and the highest commercial grades parts available with each ILPM (e.g., hi-rel parts and AEC-Q parts, SAE connectors and wires, etc.);
 - Select manufacturers that possess DLA certifications for their other product lines and the highest commercial grades parts available;
 - Select COTS parts designed and manufactured with matured technologies (e.g., technology generations/nodes between 2 to 8 years old);
 - Select COTS parts that are widely used in commercial electronics;
 - Recognize that leading edge technology parts may require significant specialized effort to ensure the reliability;
 - Select parts with “flight heritage” and ensure the MEAL for the new mission is within the bounds of the previous mission.



NESC Recommendations - COTS parts selection, procurement and verification at part-level (II)

- R-7 When purchasing COTS parts for spaceflight units, Project Procurement Organization and EEE Parts Engineers should follow the best practices including but not limited to (Sections 7.2-7.9, 7.10.6, 7.10.7): **(F-8, O-6)**
 - Procure COTS parts from OCMs and authorized distributors.
 - Obtain CoC (Certificate of Conformance) and lot trace code so that parts can be traceable to a specific manufacturer, part number, and lot number.
 - Communicate with the OCMs and authorized distributors to ensure the parts are from the same wafer lots, and/or procure one reel of the parts to maximize the probability.
 - Request PPAP (Production Part Approval Process) Package (Appendix B.1) for automotive grade parts.
 - Procure a minimum quantity of 20 percent over the number of parts required to support equipment maintenance, planned future builds, and potential future builds.



NESC Recommendations - COTS parts selection, procurement and verification at part-level (III)

- R-8 When verifying COTS parts at part-level, EEE Parts Engineers should follow the best practices below (Sections 7.2- through 7.9, 7.10.4): **(F-4, F-5, F-6, F-7, F-8, O-3, O-4, O-5, O-6, O-7)**
 - Perform parts manufacturer assessment. Verify parts manufacturer has documented proof of high standards for quality, reliability and workmanship as outlined in Section 7.10.3. The levels of verification can be based on published materials (e.g., Quality Manual, DPPM and FIT rates) published on the manufacturer's website, or unpublished materials obtained through direct contact with the manufacturer, or through third party.
 - Perform re-evaluation on verified ILPMs periodically.
 - Understand parts technology. When a COTS part's construction is not fully understood or it is not selected from an ILPM, perform DPA and/or parametric/functional testing on sample parts or and any other testing necessary (e.g., x-ray, PIND, etc.) to ensure the part meet MEAL with project risk posture.
 - Recognize part-level verification may require a different set of testing other than MIL-SPEC standards.
 - Establish and maintain an ongoing relationship with parts manufacturers, especially with their local offices.
 - Monitor manufacturer changes through the monitoring of PCNs, GIDEPs, and other Alerts. Recent changes should be reviewed and the appropriate parties notified.



NESC Recommendations - COTS parts selection, procurement and verification at part-level (IV)

- R-9 EEE Parts Engineers should perform obsolescence analysis on COTS parts to ensure projected part availability exceeds mission requirements over the duration of development or reuse for serviceable missions or GSE. **(F-8, F10, F11, O-6)**
 - Evaluate part life cycle to ensure availability from hardware design and part selection to procurement and installation.
 - Coordinate with project to determine if design is a single or multiple build to ensure sufficient part quantities are procured.
 - Review manufacturer's life cycle management policy.
 - Monitor parts lists on continuous basis for obsolescence alerts.



Snapdragon Co-Processor Board Features & Interfaces

Actual SCP
(back side)

- **Coprocessor Features**

- Qualcomm SA8155P SOC
- 2x 64Gb LPDDR4 memory
- 1024Gb Non-Volatile Flash Storage
- 2Mb FRAM
- Independent rad hard (100Krad) watchdog circuit

- **Mezzanine Interfaces and I/O**

- 1x 2-lane PCIe Gen3, 2GB/s transfer rate to host
- 1x 1-lane PCIe Gen3
- 1x GigE RGMII support
- 2x UART, 1x JTAG, 14x General Purpose IO
- 5x Qualcomm Universal Peripheral ports - SPI, I2C, UART

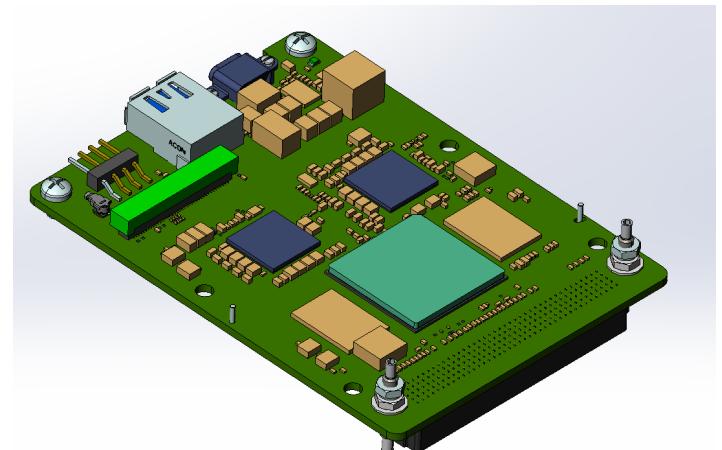
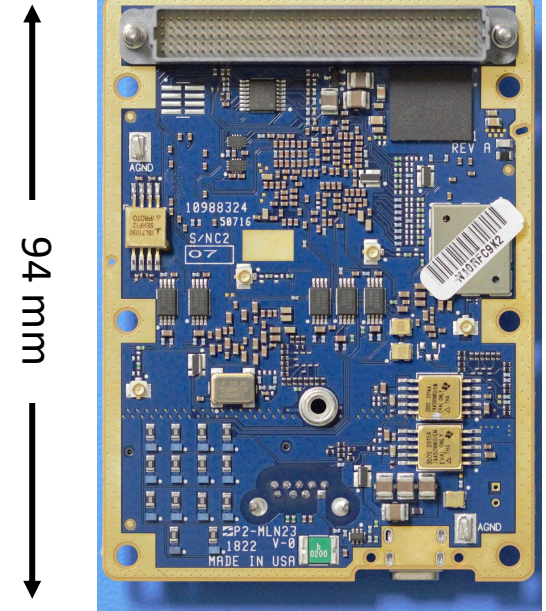
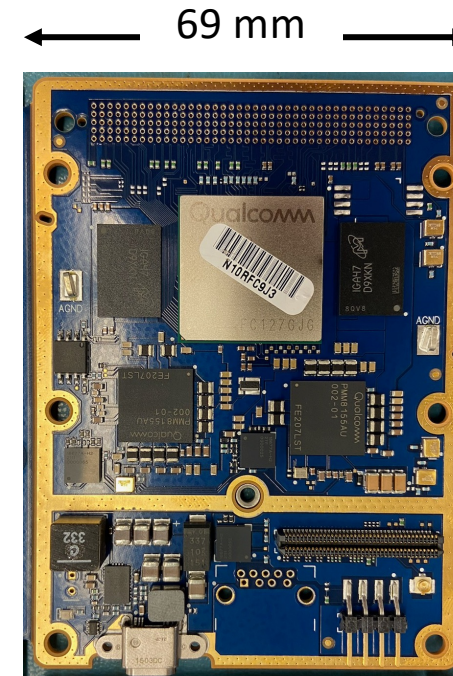
- **External Interfaces**

- 2x USB3.0 support
- 4x 4-lane MIPI Camera Serial Interface connector
- 1x Boot select Jumper

- **Mass**

- SCP with heat plate & mounting hardware -> 198 grams.
- SCP board without heat plate & mounting hardware -> 54 grams.

Actual SCP
(front side)



“Snapdragon Initiative and Common Instrument Electronics”, A. Jongeling, ISSC 2023.



Comparison of SCP to NESC Guidelines - 1

		<10%	10% to 75%	>75%
R1	Programs/Projects should understand and effectively manage the risk of COTS, using a holistic approach incorporating inputs from across the project/program to make informed decisions and mitigate risk			
R2	When COTS parts are used in safety or mission critical applications without any further part-level MIL-SPEC/NASA screening and space qualification, a mission specific COTS approach tailored to project's Mission, Environment, Applications and Lifetime (MEAL) should be developed and approved by Program/Project Managers with pertinent risks clearly identified, mitigated and accepted			
R3	For critical or single point failure applications, strategically use MIL-SPEC or NPSL parts or part/system redundancy or both where it is resource-effective (e.g., cost, schedule, or space on the board/box).			
R4	COTS parts verification should be performed at part-, board- and/or system-level. If part-level verification is largely based on the COTS manufacturer's data, then the system should be tested 500-1,000 hours of accumulated test time, with the last 200 hours being failure free			
R5	When using COTS parts, program/project should build multiple revisions of engineering units to start functional testing, environmental testing, qualification, and verification early in the design cycle so that any issue can be addressed to minimize the impact on system risk, cost, and schedule.			
R6 1	Select COTS parts that meet project's MEAL requirements.			
R6 2	Select COTS parts from ILPMs and the highest commercial grades parts available with each ILPM (e.g., hi-rel parts and AEC-Q parts, SAE connectors and wires, etc.);			
R6 3	Select manufacturers that possess DLA certifications for their other product lines and the highest commercial grades parts available			
R6 4	Select COTS parts designed and manufactured with matured technologies between 2 to 8 years old technology generations/nodes			
R6 5	Select COTS parts that are widely used in commercial electronics			
R6 6	Recognize that leading edge technology parts may require significant specialized effort to ensure the reliability			
R6 7	Select parts with "flight heritage" and ensure the MEAL for the new mission is within the bounds of the previous mission.			

		<10%	10% to 75%	>75%
R7 1	Procure COTS parts from OCMs and authorized distributors			
R7 2	Obtain CoC (Certificate of Conformance) and lot trace code so that parts can be traceable to a specific manufacturer, part number, and lot number			
R7 3	Communicate with the OCMs and authorized distributors to ensure the parts are from the same wafer lots, and/or procure one reel of the parts to maximize the probability			
R7 4	Request PPAP (Production Part Approval Process) Package (Appendix B.1) for automotive grade parts			
R7 5	Procure a minimum quantity of 20 percent over the number of parts required to support equipment maintenance, planned future builds, and potential future builds			
R 8 1	Perform parts manufacturer assessment. Verify parts manufacturer has documented proof of high standards for quality, reliability and workmanship as outlined in Section 7.10.3. The levels of verification can be based on published materials (e.g., Quality Manual, DPPM and FIT rates) published on the manufacturer's website, or unpublished materials obtained through direct contact with the manufacturer, or through third party			
R 8 2	Perform re-evaluation on verified ILPMs periodically			
R 8 3	Understand parts technology. When a COTS part's construction is not fully understood or it is not selected from an ILPM, perform DPA and/or parametric/functional testing on sample parts or and any other testing necessary (e.g., x-ray, PIND, etc.) to ensure the part meet MEAL with project risk posture			
R 8 4	Recognize part-level verification may require a different set of testing other than MIL-SPEC standards			
R 8 5	Establish and maintain an ongoing relationship with parts manufacturers, especially with their local offices			
R 8 6	Monitor manufacturer changes through the monitoring of PCNs, GIDEPs, and other Alerts. Recent changes should be reviewed and the appropriate parties notified			



Comparison of SCP to NESCC Guidelines - 2

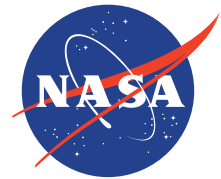
R 9 1	Evaluate part life cycle to ensure availability from hardware design and part selection to procurement and installation.			
R 9 2	Coordinate with project to determine if design is a single or multiple build to ensure sufficient part quantities are procured			
R 9 3	Review manufacturer's life cycle management policy			
R 9 4	Monitor parts lists on continuous basis for obsolescence alerts			
R10 1	Identify environments (e.g., thermal, vibe, helium, radiation, partial vacuum atmosphere plasma arcing/discharge) that might be			
R10 2	Use manufacturers' SPICE models and demonstration and/or evaluation boards for circuit verification, and implement board- and system-level verification early on in the development cycle to avoid negative impact on cost and schedule should any failure occur			
R10 3	Use more conservative derating for COTS parts in comparison to its MIL-SPEC counterpart to achieve comparable reliability, notwithstanding other pertinent attributes of either type of part			
R10 4	Use commercial version of radiation-tolerant parts, if available. Some parts are offered in both commercial versions and versions with known radiation tolerance (and often additional screening tests applied). Using the commercial versions of those parts can offer similar radiation tolerance, and also allow savings in cost and lead time. This needs to be evaluated on a case by case basis to ensure that the commercial version of the parts have comparable traceability to their radiation tolerant counterparts			
R10 5	Design for radiation tolerance at board and subsystem level, if not possible at part level, by using and validating strategic redundancy, circuit mitigation (e.g. watchdog circuits) and power cycling to limit functional disruption during nondestructive radiation upsets, and circuit mitigation (e.g. watchdog circuits) and power cycling to limit functional disruption during nondestructive radiation upsets, and reduce or eliminate (e.g. over-current protection) the effects of potentially destructive upsets such as micro-latchup and SEB failure, and other mitigations (HW & SW) through circuit designs.			
R10 6	Radiation-tolerant circuit design should play more significant role compared to individual part radiation hardness efforts, whether using COTS (or MIL-SPEC parts in this matter). For COTS parts, plan on more extensive radiation testing and mitigation than with MIL-SPEC counterparts, as there should be a greater level of expectation that radiation will cause a problem			

R 11 1	Circuit Designers should collaborate with Parts Engineers to assure required performance characteristics are within specified datasheet parameters over the mission lifetime			
R 11 2	Circuit Designers and Parts Engineers should collaborate in identifying environments (e.g., thermal, humidity, shock, vibration, helium or other gases, vacuum, atmosphere, etc.) that might cause problems in their applications (whether at the part or at higher integration levels). Such issues may require additional testing and/or analysis to verify the circuit(s) operates as intended			
R 11 3	Circuit Designers should use manufacturers' models (e.g., SPICE, Verilog, VHDL), if available, to verify worst-case conditions (e.g., temperature, voltages, timing, radiation degradation, End-of-Line-electrical performance degradation, SEE impacts, SET circuit impacts, residual rates after TMR implementation, etc.). Use demonstration and/or evaluation boards for circuit verification. Implement board- and box-level verification early in the development cycle to avoid negative impacts on cost and schedule should any problems or failures arise			
R 11 4	Circuit Designers should use more conservative derating for COTS parts, mainly passive parts, where appropriate, compared to MIL-SPEC counterparts, notwithstanding other pertinent attributes of either type of part. For example, MIL-SPEC ceramic capacitors (e.g., MIL-PRF-55681 and MIL-PRF-123) are designed to handle extended operation at twice the rated voltage, but COTS ceramic capacitors are designed largely to tolerate the datasheet limits with minimal over-rated voltage excursions			
R 11 5	When resources or availability prohibit using rad-hard MIL-SPEC parts, Circuit Designers and Parts Engineers should consider the commercial version of radhard parts, if the rad-hard parts and commercial version of the rad-hard parts have the same silicon die. Some rad-hard parts have non-rad-hard commercial versions available with the same die, where the main difference is that no radiation testing has been performed on the commercial version. These parts offer similar radiation tolerance (but without the radiation hardness guarantees of the rad-hard versions) and may allow savings in cost and procurement time. When using the commercial version, it must be acknowledged that the part is considered non-rad-hard and is subject to relevant guidance in this report. For Class D and Sub-Class D projects, this would provide a good solution when available and, in some cases, it might be the only choice available in lower-risk-tolerant applications			



Summary

- The Qualcomm Snapdragon SoC parts meet the requirements of the ILPM and ECP
- The NESC guidelines provide a robust methodology to mitigate risks of COTS usage for NASA missions
- The board level vs part level qualification approach has significant advantages and helps bridge the gap to Class B requirements



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